2009 SYMPOSIUM ON VLSI CIRCUITS

Welcome to the 2009 Symposium on VLSI Circuits

You are cordially invited to attend the 2009 Symposium on VLSI Circuits, to be held on June 16-18th, 2009, at the Rihga Royal Hotel Kyoto in Kyoto, Japan. We are repeating last year's successful two day overlap with the Technology symposium to foster greater communication between these two key gatherings. The juxtaposition of these two conferences is one of the unique features that distinguish the Symposia from other gatherings. The Symposium brings experts and experienced engineers and scientists from around the world together to discuss the present and future challenges in VLSI Circuits and Technology.

Preceding the Symposium on June 15th, a one-day Short Course will be held. This short course will focus on "Energy Management for Green SoC's and SiP's" where experts will give educational talks on this timely topic in VLSI circuits. On the same day, we have a Workshop on "MM-Wave and Multi-Gigabit Transceivers for High- Speed Wireless Communication." With a single Short Course/ Workshop registration fee you can select to attend either session. The new highlight of the conference is the Luncheon. This year's speaker will be Kosuke Hayakawa from Central Japan Railway Company with a talk on "The Series N700 and the Tokaido Shinkansen". This is a great opportunity to hear from one of the developers of this icon of Japanese transportation on its history and future. This year, the technical program committee reviewed 313 papers and selected 110 papers for presentation covering a range of topics from Digital Circuits and Systems, Memories, Analog, Data Converters, Wireless and Wireline Communications. The core tradition of the Symposium is the paper quality and this year the committee has selected very high quality papers representing the scope of the symposium. We have also invited four distinguished speakers to describe recent advances and new challenges in the areas of Nanotechnology, Medical Electronics, Mobile and Personal Communication and Networking. To complement the formal talks, we have arranged two evening sessions on interesting and provocative subjects to give you an opportunity to participate in the discussions and mix with the participants. The evening sessions explore: "Energy Efficiency: How is 'Green' Implemented in Reality?" and "32nm SoC and Beyond – Reliable or Not?" The rich technical content of the program will undoubtedly interest you, and we certainly hope that the Symposium will be a fruitful and enjoyable experience. This booklet contains the advance program together with forms for the Symposium registration and hotel reservations. Please complete and return these forms or visit our website for online registration at http://www.vlsisymposium. org/symposia.html. Although on-site registration will be available at the conference, preregistration will facilitate Symposium planning. We look forward to meeting with you at the Symposium in Kyoto.

Masayuki Mizuno Ajith Amerasekera

Program Chair Program Co-Chair

CONFERENCE SCHEDULE

Sunday, June 14	8:00-17:00	Registration	
Monday, June 15	7:30-17:00	Registration	
	8:10-12:00	Short Course [Suzaku I] / Workshop [Suzaku III]	
	13:30-17:15	Short Course [Suzaku I] / Workshop [Suzaku III]	
	20:00-22:00	Joint Rump Session [Suzaku I,II]	
Tuesday, June 16	7:30-17:00	Registration	
	8:30-10:05	Session 1	**Welcome and Plenary Session I [Suzaku I, II]**
	10:30-12:35	Session 2	**CDRs and Limiting Amplifiers [Suzaku I]**
		Session 3	**Non-Volatile and Fuse Memories [Suzaku II]**
		Session 4	**Biomedical and Personal Technology [Suzaku III]**
	12:35-13:55	Lunch	
	13:55-16:00	Session 5	**Transmitters and Receivers [Suzaku I]**
		Session 6	**Biomedical and Sensors [Suzaku III]**
	13:55-15:10	Speci al Session [Shunju I, II]	
	16:10-17:50	Session 7	**Sigma-Delta ADCs [Suzaku I]**
		Session 8	**Special Non-Volatile Memories [Suzaku II]**
		Session 9	**Data Interconnect Technology [Suzaku III]**
	19:00-21:00	Joint Dinner	
Wednesday, June 17	8:00-17:00	Registration	
	8:45-10:05	Session 10	**Plenary Session II [Suzaku I, II]**
	10:30-12:35	Session 11	**Reliability and Security [Suzaku I]**
		Session 12	**Clock Generators [Suzaku III]**
	12:35-14:20	Lunch	Luncheon Talk [Suzaku II](12:45-14:05)
	14:20-16:00	Session 13	**DRAM and Interface [Suzaku I]**
		Session 14	**Discrete-Time Analog [Suzaku III]**
	16:15-17:55	Session 15	**SRAMS and Clock Circuits [Suzaku I]**
		Session 16	**DC-DC Converters [Suzaku III]**
	20:00-22:00	Rump Sessions [Suzaku I, II, III]	
		Special Evening Session	
Thursday, June 18	8:00-15:00	Registration	
	8:30-10:10	Session 17	**Image Sensors [Suzaku I]**

		Session 18	**Frequency Synthesizers [Suzaku II]**
		Session 19	**Power Management and High-Efficiency Logic [Suzaku III]**
	10:30-12:10	Session 20	**Analog Techniques [Suzaku I]**
		Session 21	**Advanced Equalizers [Suzaku II]**
		Session 22	**Clock Generation Techniques [Suzaku III]**
	12:10-13:30	Lunch	
	13:30-15:10	Session 23	**Low Power ADCs [Suzaku I]**
		Session 24	**MM-Wave Techniques [Suzaku II]**
		Session 25	**Media Processor Architecture [Suzaku III]**
	15:25-17:05	Session 26	**High-Speed ADCs [Suzaku I]**
		Session 27	**Wireless Transceivers [Suzaku II]**
		Session 28	**Signal Processing [Suzaku III]**

PROGRAM

Tuesday, June 16

Session 1		**Welcome and Plenary Session I [Suzaku I, II]**
Chairpersons		M. Mizuno, *NEC Corp.* A. Amerasekera, *Texas Instruments*
8:30	1-1	**Welcome and Opening Remarks**
		K. Yano, *Hitachi, Ltd.* K. Nakamura, *Analog Devices, Inc.*
8:45	1-2	**Challenges in Nanoelectronics: Dream or Reality?**
Invited		N. Yokoyama, *Fujitsu Laboratories Ltd.*
9:25	1-3	**Creating Support Circuits for the Brain: VLSI for Brain Machine Interfacing**
Invited		T. Denison, *Medtronic, Inc.*

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(Break 10:05-10:30)

Tuesday, June 16

Session 2		**CDRs and Limiting Amplifiers [Suzaku I]**
Chairpersons		J. Lee, *National Taiwan Univ.* K. Chang, *Rambus Inc.*
10:30	2-1	**A 2 x 22Gb/s SFI5.2 CDR/Deserializer in 65nm CMOS Technology**
Abstract		N. Nedovic*, S. Parikh*, A. Kristensson*, N. Tzartzanis*, W. Walker*, S. Reddy*, H. Tamura**, S. McLeod*, T. Yamamoto**, Y. Doi**, J. Ogawa**, M. Kibune**, T. Shibasaki**, T. Hamada**, Y. Tomita**, T. Ikeuchi***,**** and N. Kuwata***,****
		**Fujitsu Laboratories of America,USA, **Fujitsu Laboratories Ltd., ***Fujitsu Ltd. and ****OITDA, Japan*

10:55	2-2	**Adaptation of CDR and Full Scale Range of ADCBased SerDes Receiver**
Abstract		E.-H. Chen*, W. Leven**, N. Warke**, A. Joy***, S. Hubbins**, A. Amerasekera** and C.-K. K. Yang*
		**University of California, Los Angeles, **Texas Instruments, Dallas, USA and ***Texas Instruments, Northampton, United Kingdom*
11:20	2-3	**A Reference-Free, Digital Background Calibration Technique for Gated-Oscillator-Based CDR/PLL**
Abstract		C.-F. Liang, S.-C. Hwu, Y.-H. Tu, Y.-L. Yang and H.-S. Li
		MediaTek, Taiwan
11:45	2-4	**A Digital Offset-Compensation Scheme for an LA and CDR in 65-nm CMOS**
Abstract		S. McLeod*, A. Sheikholeslami*, T. Yamamoto**, N. Nedovic***, H. Tamura** and W.W. Walker***
		**University of Toronto, Canada, **Fujitsu Laboratories Limited, Japan and ***Fujitsu Laboratories of America, USA*
12:10	2-5	**A 10-Gb/s Burst-Mode Limiting Amplifier Using a Two-Stage Active Feedback Circuit**
Abstract		M. Nogawa, K. Nishimura, J. Terada, M. Nakamura, S. Nishihara and Y. Ohtomo
		Nippon Telegraph and Telephone Corporation, Japan

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(Lunch 12:35-13:55)

Tuesday, June 16

Session 3		**Non-Volatile and Fuse Memories [Suzaku II]**
Chairpersons		H. Yamauchi, *Fukuoka Institute of Technology* G. Lehmann, *Infineon Technologies AG*
10:30	3-1	**Multi-Stacked 1G Cell/Layer Pipe-Shaped BiCS Flash Memory**
Abstract		T. Maeda, K. Itagaki, T. Hishida, R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, H. Aochi, Y. Iwata and Y. Watanabe
		Toshiba Corporation, Semiconductor Company, Japan
10:55	3-2	**Dynamic Vpass ISPP Scheme and Optimized Erase Vth Control for High Program Inhibition in MLC NAND Flash Memories**
Abstract		K.-T. Park, M. Kang, S. Hwang, Y. Song, J. Lee, H. Joo, H.-S. Oh, J.-h. Kim, Y.-t. Lee, C. Kim and W. Lee
		Samsung Electronics Co., Ltd., Korea
11:20	3-3	**Digital Rosetta Stone: A Sealed Permanent Memory with Inductive-Coupling Power and Data Link**
Abstract		Y. Yuxiang*, N. Miura*, S. Imai**, H. Ochi*** and T. Kuroda*
		**Keio University, **Sharp Corporation and ***Kyoto University, Japan*
11:45	3-4	**High-Density 3-D Metal-Fuse PROM Featuring 1.37μm^2 1T1R Bit Cell in 32nm High-k Metal-Gate CMOS Technology**
Abstract		S.H. Kulkarni, Z. Chen, J. He, L. Jiang, B. Pedersen and K. Zhang
		Intel Corporation, USA
12:10	3-5	**A 1.25μm^2 Cell 32Kb Electrical Fuse Memory in 32nm CMOS with 700mV Vddmin and Parallel/Serial Interface**
		S. Chung, T.-W. Chung, P.-Y. Ker and F.-L. Hsueh

Abstract	*Taiwan Semiconductor Manufacturing Corp., Taiwan*

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(Lunch 12:35-13:55)

Tuesday, June 16

Session 4		**Biomedical and Personal Technology [Suzaku III]**
Chairpersons		S. Mutoh, *NTT Corp.* T. Kwan, *Broadcom Corp.*
10:30	4-1	**Asymmetric RF Tags for Ingestible Medication Compliance Capsules**
Abstract		H. Yu, C.-M. Tang and R. Bashirullah
		University of Florida, USA
10:55	4-2	**A 490uW Fully MICS Compatible FSK Transceiver for Implantable Devices**
Abstract		J. Bae, N. Cho and H.-J. Yoo
		KAIST, Korea
11:20	4-3	**A Super-Regenerative ASK Receiver with ΔΣ Pulse-Width Digitizer and SAR-Based Fast Frequency Calibration for MICS Applications**
Abstract		Y.-H. Liu, H.-H. Liu and T.-H. Lin
		National Taiwan University, Taiwan
11:45	4-4	**A 0.2mm^2, 27Mbps 3mW ADC/FFT-Less FDM BAN Receiver with Energy Exploitation Capability**
Abstract		H. Ishizaki and M. Mizuno
		NEC Corporation, Japan
12:10	4-5	**A Dynamic Real-Time Capacitor Compensated Inductive Coupling Transceiver for Wearable Body Sensor Network**
Abstract		S. Lee, J. Yoo, H. Kim and H.-J. Yoo
		KAIST, Korea

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(Lunch 12:35-13:55)

Tuesday, June 16

Session 5		**Transmitters and Receivers [Suzaku I]**
Chairpersons		C. Kim, *Samsung Electronics Co.,Ltd.* J. Wieser, *National Semiconductor Corp.*
13:55	5-1	**A 0.6mW/Gbps, 6.4-8.0Gbps Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90nm CMOS**
Abstract		K. Hu*, T. Jiang*, J. Wang*, F. O'Mahony** and P.Y. Chiang*
		**Oregon State University and **Intel Corporation, USA*
14:20	5-2	**A 40-Gb/s Transmitter with 4:1 MUX and Subharmonically Injection-Locked CMU in 90-nm CMOS Technology**
Abstract		H. Wang and J. Lee
		National Taiwan University, Taiwan
14:45	5-3	**A 21-Gb/s 87-mW Transceiver with FFE/DFE/Linear Equalizer in 65-nm CMOS Technology**

Abstract		H. Wang*, C.-C. Lee**, A.-M. Lee** and J. Lee*
		**National Taiwan University and **Realtek Semiconductor Corp., Taiwan*
15:10	5-4	**A 12-Gb/s Transceiver in 32-nm Bulk CMOS**
Abstract		S. Joshi, J. T.-S. Liao, Y. Fan, S. Hyvonen, M. Nagarajan, J. Rizk, H.-J. Lee and I. Young
		Intel Corporation, USA
15:35	5-5	**Self-Calibrating Transceiver for Source Synchronous Clocking System with On-Chip TDR and Swing Level Control Scheme**
Abstract		Y.-C. Jang, J.-Y. Park, S. Shin, H. Choi, K. Lee, B. Woo, H. Park, W.-S. Kim, Y. Choi, J. Kim, H.-K. Kim, J. Kim, S. Lim, S.-J. Chung, S. Kim, J. Yoo and C. Kim
		Samsung Electronics Co., LTD, Korea

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(Break 16:00-16:10)

Tuesday, June 16

Session 6		**Biomedical and Sensors [Suzaku III]**
Chairpersons		K. Nakahara, *Sharp Corp.* J. Dawson, *Massachusetts Institute of Technology*
13:55	6-1	**A 190µW-915MHz Active Neural Transponder with 4-Channel Time Multiplexed AFE**
Abstract		Z. Xiao, C.-M. Tang, C.-C. Peng, H. Yu and R. Bashirullah
		University of Florida, USA
14:20	6-2	**A 2.6-µW Sub-Threshold Mixed-Signal ECG SoC**
Abstract		S. C. Jocke, J. F. Bolus, S. N. Wooters, A. D. Jurik, A. C. Weaver, T. N. Blalock and B. H. Calhoun
		University of Virginia, USA
14:45	6-3	**A Micro-Power EEG Acquisition SoC with Integrated Seizure Detection Processor for Continuous Patient Monitoring**
Abstract		N. Verma, A. Shoeb, J.V. Guttag and A.P. Chandrakasan
		Massachusetts Institute of Technology, USA
15:10	6-4	**A CMOS Accelerometer Using Bondwire Inertial Sensing**
Abstract		Y.-T. Liao, W. Biederman and B. Otis
		University of Washington, USA

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(Break 15:35-16:10)

Tuesday, June 16

Special Session		**Technology Highlights [Shunju I, II]**
Chairpersons		S.S. Chung, *National Chiao Tung Univ.* K. Schruefer, *Infineon Technologies AG*
13:55	T7-1	**Pipe-Shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices**
		R. Katsumata*, M. Kito*, Y. Fukuzumi*, M. Kido*, H. Tanaka*, Y. Komori*, M. Ishiduki*, J. Matsunami*, T. Fujiwara*, Y. Nagata***, L. Zhang**, Y. Iwata*, R. Kirisawa*, H. Aochi* and A. Nitayama*
		Toshiba Corporation, Semiconductor Company,Toshiba Corporation and ***Toshiba*

		Information Systems (Japan) Corporation, Japan
14:20	T7-2	**Extremely Scaled Gate-First High-k/Metal Gate Stack with EOT of 0.55 nm Using Novel Interfacial Layer Scavenging Techniques for 22nm Technology Node and Beyond**
		K. Choi*, H. Jagannathan**, C. Choi***, L. Edge**, T. Ando***, M. Frank***, P. Jamison***, M. Wang***, E. Cartier***, S. Zafar***, J. Bruley***, A. Kerber*, B. Linder***, A. Callegari***, Q. Yang***, S. Brown***, J. Stathis***, J. Iacoponi*, V. Paruchuri** and V. Narayanan***
		**Advanced Micro Devices, Inc., **IBM Research Division and ***IBM Research Division, T.J. Watson Research Center, USA*
14:45	T7-3	**High Performance 32nm SOI CMOS with High-k/ Metal Gate and 0.149µm^2 SRAM and Ultra Low-k Back End with Eleven Levels of Copper**
		B. Greene*, Q. Liang*, K. Amarnath**, Y. Wang*, J. Schaeffer***, M. Cai*, Y. Liang*, S. Saroop*, J. Cheng**, A. Rotondaro*, S-J. Han*, R. Mo*, K. McStay*, S. Ku*, R. Pal**, M. Kumar*, B. Dirahoui*, B. Yang**, F. Tamweber*, W-H. Lee*, M. Steigerwalt*, H. Weijtmans**, J. Holt*, L. Black**, S. Samavedam***, M. Turner***, K. Ramani**, D. Lee**, M. Belyansky*, M. Chowdhury***, D. Aimé***, B. Min***, H. van Meer**, H. Yin*, K. Chan*, M. Angyal*, M. Zaleski***, O. Ogunsola*, C. Child**, L. Zhuang*, H. Yan*, D. Permana**, J. Sleight*, D. Guo*, S. Mittl*, D. Ioannou*, E. Wu*, M. Chudzik*, D-G. Park*, D. Brown**, S. Luning**, D. Mocuta*, E. Maciejewski*, K. Henson* and E. Leobandung*
		**IBM Semiconductor Research and Development Center (SRDC), **Advanced Micro Devices Inc, ***Freescale Semiconductor, USA*
15:10	T7-4	**Characteristics of sub 5nm Tri-Gate Nanowire MOSFETs with Single and Poly Si Channels in SOI Structure**
		S.D. Suk, M. Li, Y.Y. Yeoh, K.H. Yeo, J. K. Ha, H. Lim, H.W. Park, D.-W. Kim, T.Y. Chung, K.S. Oh and W.-S. Lee
		Samsung Electronics Co., Korea

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(Break 15:35-16:10)

Tuesday, June 16

Session 7		**Sigma-Delta ADCs [Suzaku I]**
Chairpersons		M. Song, *Dongguk Univ.* U.-K. Moon, *Oregon State Univ.*
16:10	7-1	**A 5th-Order Delta-Sigma Modulator with Single- Opamp Resonator**
Abstract		K. Matsukawa*, Y. Mitani*, M. Takayama*, K. Obata*, S. Dosho* and A. Matsuzawa**
		**Panasonic Corporation and **Tokyo Institute of Technology, Japan*
16:35	7-2	**A 500kHz-10MHz Multimode Power-Performance Scalable 83-to-67dB DR CTΔΣ in 90 nm Digital CMOS with Flexible Analog Core Circuitry**
Abstract		P. Crombez*,**, G. Van der Plas*, M. Steyaert** and J. Craninckx*
		**IMEC and **ESAT-MICAS, Belgium*
17:00	7-3	**Technology Portable, 0.04mm^2, Ghz-Rate ΣΔ Modulators in 65nm and 45nm CMOS**
Abstract		R.H.M. van Veldhoven, N. Nizza and L.J. Breems
		NXP Semiconductor, The Netherlands
17:25	7-4	**A 79dB 80MHz 8X-OSR Hybrid Delta- Sigma/Pipeline ADC**
		O. Rajaee*,T. Musah*, S. Takeuchi**, M. Aniya**, K. Hamashita**, P. Hanumolu* and U. Moon*

Abstract	**Oregon State University, USA and **Asahi Kasei EMD Corporation, Japan*

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(Joint Dinner 19:00-21:00)

Tuesday, June 16

Session 8		**Special Non-Volatile Memories [Suzaku II]**
Chairpersons		S.C. Chung, *TSMC* O. Jungroth, *Intel Corp.*
16:10	8-1	**Ferroelectric(Fe)-NAND Flash Memory with Non- Volatile Page Buffer for Data Center Application Enterprise Solid-State Drives (SSD)**
Abstract		T. Hatanaka*, R. Yajima*, T. Horiuchi**, S. Wang**, X. Zhang**, M. Takahashi**, S. Sakai** and K. Takeuchi*
		**The University of Tokyo and **National Institute of Advanced Industrial Science and Technology, Japan*
16:35	8-2	**Fabrication of a Nonvolatile Lookup-Table Circuit Chip Using Magneto/Semiconductor-Hybrid Structure for an Immediate-Power-Up Field Programmable Gate Array**
Abstract		D. Suzuki*, M. Natsui*, S. Ikeda*, H. Hasegawa*, K. Miura*,**, J. Hayakawa**, T. Endoh*, H. Ohno* and T. Hanyu*
		**Tohoku University and **Hitachi, Ltd., Japan*
17:00	8-3	**A 5ns Fast Write Multi-Level Non-Volatile 1 K Bits RRAM Memory with Advance Write Scheme**
Abstract		S.-S. Sheu*,**, P.-C. Chiang*, W.-P. Lin*, H.-Y. Lee*,****, P.-S. Chen***, Y.-S. Chen*, T.-Y. Wu*, F.T. Chen*, K.-L. Su*, M.-J. Kao*, K.-H. Cheng** and M.-J. Tsai*
		**ITRI, **National Central University, ***MingShin University of Science & Technology and ****National Tsing Hua University, Taiwan*
17:25	8-4	**32-Mb 2T1R SPRAM with Localized Bi-Directional Write Driver and '1'/'0' Dual-Array Equalized Reference Cell**
Abstract		R. Takemura*, T. Kawahara*, K. Miura*,**, H. Yamamoto*,**, J. Hayakawa*, N. Matsuzaki*, K. Ono*, M. Yamanouchi*, K. Ito*, H. Takahashi*, S. Ikeda**, H. Hasegawa*,**, H. Matsuoka* and H. Ohno**
		**Hitachi, Ltd. and **Tohoku University, Japan*

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(Joint Dinner 19:00-21:00)

Tuesday, June 16

Session 9		**Data Interconnect Technology [Suzaku III]**
Chairpersons		H. Kabuo, *Panasonic Corp.* J. Holst, *Cisco Systems*
16:10	9-1	**Crosstalk-Aware PWM-Based On-Chip Global Signaling in 65nm CMOS**
Abstract		J.-s. Seo, D. Sylvester and D. Blaauw
		University of Michigan, USA
16:35	9-2	**A Simultaneous Tri-Band On-Chip RF-Interconnect for Future Network-on-Chip**
Abstract		S.-W. Tam, E. Socher, A. Wong and M.-C.F. Chang
		University of California Los Angeles, USA

17:00	9-3	**A 4.7Gb/s Inductive Coupling Interposer with Dual Mode Modem**
Abstract		S. Kawai, H. Ishikuro and T. Kuroda
		Keio University, Japan
17:25	9-4	**A Scalable 3D Processor by Homogeneous Chip Stacking with Inductive-Coupling Link**
Abstract		Y. Kohama, Y. Sugimori, S. Saito, Y. Hasegawa, T. Sano, K. Kasuga, Y. Yoshida, K. Niitsu, N. Miura, H. Amano and T. Kuroda
		Keio University, Japan

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(Joint Dinner 19:00-21:00)

Wednesday, June 17

Session 10		**Plenary Session II [Suzaku I, II]**
Chairpersons		M. Mizuno, *NEC Corp.* A. Amerasekera, *Texas Instruments*
8:45	10-1	**Future of Mobile Devices - Challenges for Energy Efficient Sensing, Computing and Communication**
Invited		T. Rynahen, *Nokia Strategic Research*
9:25	10-2	**A Human - Area Networking Technology as a Universal Interface – Communication through Natural Human Actions: Touching, Holding, Stepping –**
Invited		Y. Kado, *NTT Microsystem Integration Laboratories*

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(Break 10:05-10:30)

Wednesday, June 17

Session 11		**Reliability and Security [Suzaku I]**
Chairpersons		K. Kobayashi, *Kyoto Univ.* A. Bhavnagarwala, *IBM TJ Watson Research Center*
10:30	11-1	**An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB**
Abstract		J. Keane, D. Persaud and C.H. Kim
		University of Minnesota, USA
10:55	11-2	**Post-Silicon Tuning Capabilities of 45nm Low- Power CMOS Digital Circuits**
Abstract		M. Meijer*, B. Liu**, R. van Veen* and J.P. de Gyvez*,**
		**NXP Semiconductors and **Technical University of Eindhoven, The Netherlands*
11:20	11-3	**Tunable Replica Circuits and Adaptive Voltage- Frequency Techniques for Dynamic Voltage, Temperature, and Aging Variation Tolerance**
Abstract		J. Tschanz, K. Bowman, PS. Walstra, M. Agostinelli, T. Karnik and V. De
		Intel, USA
11:45	11-4	**Tunable Duplex LSIs Achieved by Multiple Phase- Modulated Clocks Capable of Predicting Delay- Increase and -Decrease Faults**
Abstract		Y. Kameda and M. Mizuno
		NEC Corporation, Japan

12:10	11-5	**Silicon Physical Unclonable Function Resistant to a 10^{25}-Trial Brute Force Attack in 90 nm CMOS**
Abstract		S. Stanzione and G. Iannaccone
		Università di Pisa, Italy

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(Lunch 12:35-14:20)

Wednesday, June 17

Session 12		**Clock Generators [Suzaku III]**
Chairpersons		S. Dosho, *Panasonic Corp.* J. Barth, *IBM Microelectronics*
10:30	12-1	**Multi-Decade Carrier Generation for Cognitive Radios**
Abstract		B. Razavi
		University of California, Los Angeles, USA
10:55	12-2	**A 1.3GHz 350mW Hybrid Direct Digital Frequency Synthesizer in 90nm CMOS**
Abstract		H.C. Yeoh, J.-H. Jung, Y.-H. Jung and K.-H. Baek
		Chung-Ang University, Korea
11:20	12-3	**A Bandwidth Tracking Technique for a 65nm CMOS Digital Phase-Locked Loop**
Abstract		P.-H. Hsieh, J. Maxey* and C.-K. Ken Yang
		*University of California, Los Angeles and *Texas Instruments, USA*
11:45	12-4	**CMOS Frequency Generation System for W-Band Radars**
Abstract		N. Zhang and K.K. O
		Univ. of Florida, USA
12:10	12-5	**A 5GHz Phase-Locked Loop Using Dynamic Phase-Error Compensation Technique for Fast Settling in 0.18-µm CMOS**
Abstract		W.-H. Chiu, Y.-H. Huang and T.-H. Lin
		National Taiwan University, Taiwan

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(Lunch 12:35-14:20)

Wednesday, June 17,
12:45-14:05 (Separate Registration Required)

Luncheon Talk [Suzaku II]

The Series N700 and the Tokaido Shinkansen
K. Hayakawa, *Central Japan Railway Company*

Does the term “eco-business trip” sound familiar?
Tokaido Shinkansen is an extremely environmentally friendly mode of transportation and with the debut of the Series N700 this friendliness has been bettered further. As a way to deal with global warming, we are promoting “eco-business trips”: the selection of environmentally friendly mode of transport for business trips to reduce the emission of greenhouse gases.

The history of Tokaido Shinakansen rolling stock is a history of epoch-making events. The inauguration of the Tokaido Shinakansen in 1964 with the Series 0, needless to say, is the first high-speed railway in the world. With the debut of the Series 300 in 1992, we managed to adopt the bolsterless bogie and to reduce the weight of the train-set by almost 200 tons. It is with this series that we managed to increase the maximum operating speed from 220km/h to 270km/h. Then came the Series 700 in 1999, with which we managed to

better ride comfort significantly by using new vibration damping technology. And finally in July 2007 came the truly energy efficient Series N700. The first Shinkansen rolling stock equipped with the body inclining system that allows it to travel through curves without decreasing speed.

This talk will center on the aspects of the Series N700 while touching on the characteristics and history of the Tokaido Shinkansen.

*To register for the Luncheon Talk please refer to the registration form for fee information.

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Wednesday, June 17

Session 13		**DRAM and Interface [Suzaku I]**
Chairpersons		K. Kajigaya, *Elpida Memory, Inc.* M. Clinton, *Texas Instruments*
14:20	13-1	**A 31ns Random Cycle VCAT-Based $4F^2$ DRAM with Enhanced Cell Efficiency**
Abstract		K.-W. Song, J.-Y. Kim, H. Kim, H.-W. Chung, H. Kim, K. Kim, H.-W. Park, H.C. Kang, S. Kim, N.-k. Tak, D. Park, W.-S. Kim, Y.-T. Lee, Y.C. Oh, G.-Y. Jin, J. Yoo, K. Oh, C. Kim and W.-S. Lee
		Samsung Electronics Co., Korea
14:45	13-2	**A Sub-0.9V Logic-Compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-Line Write Scheme and PVT-Tracking Read Reference Bias**
Abstract		K.C. Chun, P. Jain, J.H. Lee* and C.H. Kim
		*University of Minnesota, USA and *Samsung Electronics, Korea*
15:10	13-3	**A 4.3GB/s Mobile Memory Interface With Power- Efficient Bandwidth Scaling**
Abstract		R. Palmer, J. Poulton, B. Leibowitz, Y. Frans, S. Li, A. Fuller, J. Eyles, J. Wilson, M. Aleksic, T. Greer, M. Bucher and N. Nguyen
		Rambus Inc., USA
15:35	13-4	**Wide-Range Fast-Lock Duty-Cycle Corrector with Offset-Tolerant Duty-Cycle Detection Scheme for 54nm 7Gb/s GDDR5 DRAM Interface**
Abstract		D. Shin, K.-J. Na, D. Kwon, J.-H. Kang, T. Song, H.-D. Jung, W.-Y. Lee, K.-C. Park, J.-H. Park, Y.-S. Joo, J.-H. Cha, Y. Jung, Y. Kim, D. Han, B.-J. Choi, G.-I. Lee, J.-H. Cho and Y.-J. Choi
		Hynix Semiconductor Inc., Korea

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(Break 16:00-16:15)

Wednesday, June 17

Session 14		Discrete-Time Analog [Suzaku III]
Chairpersons		K. Agawa, *Toshiba Corp.* B. Nauta, *Univ. of Twente*
14:20	14-1	**A Highly Reconfigurable 400-1700MHz Receiver Using a Down-Converting Sigma-Delta A/D with 59-dB SNR and 57-dB SFDR Over 4-MHz Bandwidth**
Abstract		R. Winoto and B. Nikolié
		University of California, Berkeley, USA
14:45	14-2	**A RF Receiver Front-End with Adaptive Discrete-Time Charge-Transfer Filter and Passive Gain- Boosting in 90nm CMOS**
Abstract		M.-C. Lee, K. Muhammad and C.-M. Hung
		Texas Instruments, USA
15:10	14-3	**A 1.28mW 100Mb/s Impulse UWB Receiver with Charge-Domain Correlator and Embedded Sliding Scheme for Data Synchronization**
Abstract		L. Liu, T. Sakurai and M. Takamiya
		The University of Tokyo, Japan
15:35	14-4	**A 73.1dB SNDR Digitally Assisted Subsampler for RF Power Amplifier Linearization Systems**
Abstract		S.W. Chung and J.L. Dawson
		Massachusetts Institute of Technology, USA

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(Break 16:00-16:15)

Wednesday, June 17

Session 15		SRAMS and Clock Circuits [Suzaku I]
Chairpersons		M. Yamaoka, *Hitachi, Ltd.* M. Whately, *Cypress Semiconductor*
16:15	15-1	**A 45nm 24MB On-Die L3 Cache for the 8-Core Multi-Threaded Xeon® Processor**
Abstract		J. Chang, S.-L. Chen, W. Chen, S. Chiu, R. Faber, R. Ganesan, M. Grgek, V. Lukka, W.W. Mar, J. Vash, S. Rusu and K. Zhang
		Intel Corporation, USA
16:40	15-2	**Clock Generation & Distribution for a 45nm, 8- Core Xeon® Processor with 24MB Cache**
Abstract		S. Tam, J. Leung and R. Limaye
		Intel Corporation, USA
17:05	15-3	**A Differential Data Aware Power-Supplied (D^2AP) 8T SRAM Cell with Expanded Write/Read Stabilities for Lower VDDmin Applications**
Abstract		M.-F. Chang*, J.-J. Wu*, K.-T. Chen* and H. Yamauchi**
		**National Tsing Hua University, Taiwan and **Fukuoka Institute of Technology, Japan*
17:30	15-4	**A 45nm 0.6V Cross-Point 8T SRAM with Negative Biased Read/Write Assist**

Abstract	M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, Y. Nakase and H. Shinohara
	Renesas Technology Corp., Japan

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Wednesday, June 17

Session 16		**DC-DC Converters [Suzaku III]**
Chairpersons		M. Nomura, *NEC Electronics Corp.* J. Lloyd, *Analog Devices*
16:15	16-1	**20mV Input Boost Converter for Thermoelectric Energy Harvesting**
Abstract		E. Carlson, K. Strunz and B. Otis
		University of Washington, USA
16:40	16-2	**Single-Inductor Dual Buck-Boost Output (SIDBBO) Converter with Adaptive Current Control Mode (ACCM) and Adaptive Body Switch (ABS) for Compact Size and Long Battery Life in Portable Devices**
Abstract		M.-H. Huang and K.-H. Chen
		National Chiao Tung University, Taiwan
17:05	16-3	**A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications**
Abstract		M. Wieckowski, G.K. Chen, M. Seok, D. Blaauw and D. Sylvester
		University of Michigan, USA
17:30	16-4	**High-Efficiency, 12V-to-1.5V DC-DC Converter Realized with Switched-Capacitor Architecture**
Abstract		V.W. Ng, M.D. Seeman and S.R. Sanders
		University of California, Berkeley, USA

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Wednesday, June 17
20:00

Rump Sessions	
R-1	**Special Evening Session: "Energy Efficiency: How is 'Green' Implemented in Reality?" [Suzaku I, II]**
Organizers	M. Takamiya, *The Univ. of Tokyo* G. Van der Plas, *IMEC*
Moderator	M. Nomura, *NEC Electronics Corp.*
Speakers	**"Doing Nothing Well"** J. Rabaey, *Univ. of California, Berkeley* **"Vibration-Driven Energy Harvesting Using High-Performance Polymer Electret"** Y. Suzuki, *The Univ. of Tokyo* **"Energy Harvesting for Green Electronics"** P. Mitcheson, *Imperial College* **"Wearable Green SoC - Beyond Portable Low Power SoC"** H.-J. Yoo, *KAIST*

In today's world, green is everywhere. Energy efficiency is a critical feature of any system.

In this session, 4 experts will give an overview of state-of-the-art techniques that are used today to implement energy efficient systems. These techniques will proliferate to more and more systems in the future.

Topics that will be covered include energy scavenging, efficient power conversion techniques and design techniques for efficient circuits and systems. Energy scavenging from the environment is the ultimate energy efficiency. These devices and their associated power converters will be discussed in detail. Sensor interface systems and efficient wireless circuits found in, for instance, body sensor systems are an excellent example of energy efficient system design and will also be covered.

Attending this session will give you a broad view on how green electronics are realized today and in the future.

R-2	**32nm SoC and Beyond - Reliable or Not? [Suzaku III]**
Organizers	M. Takamiya, *The Univ. of Tokyo* K. Chang, *Rambus Inc.*
Moderator	S. Borkar, *Intel Corp.*
Panelists	D. Scott, *TSMC* S. Yamamichi, *NEC Corp.* J. Warnock, *IBM Corp.* J. Stinson, *Intel Corp.* Y. Urakawa, *Toshiba Corp.* S. Mitra, *Stanford Univ.* *Please be informed that the Pauelists has been changed from the Advance Program.

Moore's law continues to push us to the 32nm regime for billion transistor SoCs. This causes major concerns in reliability and dependability due to increase in process variability, and design/architecture complexity. Where are the major bottlenecks for achieving high yield and low product return on 32nm SoCs? Which is more important - system architecture, circuit design, manufacturing, modeling, package design, test, or perhaps all? This panel discusses different aspects of the design world and tries to identify who should take a bigger role and assume more responsibility in solving the reliability problems of migration to 32nm and beyond.

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Monday, June 15

Joint Rump Session with Technology	
J-R	**Is TSV 3D LSI's and Packaging Finally Ready or Is It Just Another Fantasy? [Suzaku I, II]**
Organizers	M. Takamiya, *The Univ. of Tokyo* M. Clinton, *Texas Instruments, Inc* K. Schruefer, *Infineon Technologies AG* K-W. Lee, *Tohoku Univ.*
Moderator	M. Koyanagi, *Tohoku Univ.* S. Arkalgud, *SEMATECH*
Panelists	S. Borkar, *Intel Corp.* J. Knickerbocker, *IBM Corp.* L. Durodami, *Qualcomm Inc.* T. Kuroda, *Keio Univ.* C. Berry, *Amkor Technology* B. Haba, *Tessera Inc.*

3D LSI integration and packaging have been discussed for decades. Is TSV just the latest buzz-word or will it become a mainstream process? The panel will discuss which applications (memory, processor, memory+processor, imager, mixed-signal, FPGA or others) are driving the development of TSV and what types of applications could benefit from TSV in the future. The panel will debate how these applications get an advantage in the marketplace from TSV, which they cannot get from other 3D LSI integration or packaging technologies in manufacturing today.

We have assembled a distinguished panel of experts who will discuss and debate these questions and more as they explore the prospects of TSV for 3D LSI and packaging.

- Does TSV offer design, test, performance, yield, thermal / power or cost advantages over existing 3D technologies?
- What are main challenges and limitations for the acceptance in mainstream applications?
- Who will offer TSV as a design solution; IDM's, Foundries and/or OSAT's?

*This session will be held at 20:00-22:00 on Monday, June 15.

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Thursday, June 18

Session 17		Image Sensors [Suzaku I]
Chairpersons		M. Ikeda, *The Univ. of Tokyo* V. De, *Intel Corp.*
8:30	17-1	**A 0.45-0.7V Sub-Microwatt CMOS Image Sensor for Ultra-Low Power Applications**
Abstract		S. Hanson and D. Sylvester
		University of Michigan, USA
8:55	17-2	**A 0.75V CMOS Image Sensor Using Time-Based Readout Circuit**
Abstract		K. Cho, D. Lee, J. Lee and G. Han
		Yonsei University, Korea
9:20	17-3	**A Color-Independent Saturation, Linear Response, Wide Dynamic Range CMOS Image Sensor With Retinal Rod-and Cone-Like Color Pixels**
Abstract		S. Kawada*, S. Sakai*, N. Akahane*, K. Mizobuchi** and S. Sugawa*
		**Tohoku University and **Texas Instruments, Japan*
9:45	17-4	**A CMOS Image Sensor With 2.5-e^- Random Noise and 110-ke^- Full Well Capacity Using Column Source Follower Readout Circuits**
Abstract		T. Kohara*, W. Lee*, N. Akahane*, K. Mizobuchi** and S. Sugawa*
		**Tohoku University and **Texas Instruments, Japan*

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(Break 10:10-10:30)

Thursday, June 18

Session 18		Frequency Synthesizers [Suzaku II]
Chairpersons		M. Takamiya, *The Univ. of Tokyo* L. Breems, *NXP Semiconductors*
8:30	18-1	**A Compact 0.8-6GHz Fractional-N PLL with Binary-Weighted D/A Differentiator and Offset-Frequency Δ-Σ Modulator for Noise and Spurs Cancellation**
Abstract		H.-Y. Jian*,**, Z. Xu**, Y.-C. Wu** and F. Chang*
		**University of California, Los Angeles and **SST Communications, USA*
8:55	18-2	**A 320fs-RMS-Jitter and 300kHz-BW All-Digital Fractional-N PLL with Self-Corrected TDC and Fast Temperature Tacking Loop for WiMax/WLAN 11n**
Abstract		H.-H. Chang, C.-H. Fu and M. Chiu
		MediaTek Inc., Taiwan
9:20	18-3	**A Direct Digital Frequency Modulation PLL with All Digital On-Line Self-Calibration for Quad-Band GSM/GPRS Transmitter**
Abstract		C.-H. Wang, P.-Y. Wang, L.-W. Ke, D.-Y. Yu, B.-H. Ong, C.-H. Sun, H.-H. Chen, Y.-Y. Chen, C.-M. Kuo, J.-C. Lin, T.-P. Wang and Y.-H. Chen
		MediaTek Inc., Taiwan
		A Low-Voltage, 9-GHz, 0.13-µm CMOS Frequency Synthesizer With a

9:45	18-4	**Fractional Phase-Rotating and Frequency-Doubling Topology**
Abstract		C.-H. Chang and C.-Y. Yang
		National Chung Hsing University, Taiwan

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(Break 10:10-10:30)

Thursday, June 18

Session 19		**Power Management and High-Efficiency Logic [Suzaku III]**
Chairpersons		T. Shiota, *Fujitsu Laboratories Ltd.* J. Gealow, *MediaTek Wireless, Inc.*
8:30	19-1	**Multi-Phase 1GHz Voltage Doubler Charge-Pump in 32nm Logic Process**
Abstract		D. Somasekhar, B. Srinivasan, G. Pandya, F. Hamzaoglu, M. Khellah, T. Karnik and K. Zhang
		Intel Corporation, USA
8:55	19-2	**A 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler**
Abstract		T.V. Breussegem and M. Steyaert
		ESAT-MICAS, Belgium
9:20	19-3	**Dual-Power-Path RF-DC Multi-Output Power Management Unit for RFID Tags**
Abstract		J. Yi, W.-H. Ki, P. K.T. Mok and C.-Y. Tsui
		The Hong Kong University of Science and Technology, China
9:45	19-4	**A 187MHz Subthreshold-Supply Robust FIR Filter with Charge-Recovery Logic**
Abstract		W.-H. Ma*, J.C. Kao*, V.S. Sathe*,** and M. Papaefthymiou*
		**University of Michigan and **Advanced Micro Devices, USA*

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(Break 10:10-10:30)

Thursday, June 18

Session 20		**Analog Techniques [Suzaku I]**
Chairpersons		M. Nagata, *Kobe Univ.* A. Abidi, *Univ. of California, Los Angeles*
10:30	20-1	**A 28.1dBm Class-D Outphasing Power Amplifier in 45nm LP Digital CMOS**
Abstract		H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. Elmala and K. Soumyanath
		Intel Corporation, USA
10:55	20-2	**Time Difference Amplifier Using Closed-Loop Gain Control**
Abstract		T. Nakura, S. Mandai, M. Ikeda and K. Asada
		The University of Tokyo, Japan
11:20	20-3	**A Chopper and Auto-Zero Offset-Stabilized CMOS Instrumentation Amplifier**
Abstract		J.F. Witte, J.H. Huijsing and K.A.A. Makinwa

		Delft University of Technology, The Netherlands
11:45	20-4	**Complex IIP2 Improvement Through Active Cancellation of LO Leakage**
Abstract		H. Choo, K. Muhammad and M.-C. Lee
		Texas Instruments Inc., USA

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(Lunch 12:10-13:30)

Thursday, June 18

Session 21		**Advanced Equalizers [Suzaku II]**
Chairpersons		K. Nose, *NEC Corp.* K. Chang, *Rambus Inc.*
10:30	21-1	**A 19Gb/s 38mW 1-Tap Speculative DFE Receiver in 90nm CMOS**
Abstract		D.Z. Turker*, A. Rylyakov**, D. Friedman**, S. Gowda** and E. Sánchez-Sinencio*
		**Texas A&M University and **IBM T.J. Watson Research Center, USA*
10:55	21-2	**A 40Gb/s Decision Feedback Equalizer Using Back-Gate Feedback Technique**
Abstract		C.-L. Hsieh and S.-I. Liu
		National Taiwan University, Taiwan
11:20	21-3	**A Data Pattern-Tolerant Adaptive Equalizer Using Spectrum Balancing Method**
Abstract		H.-Y. Joo, K.-S. Ha and L.-S. Kim
		KAIST, Korea
11:45	21-4	**A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion**
Abstract		S. Song, B. Kim and V. Stojanović
		Massachusetts Institute of Technology, USA

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(Lunch 12:10-13:30)

Thursday, June 18

Session 22		**Clock Generation Techniques [Suzaku III]**
Chairpersons		J.-Y. Sim, *Pohang Univ.* J. Farrell, *AMD*
10:30	22-1	**A 10MHz 80µW 67 ppm/°C CMOS Reference Clock Oscillator with a Temperature Compensated Feedback Loop in 0.18µm CMOS**
Abstract		J. Lee and S.H. Cho
		KAIST, Korea
10:55	22-2	**A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply**
Abstract		K. Okada, Y. Nomiyama, R. Murakami and A. Matsuzawa
		Tokyo Institute of Technology, Japan
11:20	22-3	**A 132.7-to-143.5GHz Injection-Locked Frequency Divider in 65nm CMOS**
		B.-Y. Lin and S.-I. Liu

Abstract		*National Taiwan University, Taiwan*
11:45	22-4	**A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13µm CMOS Technology**
Abstract		J. Yu, F.F. Dai and R.C. Jaeger
		Auburn University, USA

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(Lunch 12:10-13:30)

Thursday, June 18

Session 23		**Low Power ADCs [Suzaku I]**
Chairpersons		A. Wada, *SANYO Semiconductor Co., Ltd.* G. Van der Plas, *IMEC*
13:30	23-1	**A 0.92mW 10-Bit 50-MS/s SAR ADC in 0.13µm CMOS Process**
Abstract		C.-C. Liu, S.-J. Chang, G.-Y. Huang and Y.-Z. Lin
		National Cheng Kung University, Taiwan
13:55	23-2	**A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS**
Abstract		P. Nuzzo*,**, C. Nani*,***, C. Armiento*,****, A. Sangiovanni-Vincentelli**, J. Craninckx* and G.V. der Plas*
		**IMEC, Belgium, **University of California at Berkeley, USA, ***NXP, The Netherlands and ****University of Pisa, Italy*
14:20	23-3	**A 12b 11MS/s Successive Approximation ADC with Two Comparators in 0.13µm CMOS**
Abstract		J.J. Kang*,** and M.P. Flynn*
		**University of Michigan and **Marvell Technology Group, USA*
14:45	23-4	**A 1.3µW 0.6V 8.7-ENOB Successive Approximation ADC in a 0.18µm CMOS**
Abstract		S.-K. Lee, S.-J. Park, Y. Suh, H.-J. Park and J.-Y. Sim
		Pohang University of Science and Technology (POSTECH), Korea

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(Break 15:10-15:25)

Thursday, June 18

Session 24		**MM-Wave Techniques [Suzaku II]**
Chairpersons		J. Lee, *National Taiwan Univ.* C.-M. Hung, *Texas Instruments, Inc*
13:30	24-1	**A 77 GHz 90 nm CMOS Transceiver for FMCW Radar Applications**
Abstract		T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe and I. Seto
		Toshiba Corporation, Japan
13:55	24-2	**60-GHz Hybrid Transmit/Receive Switch Using p-n Diode and MOS Transistors**
Abstract		C. Mao and K.K. O
		University of Florida, USA
14:20	24-3	**60GHz RF-Path Phase-Shifting Two-Element Phased-Array Front-End in Silicon**

Abstract		A. Natarajan*, M.-D. Tsai** and B. Floyd*
		*IBM T. J. Watson Research Center, USA and **MediaTek Inc., Taiwan*
14:45	24-4	**36mW 63GHz CMOS Differential Low-Noise Amplifier with 14GHz Bandwidth**
Abstract		Y. Natsukari and M. Fujishima
		The University of Tokyo, Japan

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(Break 15:10-15:25)

Thursday, June 18

Session 25		**Media Processor Architecture [Suzaku III]**
Chairpersons		M. Igarashi, *Sony Corp.* S. Tam, *Intel Corp.*
13:30	25-1	**3D System Integration of Processor and Multi- Stacked SRAMs by Using Inductive-Coupling Links**
Abstract		K. Osada*, M. Saen*, Y. Okuma*, K. Niitsu**, Y. Shimazaki**,***, Y. Sugimori**, Y. Kohama**, K. Kasuga**, I. Nonomura***, N. Irie*, T. Hattori***, A. Hasegawa*** and T. Kuroda**
		*Hitachi, Ltd.,**Keio University and ***Renesas Technology Corp., Japan*
13:55	25-2	**A 116fps 74mW Mobile Heterogeneous 3D-Media Processor for 3D Display Contents**
Abstract		S.-H. Kim*, H.-Y. Kim*, Y.-J. Kim*, K. Chung*, D. Kim** and L.-S. Kim*
		*KAIST, Korea and **Qualcomm Inc., USA*
14:20	25-3	**A 22.8GOPS 2.83mW Neuro-Fuzzy Object Detection Engine for Fast Multi-Object Recognition**
Abstract		M. Kim, J.-Y. Kim, S. Lee, J. Oh and H.-J. Yoo
		KAIST, Korea
14:45	25-4	**A 1080p@60fps Multi-Standard Video Decoder Chip Designed for Power and Cost Efficiency in a System Perspective**
Abstract		D. Zhou*, Z. You**, J. Zhu**, J. Kong**, Y. Hong**, X. Chen**, X. He**, C. Xu**, H. Zhang**, J. Zhou*, N. Deng**, P. Liu** and S. Goto*
		*Waseda University, Japan and **Shanghai Jiao Tong University, China*

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(Break 15:10-15:25)

Thursday, June 18

Session 26		**High-Speed ADCs [Suzaku I]**
Chairpersons		M. Ito, *Renesas Technology Corp.* J. Savoj, *Qualcomm Inc*
15:25	26-1	**A Self-Background Calibrated 6b 2.7GS/s ADC with Cascade-Calibrated Folding-Interpolating Architecture**
Abstract		Y. Nakajima*, A. Sakaguchi*, T. Ohkido**, T. Matsumoto* and M. Yotsuyanagi*
		*NEC Electronics Corporation and **NEC Micro Systems, Japan*
15:50	26-2	**A 7.5-GS/s 3.8-ENOB 52-mW Flash ADC with Clock Duty Cycle Control in 65nm CMOS**
		H. Chung*, A. Rylyakov**, Z.T. Deniz**, J. Bulzacchelli**, G.-Y. Wei* and D.

Abstract		Friedman**
		*Harvard University and **IBM T.J. Watson Research Center, USA*
16:15	26-3	**A 1.5-GHz 63dB SNR 20mW Direct RF Sampling Bandpass VCO-Based ADC in 65nm CMOS**
Abstract		Y.-G. Yoon and S.H. Cho
		KAIST, Korea
16:40	26-4	**A Dual-Channel 10b 80MS/s Pipeline ADC with 0.16mm^2 Area in 65nm CMOS**
Abstract		X. Yu, F. Lin, K. Li, S. Ranganathan and T. Kwan
		Broadcom Corporation, USA

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Thursday, June 18

Session 27		**Wireless Transceivers [Suzaku II]**
Chairpersons		H. Ishikuro, *Keio Univ.* B. Nikolic, *Univ. of California, Berkeley*
15:25	27-1	**528mW Zero-IF Full-Segment ISDB-T CMOS Tuner with 10th-Order Channel Filters**
Abstract		T. Kamata*,**, K. Okui*, M. Fukasawa*, K. Tanaka*, C. Go*, N. Motoyama*, T. Matsuoka** and K. Taniguchi**
		*RfStream Corporation and **Osaka University, Japan*
15:50	27-2	**A 2×V_{DD}-Enabled TV-Tuner RF Front-End Supporting TV-GSM Interoperation in 90nm CMOS**
Abstract		P.-I. Mak* and R.P. Martins**
		*University of Macau, China and **On leave from Instituto Superior Técnico (IST), Portugal*
16:15	27-3	**A Frequency Translation Technique for SAW-Less 3G Receivers**
Abstract		A. Mirzaei, X. Chen, A. Yazdi, J. Chiu, J. Leete and H. Darabi
		Broadcom Corporation, USA
16:40	27-4	**A 4-Stream 802.11n Baseband Transceiver in 0.13 µm CMOS**
Abstract		A. Burg*,**, S. Haene*,**, M. Borgmann**, D. Baum**, T. Thaler**, F. Carbognani**, S. Zwicky**, L. Barbero**, C. Senning*, P. Greisen*,**, T. Peter*, C. Foelmli**, U. Schuster**, P. Tejera** and A. Staudacher
		*ETH Zurich and **Celestrius AG, Switzerland*

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Thursday, June 18

Session 28		**Signal Processing [Suzaku III]**
Chairpersons		M. Hariyama, *Tohoku Univ.* K. Shepard, *Columbia Univ.*
15:25	28-1	**A 47 Gb/s LDPC Decoder with Improved Low Error Rate Performance**
Abstract		Z. Zhang, V. Anantharam, M.J. Wainwright and B. Nikoli´c
		University of California, Berkeley, USA
15:50	28-2	**A 188-size 2.1mm^2 Reconfigurable Turbo Decoder Chip with Parallel Architecture for 3GPP LTE System**

Abstract		C.-C. Wong, Y.-Y. Lee and H.-C. Chang
		National Chiao Tung University, Taiwan
16:15	28-3	**A 58-µW Single-Chip Sensor Node Processor Using Synchronous MAC Protocol**
Abstract		T. Takeuchi, S. Izumi, T. Matsuda, H. Lee, Y. Otake, T. Konishi, K. Tsuruda, Y. Sakai, H. Fujiwara, C. Ohta, H. Kawaguchi and M. Yoshimoto
		Kobe University, Japan
16:40	28-4	**A 200Mbps+ 2.14nJ/b Digital Baseband Multi Processor System-on-Chip for SDRs**
Abstract		V. Derudder, B. Bougard, A. Couvreur, A. Dewilde, S. Dupont, L. Folens, L. Hollevoet, F. Naessens, D. Novo, P. Raghavan, T. Schuster, K. Stinkens, J.-W. Weijers and L. Van der Perre
		IMEC, Belgium

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