Analysis of Nonideal Behaviors Based on INL/DNL Plots for SAR ADCs

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***Abstract*— This paper presents a comprehensive investigation of several important error sources for the successive-approximation register (SAR) analog-to-digital converters (ADCs). The error sources that we discuss in this paper include the dynamic comparator offset, the dynamic gain error of digital-to-analog converter (DAC), the capacitor mismatch of capacitive DAC, the incomplete settling of DAC, the undershoot of reference voltage, and the input signal coupling. The integral/differential nonlinearities (INL/DNL) of SAR ADCs that are resulted from these error sources are analyzed and addressed. A diagnostic procedure is presented to identify the possible error sources based on the INL/DNL plots. In addition, design suggestions for overcoming these problems are also offered and recommended in this paper.**

***Index Terms*— Failure mode diagnosis, successive approximation register (SAR) analog-to-digital converter (ADC).**

I. Introduction

THE analog-to-digital converter (ADC) is a key component in modern electronic devices and systems. It is the bridge between the analog and the digital domains. The successive-approximation register (SAR) ADC takes the advantages of technological progress and it could possibly be a very acceptable candidate for most analog-to-digital applications to obtain power- and area-efficiencies, achieve medium-to-high speed, and work under a low voltage supply. These characteristics enable the SAR ADCs to achieve several tens of kilosamples per second to a low gigasample per second sampling rate, with 5- to 12-b resolutions and make it feasible to be an alternative for expensive pipelined ADCs [1].

As shown in Fig. 1, a typical SAR ADC consists of a comparator, a digital-to-analog converter (DAC), a sample-and-hold circuit, and a SAR control logic circuit. The errors in these blocks unavoidably affect the performance of the SAR ADC. Some methods have been proposed to test the linearity of SAR ADCs [2]–[5]. Circuit designers can adopt these methods to evaluate the linearity of their designs in a low-cost manner. In addition, to test the ADC, how to identify the potential error sources based on the test results is also an important issue for designers and test engineers. In this paper, a comprehensive cause–effect analysis was presented for various main error sources, including the dynamic offset in the comparator, the dynamic gain error of DAC, the capacitor mismatch of DAC, the incomplete settling of DAC, the undershoot of reference voltage, and the input signal coupling. We explicitly address the effects of these nonidealities on the SAR ADC performance and verify them through the simulation and/or measurement results. Design suggestions for alleviating these nonideal effects are also offered and recommended in this paper. Using the achievements accomplished in this paper, circuit designers can collect information about the linearity degradation to predict which error source is the critical one that is needed to be resolved first. Circuit designers can gradually improve their circuits in the simulation stage by considering the dominant error.

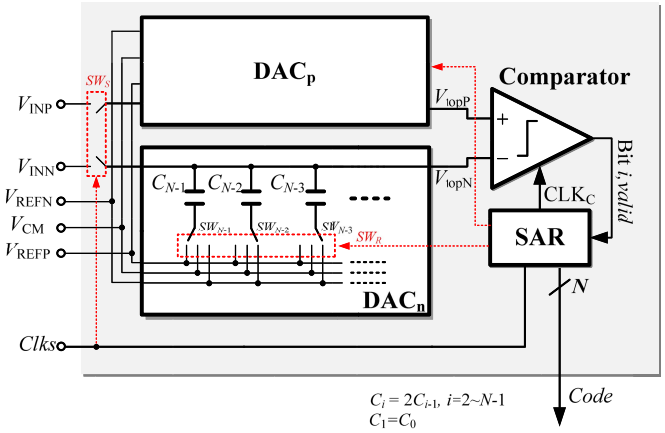

Fig. 1. Building blocks of a typical N-b SAR ADC.

The rest of this paper is organized as follows. Sections II and III discuss various error sources in the comparator and DAC, including their causes, syndromes, and solutions. Section IV shows the simulation and measurement results that verify the effects of the analyzed critical errors. Finally, conclusions are given in Section V.

II. Error Sources in Comparator

A. Static Offset

Generally, an N-bit SAR ADC performs N comparisons to obtain the converted bits. Therefore, a low-power and high-performance comparator plays an important role to enhance the overall ADC performance. Noise and offset are the most crucial errors associated with the comparator. For considering the ADC linearity, the main error source of the comparator is the dynamic offset that is sourced from the asymmetry of the

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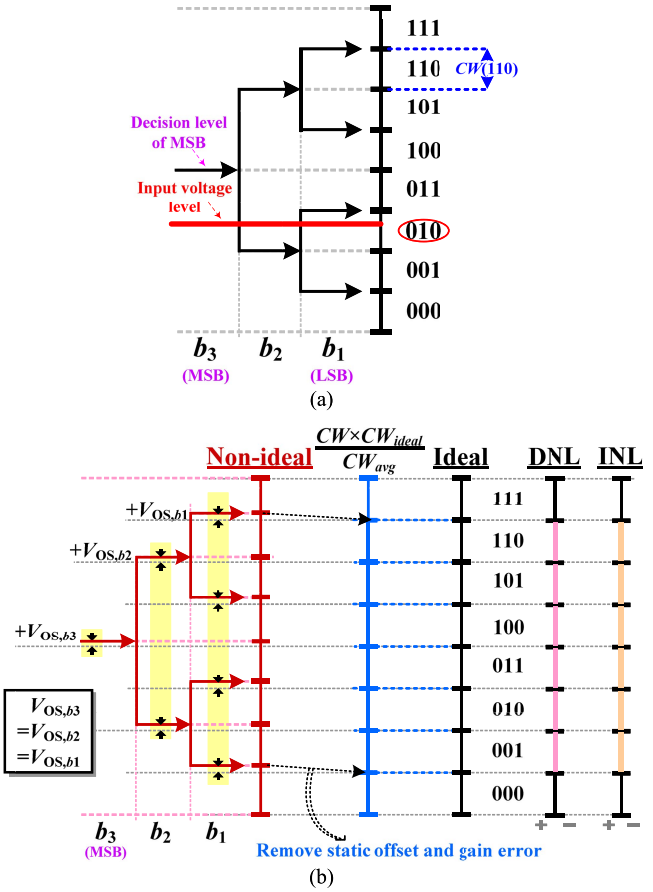

Fig. 2. Binary search procedure of a 3-b SAR ADC. (a) Ideal search procedure. (b) Search procedure with the static offset in the comparator.

component and the offset could be formulated as

$$V_{\mathrm{OS}} = \Delta V_{\mathrm{TH}} + \frac{(V_{\mathrm{GS}} - V_{\mathrm{TH}})}{2} \times \left(\frac{\Delta S}{S} + \frac{\Delta R}{R}\right) \tag{1}$$

where ΔV_{TH} is the threshold voltage offset of the differential input pair, S and ΔS are the physical dimension and its mismatch of input pair, and R and ΔR are the loading resistance and its mismatch [6]. The ΔV_{TH} is a static offset that does not affect the linearity. For example, in a 3-b SAR ADC ($N = 3$), the ideal binary search procedure from the most significant bit (MSB) to the least significant bit (LSB) is shown in Fig. 2(a). The code width for a particular code B is denoted as $\mathrm{CW}(B)$. The quantization result of the input voltage level is represented by an N-bit binary code, i.e., $B = b_N b_{N-1} \ldots b_2 b_1$. While the practical search procedure with the static offset, which is denoted by $V_{\mathrm{OS},bi}$ in the bit i, is shown in Fig. 2(b). The ideal, practical, and averaged code widths are denoted as $\mathrm{CW}_{\mathrm{ideal}}$, CW, and $\mathrm{CW}_{\mathrm{avg}}$, respectively. The static offset error and gain error should be removed before calculating the differential nonlinearity (DNL) and the integral nonlinearity (INL) since they do not influence the linearity. Therefore, Fig. 2(b) shows that the linearity of ADC is maintained if the offset is a constant, i.e., $V_{\mathrm{OS},b1} = V_{\mathrm{OS},b2} = V_{\mathrm{OS},b3}$.

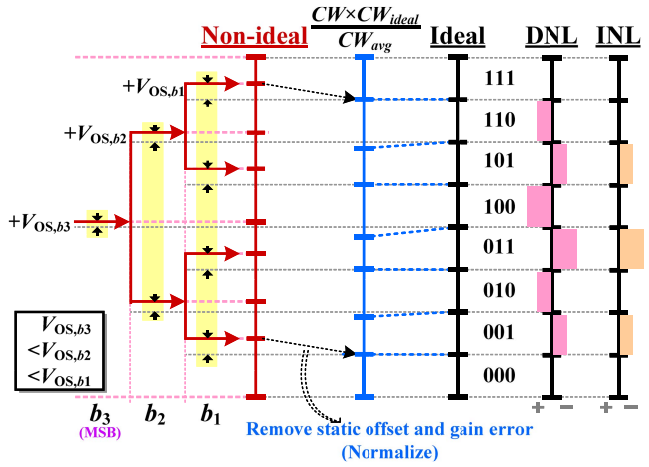

Fig. 3. Decision levels of a 3-b SAR ADC with a dynamic offset voltage in the comparator.

B. Dynamic Offset

In fact, the second term in (1) is a signal-dependent dynamic offset and it varies with the common-mode voltage of the compared voltage [7]. As shown in Fig. 3, the decision levels of bit i are shifted by unequal offset $V_{\mathrm{OS},bi}$, and the width of code B, i.e., $\mathrm{CW}(B)$, is extended or shrunk. Hence, the nonlinearity is unavoidably induced, even removing the static offset and gain error.

To formulate the nonlinearity induced by the dynamic offset, we should first obtain the code width for the code B, i.e., $\mathrm{CW}(B)$. The code width $\mathrm{CW}(B)$ is determined by two decision levels for its upper and lower bounds. The decision level of the LSB will be the upper/lower bound of $\mathrm{CW}(B)$. For example, in the case that code B is an odd, i.e., the least bit is in logic one, the input signal is certainly higher than a threshold level, which is regarded as the lower bound of $\mathrm{CW}(B)$. In contrast, if code B is an even, i.e., the least bit is in logic zero, the input signal is certainly lower than a threshold level, which is regarded as the upper bound of $\mathrm{CW}(B)$.

From Fig. 3 we can find that the other bound can be obtained from the decision level of the first changing bit from the LSB to the MSB, which is denoted by b_x. For an N-bit SAR ADC, bit b_x must satisfy the constraints

$$\begin{cases} B = b_N \ldots b_{x+1} b_x b_{x-1} \ldots b_2 b_1 \\ b_{x-1} = \cdots = b_2 = b_1 \\ b_x \neq b_{x-1}. \end{cases} \tag{2}$$

For example, in $B = 10\,100$, the decision level of b_1 is its upper bound and the other bound, i.e., the lower bound, is the decision level of b_3 according to the constraints in (2). After obtaining the upper and lower bounds, the variation of $\mathrm{CW}(B)$, which is denoted by $\Delta\mathrm{CW}(B)$, is equal to the difference between the upper and the lower bound offsets. That is to say, $\Delta\mathrm{CW}(B) = V_{\mathrm{OS},b1} - V_{\mathrm{OS},bx}$ when B is an even number ($b_1 = 0$) and $\Delta\mathrm{CW}(B) = V_{\mathrm{OS},bx} - V_{\mathrm{OS},b1}$ when B is an odd number ($b_1 = 1$). Then, $\mathrm{CW}(B)$ in a binary-weighted SAR ADC can be calculated as

$$\begin{aligned} \mathrm{CW}(B) &= V_{\mathrm{LSB}} + \Delta\mathrm{CW}(B) \\ &= V_{\mathrm{LSB}} + (-1)^{b_1} \times (V_{\mathrm{OS},b1} - V_{\mathrm{OS},bx}) \end{aligned} \tag{3}$$

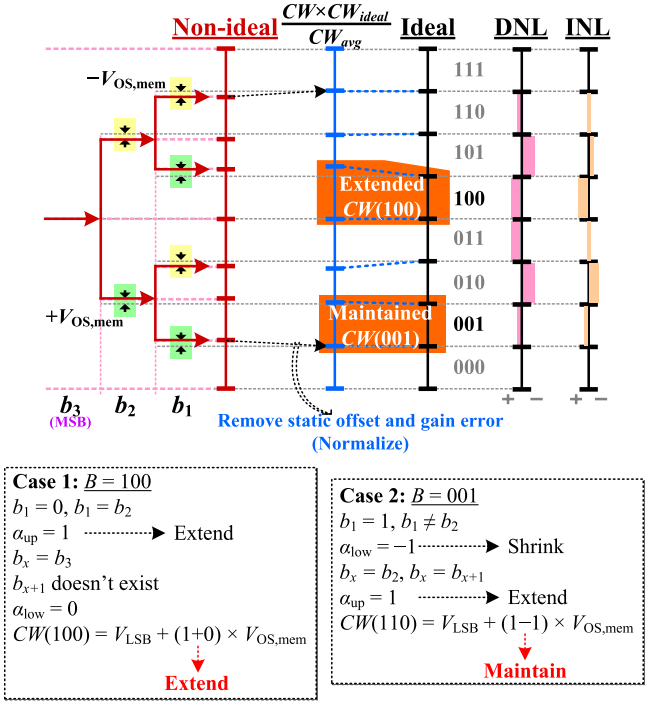

Fig. 4. Decision levels of a 3-b SAR ADC with a dynamic offset voltage due to the memory effect in the comparator.

where V_{LSB} is the ideal voltage range of the LSB. It is worth to note that code B is a missing code if CW(B) is negative. To remove the static offset error and gain error, the average code width is obtained first in (4) and then the DNL and INL can be calculated as

$$\mathrm{CW}_{\mathrm{avg}} = \frac{\sum_{B=1}^{2^N-2} \mathrm{CW}(B)}{2^N - 2} \tag{4}$$

$$\begin{cases} \mathrm{DNL}(B) = \dfrac{\mathrm{CW}(B) - \mathrm{CW}_{\mathrm{avg}}}{\mathrm{CW}_{\mathrm{avg}}}, & B = 1 \text{ to } 2^N - 2 \\ \mathrm{DNL}(0) = \mathrm{DNL}(2^N - 1) = 0 \end{cases} \tag{5}$$

$$\begin{cases} \mathrm{INL}(B) = \mathrm{INL}(B-1) + \mathrm{DNL}(B), & B = 1 \text{ to } 2^N - 2 \\ \mathrm{INL}(0) = \mathrm{INL}(2^N - 1) = 0. \end{cases} \tag{6}$$

For the example shown in Fig. 3, assume that the dynamic offset $V_{OS,bi}$ is increased monotonically (i.e., $V_{OS,b3} < V_{OS,b2} < V_{OS,b1}$) during the switching procedure [7], then the widest or the narrowest code width will locate at $B = 2^{N-1}$ or $B = 2^{N-1} - 1$ according to (3).

Besides, the memory effect of the comparator is another source of the dynamic offset. The memory effect occurs when the comparator does not completely reset to the initial condition before the next comparison. If the compared voltage difference ($V_{topP} - V_{topN}$ in Fig. 1) is not sufficiently large for converting bit b_i, the comparison result of b_i may still be the same as that of b_{i+1}. The incorrect comparison results induce a dynamic offset and degrade the ADC linearity. Fig. 4 shows an example of the SAR ADC that has a memory effect. It shows that the decision level of b_i has an offset of $V_{OS,mem}$ toward the decision level of b_{i+1}. As mentioned above, CW(B) is determined by its upper and lower bounds, which are the decision levels of b_1 and b_x. When considering the memory effect, if $b_1 = b_2$ or $b_x = b_{x+1}$, the decision level shift of b_1 or b_x will extend CW(B). In contrast, CW(B) will be shrunk if $b_1 \neq b_2$ or $b_x \neq b_{x+1}$. Besides, if b_{x+1} does not exist (for the example that b_x is the MSB), there is no memory effect for the MSB bit and the corresponding decision level is not shifted. In conclusion, CW(B) can be formulated as (7), where α_{low}/α_{up} is the sign parameter of the upper/lower bound offset; Fig. 5 shows the entire procedure to obtain α_{low} and α_{up}

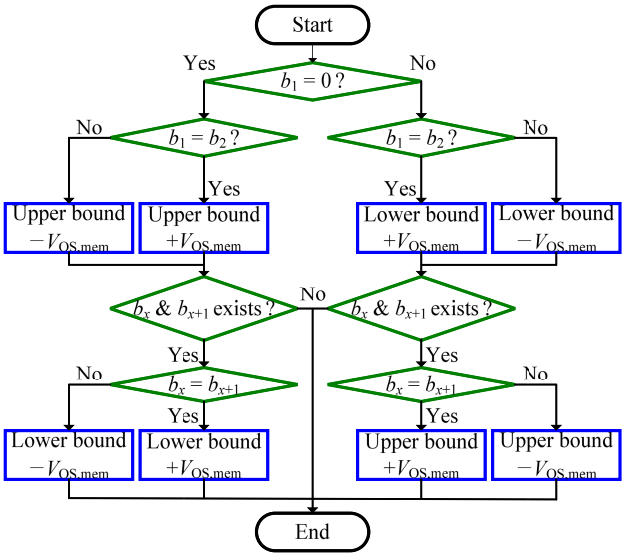

Fig. 5. Procedure to obtain the decision-level shifting due to the memory effect in the comparator.

$$\begin{aligned} \mathrm{CW}(B) &= V_{\mathrm{LSB}} + (\alpha_{\mathrm{low}} + \alpha_{\mathrm{up}}) \times V_{\mathrm{OS,mem}} \\ &= V_{\mathrm{LSB}} + [(-1)^{b_1 \oplus b_2} + (-1)^{b_x \oplus b_{x+1}}] \times V_{\mathrm{OS,mem}}. \end{aligned} \tag{7}$$

Finally, its average code width, DNL, and INL can be again calculated, respectively, from (4), (5), and (6).

There are some circuit techniques to reduce the dynamic offset. Reducing the mismatches of physical dimension and loading is an intuitive way according to (1). This can be achieved by simply enlarging the transistor size of the comparator. Another way is to reduce the variation range of the overdrive voltage, i.e., ($V_{GS}-V_{TH}$) in (1). It could be reduced by cascading a biased current source in the comparator [7] or using a DAC switching scheme (such as switchback switching procedure [8]) with the narrower variation range of the common-mode voltage. Moreover, the input referred offset voltage that is induced from the comparators can also be reduced by adding a preamplifier [9]. Calibration for offset reduction is also an interesting and important research topic [10], [11]. Additionally, if the dynamic offset is induced by the memory effect, it could be diminished by enhancing the comparator reset, such as adding reset switches or the equalizer between the internal symmetrical nodes.

III. Error Source in DAC

The DAC of SAR ADC provides the necessary voltage levels for comparison to realize the search

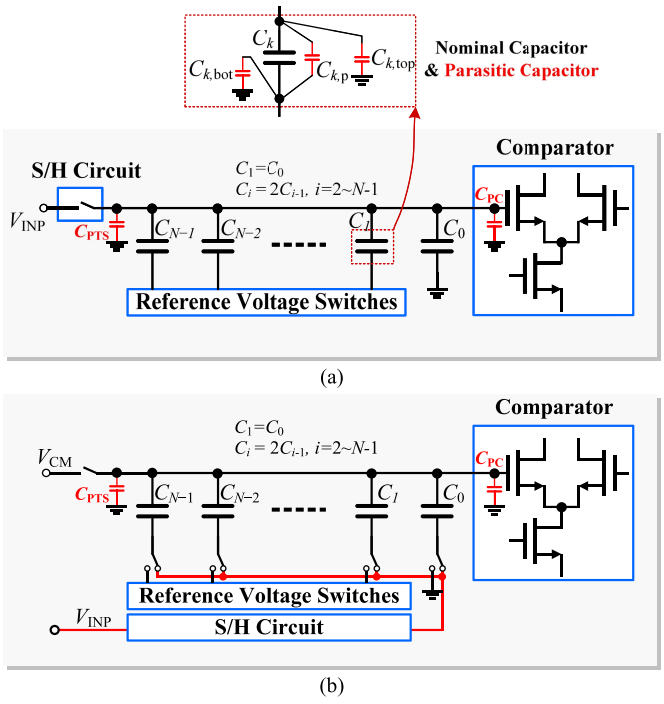

Fig. 6. Illustrations of parasitic capacitors for (a) top-plate sampling and (b) bottom-plate sampling SAR ADCs.

algorithms [7], [8], [12], [13]. Its major error sources are from the reference voltage and the passive devices. In recent years, the capacitive DAC is widely used as it does not consume static power and the precision of on-chip capacitors is sufficient for high-resolution ADCs. However, parasitic capacitors may degrade the performance. The parasitic capacitors of a nominal capacitor C_k can be roughly divided into three types as shown in Fig. 6(a). The first is the parasitic capacitor ($C_{k,p}$) between the top plate and the bottom plate due to the cross-coupled routing path. The second is the parasitic of the top plate to the ground ($C_{k,\text{top}}$). The third is the parasitic of the bottom plate to the ground ($C_{k,\text{bot}}$). They have different influences on the performance of the SAR ADC and should be analyzed individually.

A. Static Gain Error and Dynamic Gain Error

Gain error is a common error especially in the top-plate sampling SAR ADCs, i.e., ADC_{top}. The input signal (V_{INP}) is sampled on the top plate of the capacitor and the reference voltages (V_{REF}) are applied to the bottom plate of the capacitor. In contrast, both the input and reference voltages are sampled and applied to the bottom plate of the capacitor for the bottom-plate sampling SAR ADCs, i.e., ADC_{bot}. Fig. 6 shows the SAR ADCs with the top-plate sampling [7] and the bottom-plate sampling [13], respectively.

Before we introduce the gain error of DAC, some parasitic capacitors and the operation of ADC_{top} and ADC_{bot} should be described first [7], [13]. Let C_{PC} denote the parasitic capacitor of the comparator input pair, C_{PTS} denote the parasitic of switch that connects to the top plate, and $C_{P,\text{TOP}}$ denote the total parasitic of the top plate

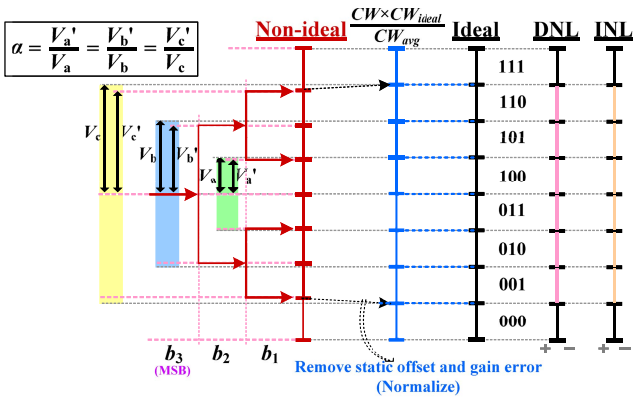

Fig. 7. Decision levels of a 3-b SAR ADC with a static gain error.

($C_{P,\text{TOP}} = C_{\text{PC}} + C_{\text{PTS}} + \Sigma C_{k,\text{top}}$). For simplifying the analysis, the capacitor bottom plates of $\text{ADC}_{\text{top}}/\text{ADC}_{\text{bot}}$ are all assumed to be reset to $V_{\text{ref}}/V_{\text{CM}}$ before the MSB conversion. After the conversion for a particular bit b_k is completed, assume the bottom plate of C_k connects to the ground if $b_k = 1$ and to V_{ref} if $b_k = 0$. Then, the residue voltage on the top plate of ADC_{top}, i.e., $V_{\text{DAC,TOP}}(V_{\text{INP}})$, and the voltage on the bottom plate of ADC_{bot}, i.e., $V_{\text{DAC,BOT}}(V_{\text{INP}})$, can be, respectively, formulated as (8) and (9) by charge conservation. (see Appendix I for the detailed derivative process)

$$V_{\text{DAC,TOP}}(V_{\text{INP}}) = V_{\text{INP}} - \frac{V_{\text{ref}}}{C_{\text{Total}}} \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) \quad (8)$$

where

$$C_{\text{Total}} = C_{P,\text{TOP}} + \sum_{k=0}^{N-1} (C'_k), C'_k = C_k + C_{k,p}$$

$$V_{\text{DAC,BOT}}(V_{\text{INP}}) = V_{\text{CM}} + \sum_{k=1}^{N-1} \left[\left(\frac{C'_k}{C_{\text{Total}}} \right) \times (b_{k+1} V_{\text{ref}} - V_{\text{INP}}) \right] + \frac{C'_0}{C_{\text{Total}}} \times (V_{\text{CM}} - V_{\text{INP}}). \quad (9)$$

Both (8) and (9) show that the reference voltage V_{ref} of ADC_{bot} and ADC_{top} are shrunk after charge redistribution with parasitic capacitors because of $C_{\text{Total}} > \Sigma C'_k$. The main difference between the two structures ADC_{bot} and ADC_{top} is that the input signal and the reference voltage of ADC_{top} are scaled with different factors while those of ADC_{bot} are scaled with the same ratio. However, the linearity is not affected by this static gain error as shown in Fig. 7.

In fact, C_{PC} and C_{PTS} in Fig. 6 are voltage-dependent capacitors as discussed in [8], so (8) and (9) should be, respectively, modified to

$$V_{\text{DAC,TOP}}(V_{\text{INP}}) = \frac{V_{\text{INP}} \times C_{\text{Total}}(V_{\text{INP}})}{C_{\text{Total}}(V_{\text{DAC,TOP}})} - \frac{V_{\text{ref}}}{C_{\text{Total}}(V_{\text{DAC,TOP}})} \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) \quad (10)$$

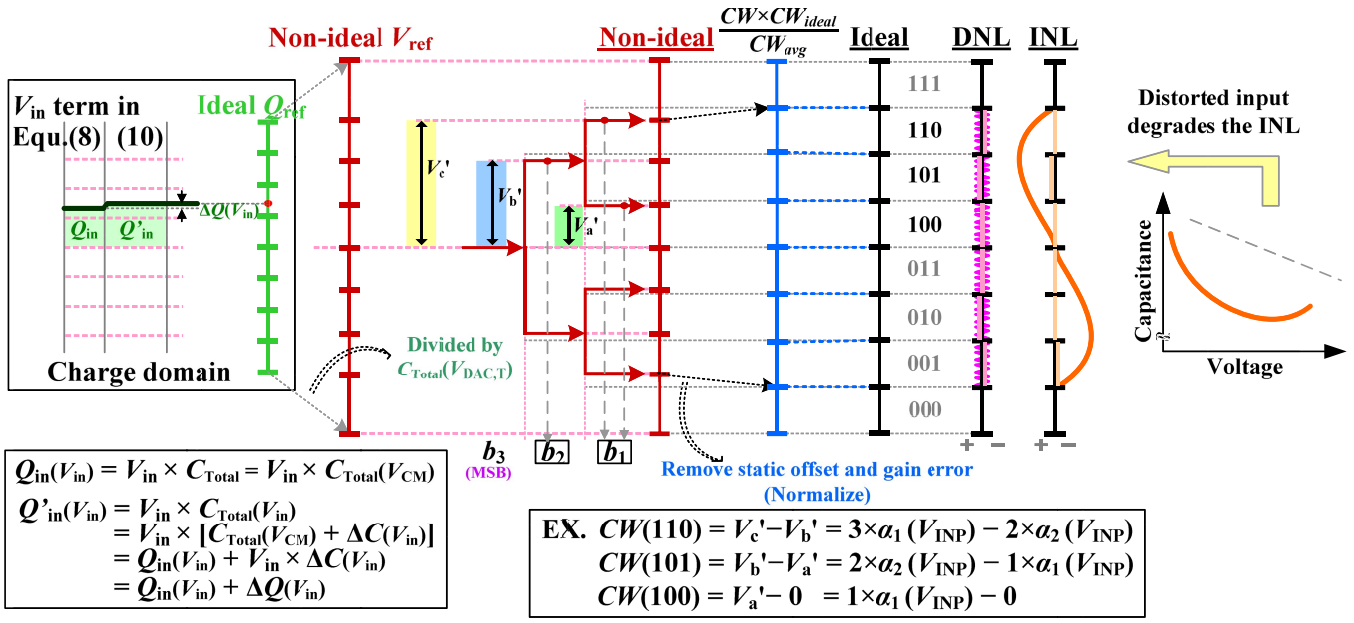

Fig. 8. Decision levels of a 3-bit SAR ADC with a dynamic gain error.

where

$$C_{\text{Total}}(V) = C_{P,\text{TOP}}(V) + \sum_{k=0}^{N-1}(C'_k),\ C'_k = C_k + C_{k,p}$$

$$V_{\text{DAC,BOT}}(V_{\text{INP}}) = \frac{V_{\text{CM}} \times C_{\text{Total}}(V_{\text{CM}})}{C_{\text{Total}}(V_{\text{DAC,BOT}})} + \sum_{k=1}^{N-1}\left[\left(\frac{C'_k}{C_{\text{Total}}(V_{\text{DAC,BOT}})}\right) \times (b_{k+1}V_{\text{ref}} - V_{\text{INP}})\right] + \frac{C'_0}{C_{\text{Total}}(V_{\text{DAC,BOT}})} \times (V_{\text{CM}} - V_{\text{INP}}). \quad (11)$$

Equation (10) can be demonstrated as shown in Fig. 8. The charge provided by the input signal V_{INP} is $Q_{\text{in}}(V_{\text{INP}}) = V_{\text{INP}}C_{\text{Total}}$ if the parasitic capacitance is independent of the voltage as expressed in (8). In contrast, the charge $Q_{\text{in}}(V_{\text{INP}})$ will be distorted by $C_{\text{Total}}(V_{\text{INP}})$ if the voltage-dependent capacitor $C_{\text{Total}}(V)$ is taken into consideration as expressed in (10). The INL will be affected by the distortion and the changed voltage-dependent charge is denoted by $Q'_{\text{in}}(V_{\text{INP}})$. Then, to transfer the charge domain to the voltage domain for comparison, both $Q'_{\text{in}}(V_{\text{INP}})$ and Q_{ref} are redistributed on a nonconstant $C_{\text{Total}}(V_{\text{DAC,TOP}})$ and it leads to a nonconstant LSB voltage (V_{LSB}). For a nonconstant V_{LSB}, the static voltage offset of the comparator becomes a dynamic one, and further degrades the ADC linearity. Fig. 8 shows that the nonlinearity induced by $C_{\text{Total}}(V_{\text{DAC,TOP}})$ is not significant (bright lines in DNL/INL plots). In contrast, the nonlinearity induced by $C_{\text{Total}}(V_{\text{INP}})$ is more obvious (dark lines in DNL/INL plots). Comparing (11) with (10), $C_{\text{Total}}(V_{\text{CM}})$ is a constant that has no effect on the ADC linearity. Besides, nonconstant $C_{\text{Total}}(V_{\text{DAC,BOT}})$ also induces a dynamic V_{LSB} that may degrade the ADC linearity.

To obtain the code width from (10) and (11), the equations should be in a closed-loop form. It is not easy to calculate the precise results without understanding the relationship between the voltage and the capacitance. To simplify the equation, we assume that the gain error for converting the bit b_i is $\alpha_i(V_{\text{INP}})$. There are three examples we show in Fig. 8 and we can formulate CW(B) as follows (see Appendix II):

$$\text{CW}(B) = (-1)^{b_1 \oplus b_N} \times \left\{ \begin{matrix} \alpha_x(V_{\text{INP}}) \times [\beta + 1 - (b_1 \oplus b_N)] \\ -\alpha_1(V_{\text{INP}}) \times [\beta + (b_1 \oplus b_N)] \end{matrix} \right\} \times V_{\text{LSB}}$$

where

$$\beta = \sum_{i=1}^{N-1}(b_i \oplus \bar{b}_N) \times 2^{i-1} \quad (12)$$

α_1 and α_x are, respectively, the gain parameters for LSB and bit x, where x is the same as defined in (2). According to (10) and (11), α_i should be a function of V_{INP}, i.e., $\alpha_i(V_{\text{INP}})$.

It has to be noted that if x is equal to N (i.e., $B = 2^{N-1}$ or $2^{N-1} - 1$), then α_x is equal to 1. There is no gain error in b_N. because the MSB bit is obtained without DAC switching. Again, the evaluated average code width is first obtained in (4), and then the evaluated average code width is substituted into (5) and (6) to obtain the DNL and INL values, respectively. Nonlinear $C_{\text{Total}}(V_{\text{INP}})$ in (10) distorts the input signal and unavoidably results in an INL error. Besides, the DNL error is small because $C_{\text{Total}}(V_{\text{INP}})$ is generally a continuous function of the voltage.

The unit capacitor in the DAC array is often enlarged to compensate the gain error induced by the voltage-dependent parasitic capacitor, however, the limited input bandwidth of SAR ADC is the penalty. Bottom-plate sampling method [13] and narrower input range are alternatively utilized to avoid the degradation of the bandwidth [8].

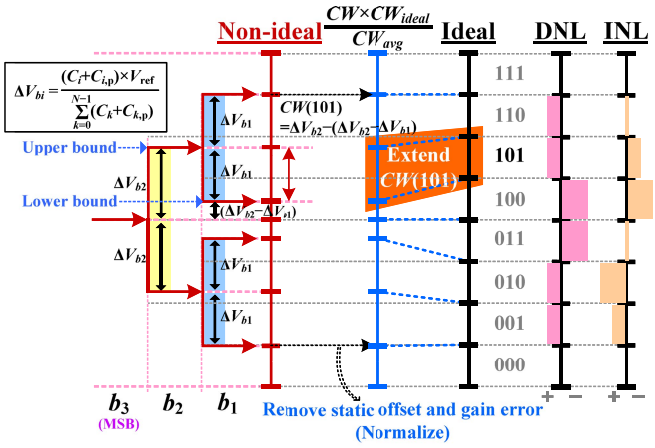

Fig. 9. Decision levels of a 3-b SAR ADC with a capacitor mismatch.

B. Capacitor Mismatch

In general, capacitor mismatch can result from a random mismatch and a systematic one [14], [15]. Random mismatch is usually induced by the process variation, while a systematic mismatch is usually generated from the irregular layout and processing gradients. Capacitor mismatch changes the bit-weighting and further shifting the decision level, as shown in Fig. 9. The decision level shifting is symmetrical to its decision branch.

To focus on this issue, parasitic capacitors C_{PC}, C_{PTS}, and $C_{k,\mathrm{top}}$ which are considered in (8) and (9) are removed in this section. After removing these parasitic capacitors, the voltage change after switching capacitor C_i is ΔV_{bi} as shown in Fig. 9, and the code width $\mathrm{CW}(B)$ of $\mathrm{ADC_{top}}$ and $\mathrm{ADC_{bot}}$ with the capacitor mismatch can be formulated as

$$\mathrm{CW}(B) = (-1)^{b_1 \oplus b_N} \sum_{k=1}^{x-1} \left[(-1)^{b_{k+1} \oplus \overline{b_N}} \times C'_k \right] \times \frac{V_{\mathrm{ref}}}{\sum_{k=0}^{N-1} (C'_k)} \tag{13}$$

where $C'_k = C_k + C_{k,p}$. It is obtained by calculating the difference between the upper bound and the lower bound of each code. For example, the upper bound of $B = 101$ locates at the distance ΔV_{b2} from the center and the lower bound locates at the distance $\Delta V_{b2} - \Delta V_{b1}$ from the center. Therefore, $\mathrm{CW}(101) = \Delta V_{b2} - (\Delta V_{b2} - \Delta V_{b1})$. The detail process of concluding the different conditions to (13) is described in Appendix III. Besides, notie that if $x = N$, i.e., $B = 2^{N-1}$ or $2^{N-1}-1$, then the second summation term in the numerator of (13) is zero, which can be neglected. The nonlinearity is induced by the different ratios of $C_{k,p}$ and those of C_k. Again, the evaluated average code width is obtained in (4), which can be substituted into (5) and (6) to obtain the DNL and INL values, respectively.

There were several studies proposed to reduce the capacitor mismatch by the proper physical design in placement [16], routing [17], and the structure of the unit capacitor [18], [19]. Other circuit techniques such as the calibration technique [20] and capacitor swapping technique [21] also successfully improve the linearity of SAR ADC.

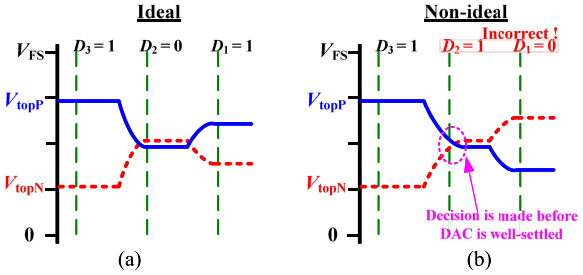

Fig. 10. (a) Complete DAC settling. (b) Incomplete DAC settling.

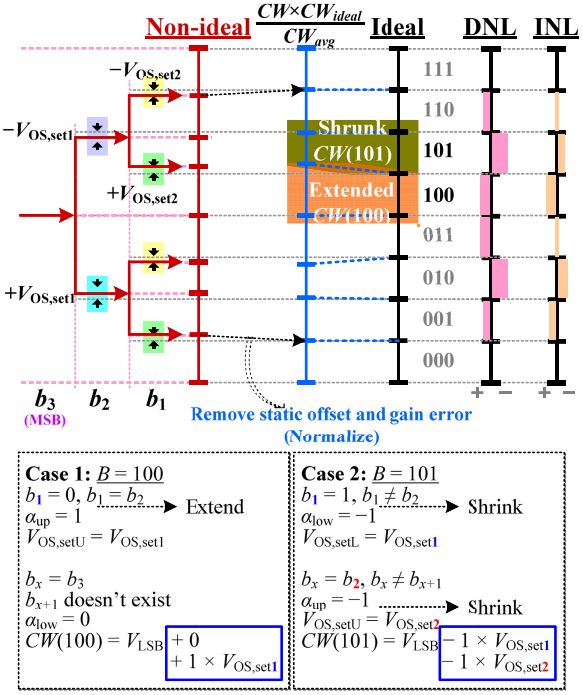

Fig. 11. Decision levels of a 3-b SAR ADC with DAC incomplete settling.

C. DAC Incomplete Settling

DAC's incomplete settling is an awkward problem in high-speed and high-resolution SAR ADCs. As shown in Fig. 10(a), the comparator should make the decision after the voltages on the top plate settle well. If the comparator makes the decision before the DAC settles sufficiently well, it will result in incorrect decision and switching [see Fig. 10(b)]. The decision level will be incorrectly shifted as shown in Fig. 11. The incomplete settling of b_i will move the decision level of b_i toward the decision branch of b_{i+1}. As a result, the shifting mechanism is similar to that of the comparator memory effect shown in Fig. 4. The only difference between them is that DAC incomplete settling may induce various offsets in each bit instead of a constant offset. The magnitude of the offset is dependent on the settling behavior in each bit, which is denoted by $V_{\mathrm{OS},\mathrm{set}i}$ for b_i.

The corresponding code width $\mathrm{CW}(B)$ can be obtained in (14) by modifying (7) because the decision level shifting is similar to that of the memory effect

$$\begin{aligned} \mathrm{CW}(B) &= V_{\mathrm{LSB}} + (\alpha_{\mathrm{low}} \times V_{\mathrm{OS,setL}}) + (\alpha_{\mathrm{up}} \times V_{\mathrm{OS,setU}}) \\ &= V_{\mathrm{LSB}} + [(-1)^{b_1 \oplus b_2} \times V_{\mathrm{OS,set1}} \\ &\quad + (-1)^{b_x \oplus b_{x+1}} \times V_{\mathrm{OS,setx}}] \end{aligned} \tag{14}$$

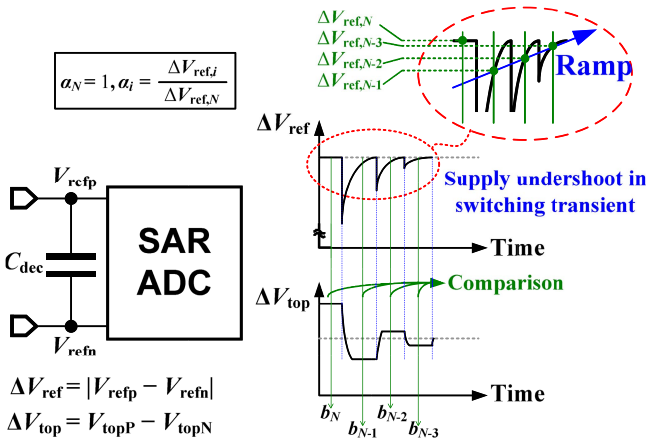

Fig. 12. Undershoot of the reference voltage during the bit conversion phases.

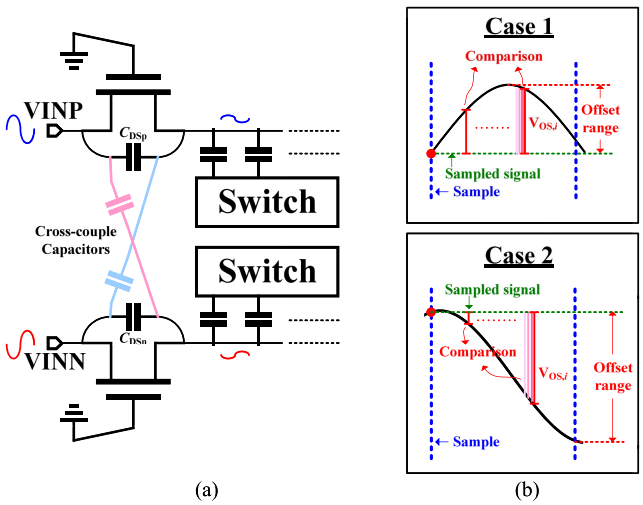

Fig. 13. External input signals couple to the top plates when the sampling switches are turned off. (a) Two cross-coupled capacitors can compensate the coupling signal. (b) Two cases of signal-dependent dynamic offsets.

where a_{low} and a_{up} have been defined in (7). In addition, $V_{\text{OS,setL}}/V_{\text{OS,setU}}$ denotes the lower/upper bound offset. These bounds can be obtained from a modified procedure as shown in Fig. 5. The offset $V_{\text{OS,setL}} = V_{\text{OS,set1}}$ is given if $b_1 = 1$ is obtained and $V_{\text{OS,setU}} = V_{\text{OS,set1}}$ is given if $b_1 = 0$ is obtained. In other words, the offset of the other bound is given as $V_{\text{OS,set}x}$ if the changing bits b_x and b_{x+1} exist.

There are some circuit techniques to resolve the problem of incomplete settling. The commonly used one is the error compensation technique [22], [23]. Alternatively, the bypass window function can reduce the critical DAC switching [24].

D. Undershoot of Reference Voltage

In this section, the reference voltage undershoot is discussed. As shown in Fig. 12, the reference voltage exhibits this undershoot during the DAC's switching transient. Voltage undershoot is induced by the insufficient driving strength of the voltage source or the insufficient on-chip decoupling capacitor. This undershoot could be regarded as a special case of the dynamic gain error as discussed in Section III-A, since the reference voltage becomes a ramp-like signal. As a result, the constant V_{ref} in (8) and (9) should be changed to a function of time (i.e., function of bit) and $a_i(V_{\text{INP}})$ in (12) should be replaced by the gain error parameters a_i (gain error of bit i)

$$\text{CW}(B) = (-1)^{b_1 \oplus b_N} \times \left\{ \begin{array}{l} (\alpha_x - \alpha_1) \times \beta \\ -(\alpha_x + \alpha_1) \times (b_1 \oplus b_N) + \alpha_x \end{array} \right\} \times V_{\text{LSB}}$$

where

$$\beta = \sum_{i=1}^{N-1} \left(b_i \oplus \bar{b}_N\right) \times 2^{i-1}. \tag{15}$$

After removing the static gain error and the offset error, the offset is proportional to β, which is the difference between code B and the middle codes. The b_1 and b_N determine the sign, i.e., positive or negative, of the DNL value. These factors will lead to a trumpet-shaped DNL plot.

E. Input Signal Coupling

The histogram-based testing method is widely used in the ADC linearity test [25], [26]. Intuitively, the frequency of the input sine-wave has no effect on the testing results. However, Nyquist-rate input signal may induce ac-coupling during the bit-conversion phases in practice, and may further result in an undesired trumpet-shaped DNL plot [18]. This issue can be regarded as a special case of the dynamic offset discussed in Section II-B. An example of the input signals coupling and the associated dynamic offset is shown in Fig. 13(a), in which the input signals couple with the top plate of DAC through the parasitic capacitors C_{DSp} and C_{DSn} of the sampling switches.

As shown in Fig. 13(b), the external signals still change during the bit-conversion phases and induce a different offset in each bit-conversion. For a Nyquist rate sine-wave, the offset range is small if the level of the sampled signal is close to the common-mode voltage (Case 1). In contrast, the offset is large if it is close to the rail-to-rail level (Case 2). Thus, the DNLs of both the end codes are worse than those of the middle ones, say the trumpet-shaped DNL plot.

This problem can be solved by adding a pair of cross-coupled capacitors to compensate for the ac-coupling signal [see Fig. 13(a)] [7], or adding dummy switches and decoupling capacitors to isolate the DAC top plates and external signals [27]. The circuit techniques for reducing the sampling switch size and its parasitic capacitor C_{DSp} and C_{DSn}, such as a bootstrapped switch [7], also alleviate this problem.

IV. Experimental Results

This section shows some experimental results of each case mentioned in Sections II and III. To distinguish the issues mentioned in the previous sections, the DNL and INL results are, respectively, obtained from MATLAB behavior models, spice simulations, and measurement results.

A. Dynamic Offset

First, the dynamic offset discussed in Section II-B is investigated. Set the dynamic offset as $V_{\text{OS},bk} = [V_{\text{topP}}(k) + V_{\text{topN}}(k)]/2^N$, where $V_{\text{topP}}(k)$ and $V_{\text{topN}}(k)$ are the top-plate voltages of both the DACs under the conversion phase of b_k.

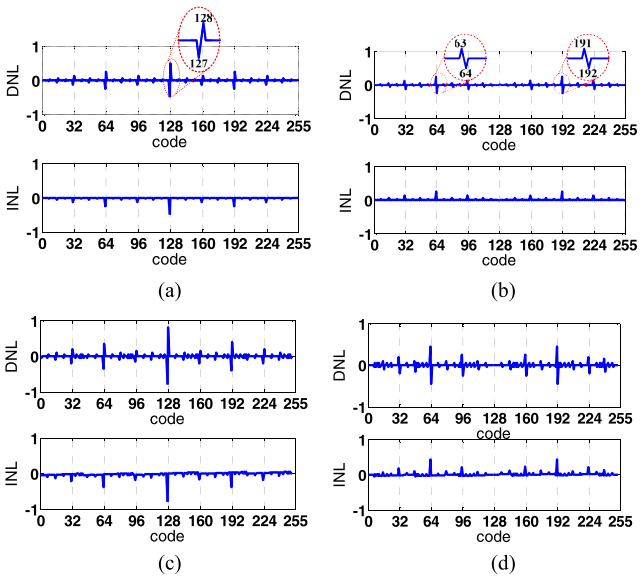

Fig. 14. DNL and INL plots with the dynamic offset. (a) and (b): behavior model simulation results with the monotonic (set-and-up) and switchback switching schemes. (c) and (d): spice simulation results with the monotonic and switchback switching schemes.

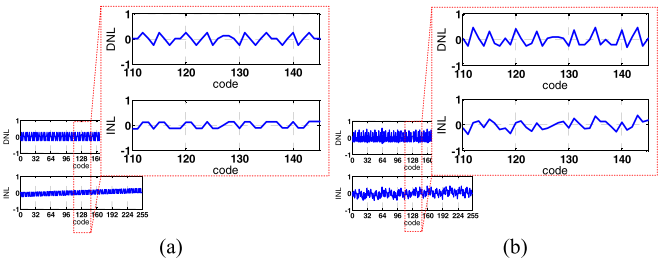

Fig. 15. DNL and INL plots with the memory effect-induced dynamic offset. (a) Behavior model simulation result. (b) Spice simulation result.

If the SAR ADC with the monotonic DAC switching scheme (set-and-up) is used [7], the offset voltage will be gradually increased from the conversion for the MSB to that for the LSB (for an 8-b SAR ADC, $V_{\mathrm{OS},b8} < \cdots < V_{\mathrm{OS},b1}$). According to (3), the maximum and the minimum peaks of DNL must occur when the changing bit b_x is b_8, i.e., $B = 2^{8-1}$ and $2^{8-1} - 1$, respectively. The DNL and INL plots are shown in Fig. 14(a) and are consistent with what we predict in (3); while the maximum offset is $V_{\mathrm{OS},b7}$ if the switchback DAC switching scheme is used [8]. As shown in Fig. 14(b), it results in two maximum peaks at $2^{8-2} - 1 = 63$ and $2^8 - 2^{8-2} - 1 = 191$, and two minimum peaks at $2^{8-2} = 64$ and $2^8 - 2^{8-2} = 192$. The nonlinearity is reduced because the variation range of the common-mode voltage is narrower in the SAR ADC with the switchback DAC switching scheme. The spice simulation results of these two switching schemes are also, respectively, shown in Fig. 14(c) and (d) to demonstrate this issue.

The other source of dynamic offset is the comparator memory effect. Set $V_{\mathrm{OS,mem}} = 0.125\ V_{\mathrm{LSB}}$ for example, and evaluate the code width of the code B with (7). The behavior model simulation result is shown in Fig. 15(a), where the DNL of medium codes (127 and 128) are $V_{\mathrm{OS,mem}}$ (=0.125 V_{LSB}) and the others are either $\pm 2 \times V_{\mathrm{OS,mem}}$ (=$\pm$0.25 V_{LSB}) or 0.

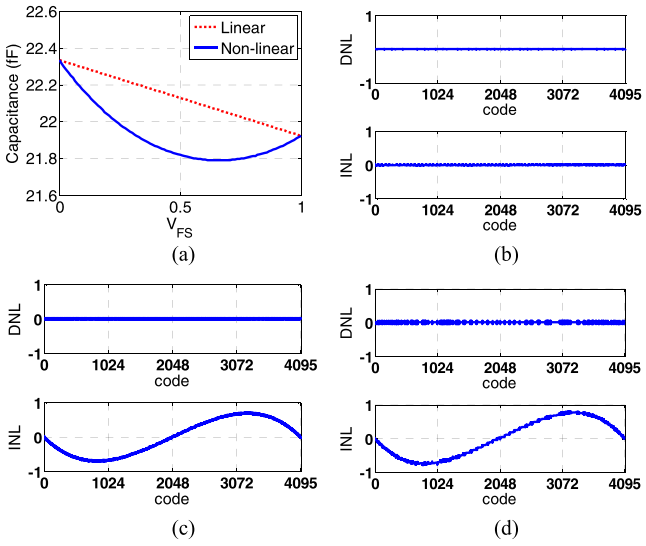

Fig. 16. Voltage-dependent parasitic capacitor may induce the INL of SAR ADC. (a) Relationship between the top-plate voltage and $C_{\mathrm{PC}} + C_{\mathrm{PTS}}$, which are obtained from the spice simulation results. (b) DNL and INL plots of an ADC with linear $C_{\mathrm{Total}}(V)$. (c) DNL and INL plots of an ADC with nonlinear $C_{\mathrm{Total}}(V)$. (d) Spice simulation results of (c).

The spice simulation result in Fig. 15(b) is also consistent with that of the behavior model simulation.

B. Dynamic Gain Error

The voltage-dependent total capacitance $C_{\mathrm{Total}}(V)$ in (10) and (11) induces a dynamic gain error. The examples of linear and nonlinear voltage-to-capacitance functions are shown in Fig. 16(a). After taking the behavior model simulation into discussion, the resultant DNL and INL plots are, respectively, shown in Fig. 16(b) and (c). Both these functions are continuous, so the small difference between $C_{\mathrm{Total}}(V)^{-1} - C_{\mathrm{Total}}(V + V_{\mathrm{LSB}})^{-1}$ is small and leads to an insignificant impact on the DNL plots. If $C_{\mathrm{Total}}(V)$ is a linear function, $V_{\mathrm{INP}} \times C_{\mathrm{Total}}(V_{\mathrm{INP}})$ in (10) induces a second-order term of V_{INP}. A special case is that the second-order distortion only results in a static gain error that can be removed in differential-input SAR ADCs (see Appendix IV). Generally, $C_{\mathrm{Total}}(V)$ is a nonlinear function, the nonlinear $C_{\mathrm{Total}}(V_{\mathrm{INP}})$ in the numerator of (10) has a significant impact on the INL of $\mathrm{ADC_{top}}$. However, the nonlinear $C_{\mathrm{Total}}(V)$ has a negligible impact on the INL of $\mathrm{ADC_{bot}}$ since the $C_{\mathrm{Total}}(V_{\mathrm{CM}})$ in the numerator of (11) is a constant. The spice simulation result shown in Fig. 16(d) is also consistent with the behavior model simulation result of $\mathrm{ADC_{top}}$.

C. Capacitor Mismatch

Two capacitor mismatch examples for 8-b SAR ADCs are discussed to investigate their associated influences. Suppose the ideal capacitances of DAC are {64, 32, 16, 8, 4, 2, 1, 1} fF; nevertheless, in the first case, suppose the capacitances of DAC are deviated to {64, 32, **15.5**, 8, 4, 2, 1, 1} fF. By normalization to make the total capacitance be identical to the ideal value, they can be formulated as $\{2^6 \times A_1,\ 2^5 \times A_1,\ 2^4 \times A_2,\ 2^3 \times A_1,\ 2^2 \times A_1,\ 2^1 \times A_1,\ 2^0 \times A_1,\ 2^0 \times A_1\}$ fF, where A_1 and A_2 are 1.0039 and 0.9725, respectively. In the second

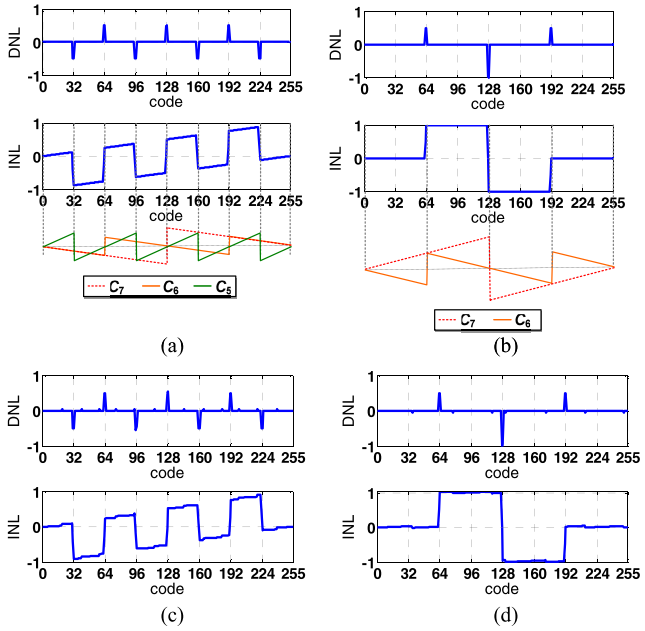

Fig. 17. DNL and INL of a SAR ADC with the capacitor mismatch. (a) Capacitances of DAC are {64, 32, **15.5**, 8, 4, 2, 1, 1} fF. (b) Capacitances of DAC are {**63.5**, **32.5**, 16, 8, 4, 2, 1, 1} fF. (c) Spice simulation results of (a). (d) Spice simulation results of (b).

case, suppose the capacitances of DAC are {**63.5**, **32.5**, 16, 8, 4, 2, 1, 1} fF. After normalization, they can be formulated as $\{2^6 \times A_3, 2^5 \times A_4, 2^4 \times A_5, 2^3 \times A_5, 2^2 \times A_5, 2^1 \times A_5, 2^0 \times A_5, 2^0 \times A_5\}$ fF, where A_3, A_4, A_5 are 0.9922, 1.0156 and 1, respectively. The straight and dashed lines at the bottom of Fig. 17(a) and (b) represent the local gain errors induced by the mismatched capacitors (C_{N-1} to C_{N-3}). The total INL can be obtained from the summation of these local ones. They result in some peaks in the DNL plot and some steps in the INL plot. In addition to the behavior model simulation, spice simulation results are also shown in Fig. 17(c) and (d) to demonstrate this issue.

D. DAC Incomplete Settling

For an ideal conversion of bit b_m, the bottom plate of capacitor C_m should settle to V_{target}, that is, V_{ref} or 0, before the comparator determines the b_m. The DAC incomplete settling occurs if the comparator determines b_m as the bottom plate of C_m just settles to $|V_{\text{target}} - \gamma_m \times V_{\text{LSB}}|$, where γ_m models the settling error. As the capacitance of C_m is $2^{-(N-m)}$ of the total capacitance of DAC, it induces a voltage shifting of $\gamma_m \cdot V_{\text{LSB}}/2^{(N-m)}$ on the top plate. For example, if $N = 10$ and the capacitance of C_9 is 1/2 of the total capacitance of DAC, this induces an offset of $V_{\text{LSB}}/2$ on the top plate (assume $\gamma_9 = 1$). According to (14), the code width of a specific code is adjusted by the settling behavior of the corresponding bit. The settling error of C_m will result in nonlinearity at codes $(2 \cdot j + 1)/2^{(N-m+1)} \times 2^N = (2 \cdot j + 1)/2^{(-m+1)}$, where $j = 0$ to $2^{(N-m)} - 1$. As shown in Fig. 18(a), it induces the negative peaks at codes 256 (≈1/4 full scale) and 767 (≈3/4 full scale), while it induces the positive peaks at codes 255 (≈1/4 full scale) and 768 (≈3/4 full scale). In addition, if γ_8 is 1/2, more peaks are generated at codes about 1/8, 3/8, 5/8, and 7/8 of the

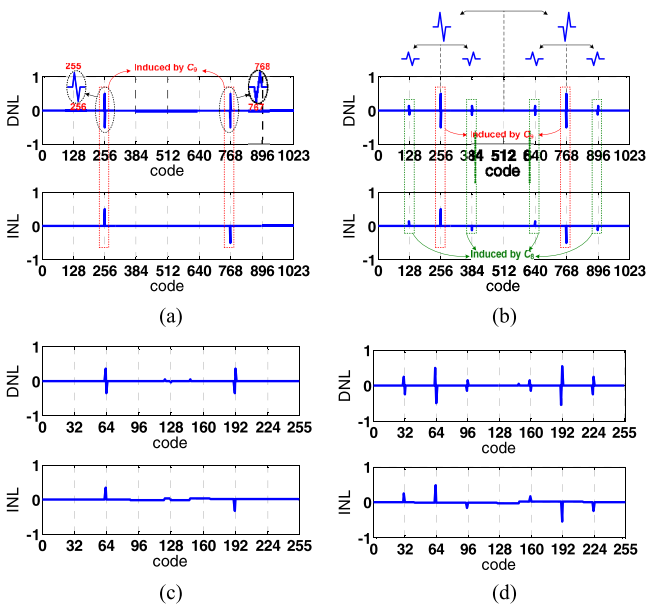

Fig. 18. DNL and INL of a SAR ADC with incomplete settling in DAC. (a) C_9. (b) C_9 and C_8. (c) Spice simulation results of case (a). (d) Spice simulation results of case (b).

full-scale [see Fig. 18(b)]. The magnitudes of these peaks are $V_{\text{LSB}}/8$ since the $V_{\text{LSB}}/2$ gap at the bottom plate of C_8 and the capacitance of C_8 is 1/4 of the total capacitance of DAC. The DNL plots show that the peaks of the corresponding codes are symmetrical to their decision branches. In addition to the behavior model simulation, the spice simulation results shown in Fig. 18(c) and (d) also demonstrate this issue.

E. Undershoot of Reference Voltage

A practical measurement was applied to our design of a 10-b SAR ADC to address the effect induced by the reference voltage undershoot. The causes of the performance degradation can be traced from the measurement results. In addition, the traced cause was included in the spice simulation and was next incorporated into a behavior model. The reference voltage is given as a repeated ramp function in a 10-b SAR ADC behavior model, as shown in Fig. 12. The ramp function is $V_{\text{ref}} - V_{\text{LSB}} + (k/10) \times V_{\text{LSB}}$, where k is the comparison phase of the bit b_k. The corresponding simulation results offered by the spice simulation and behavior model have a similar scenario compared with that obtained from the practical measurements (see Fig. 19). They are all trumpet-shaped as mentioned in Section III-D. The spurs in the measurement results are induced by the capacitor mismatch. It is excluded in the spice and behavior model simulations to identify this individual issue. As a result, this practical design and the associated measurements were the evidences of our investigations addressed in this paper. The circuit designers can refer to this experimental result for determining the suitable on-chip decoupling capacitor and the driving strength of the voltage source.

F. Input Signal Coupling

The external signal will couple to DAC through the parasitic capacitors of the sampling switch C_{DSp} and C_{DSn}

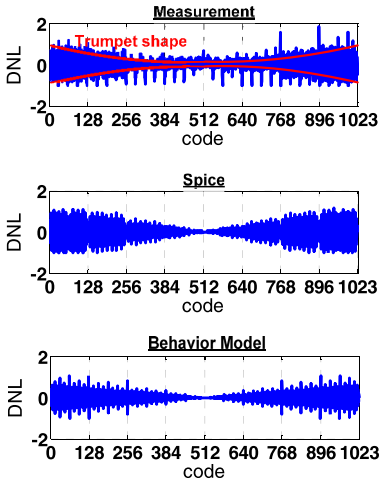

Fig. 19. DNL plots of measurement, spice simulation, and behavior model simulation of a 10-b SAR ADC, which has an undershoot in the reference voltage.

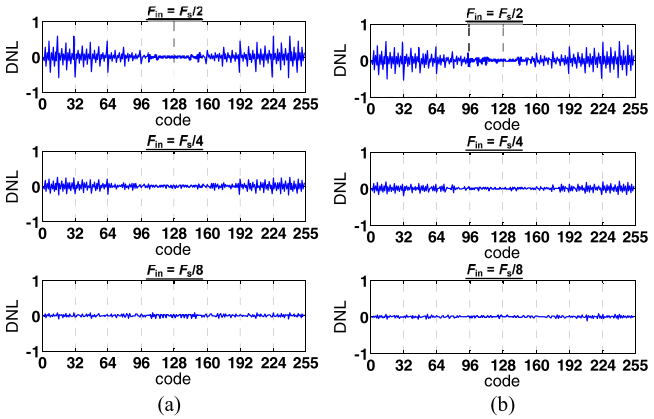

Fig. 20. DNL plots of a SAR ADC with various input signal frequencies ($F_{IN} = F_S/2$ to $F_S/8$). (a) Behavior model simulation. (b) Spice simulation.

in Fig. 13(a) [18]. It results in a trumpet-shaped DNL plot if the input signal frequency (F_{IN}) is close to the Nyquist rate, i.e., half of the sampling frequency (F_S). The DNL plots in Fig. 20 are examples of an 8-b SAR ADC with $C_{DSp} = C_{DSn} = C_{Total} \times 2^{-8}$ under various input signal frequencies ($F_S/2$, $F_S/4$, and $F_S/8$). The Nyquist-rate input signal may induce ac-coupling during the bit-conversion phases and worsen the performance of the DNL; therefore, the performances of DNL are gradually improved by decreasing F_{IN}. Experimentally, when F_{IN} is decreased to $F_S/8$, this effect can be ignored [see Fig. 20(a)]. In addition to the behavior model simulation, the spice simulation results are also shown in Fig. 20(b) to demonstrate this issue.

G. Check Flow and Multiple Errors Example

From the experimental results in this section, the errors can be categorized into four types according to the syndromes on the DNL and INL plots. The first type has slopes or steps in the INL plots. They are induced by the capacitor mismatch. The second type has arbitrary smoothing curves in the INL plots. They are induced by voltage-dependent parasitic capacitors or

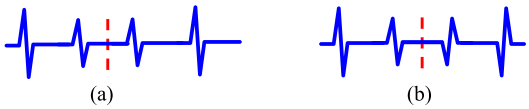

Fig. 21. Different symmetrical types of DNL. (a) Odd symmetry. (b) Even symmetry.

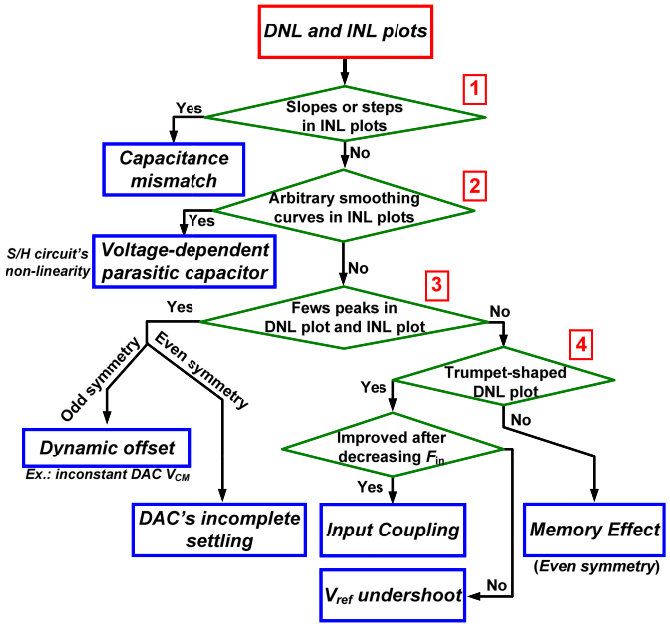

Fig. 22. Check flow for the identification of nonlinearity sources.

the nonlinearity of the sampling switch. The third type has a few peaks in the DNL and INL plots. If the DNL plot exhibits an odd symmetrical to the center [see Fig. 21(a)], this dynamic offset is often induced by inconstant common-mode levels of the compared voltages. If the DNL exhibits an even symmetrical to the middle code [see Fig. 21(b)], this syndrome is induced by the DAC's incomplete settling or memory effect (uniform peaks) in the comparator. The fourth type has a trumpet-shaped DNL. It is usually generated by the reference voltage undershoot and the coupling of the Nyquist rate input sine-wave in linearity testing. We can summarize the aforementioned errors to a systematic check flow for identifying the nonlinearity factors, as shown in Fig. 22.

From the previous sections, the effects of each individual error on the functionality of the SAR ADC are investigated, respectively. In practice, multiple errors may occur at the same time. The analysis of the deviated functionality due to multiple errors is more complex than that due to a single error. Fortunately, it is possible to identify the *dominant error*. If the shapes of the DNL/INL plots, which are induced by the different errors, are dissimilar to a large degree, such as peaks and slopes, then the derived qualitative analysis would be easily carried out by observing the dominant syndrome of the DNL/INL plots. For example, the dynamic offset induces odd symmetry peaks (odd symmetry has been defined in Fig. 21) in the DNL plot as shown in Fig. 14(d) and the capacitor mismatch induces slopes in the INL plot as shown in Fig. 23(a)

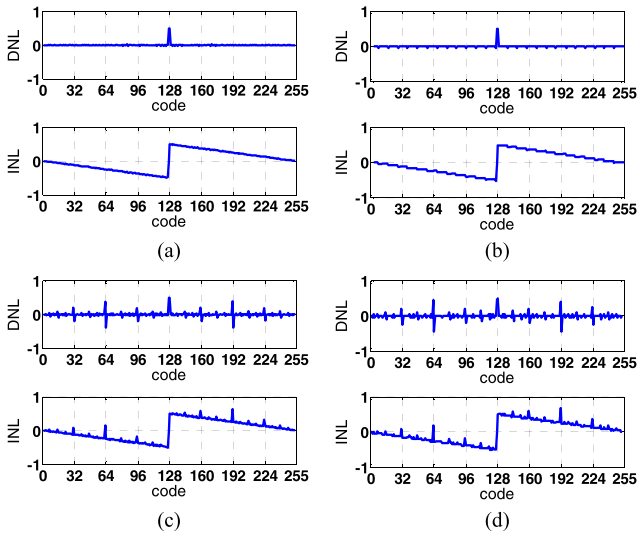

Fig. 23. DNL and INL of a SAR ADC with multiple errors. (a) Capacitor mismatch: the capacitances of DAC are {**64.5**, 32, 16, 8, 4, 2, 1, 1} fF. (b) Spice simulation results of (a). (c) Multiple errors: the capacitor mismatch as in (a) and the dynamic offset as in Fig. 14(d). (d) Spice simulation results of (c).

for the behavior model simulation and Fig. 23(b) for the spice simulation. If these errors occur at the same time, the syndromes of the resultant DNL and INL plots will combine the peaks and slopes as shown in Fig. 23(c) and (d) for the behavior model simulation and spice simulation, respectively. According to the check flow in Fig. 22, the answers to questions 1 and 3 are yes, then we can conclude that the possible dominant error is either the capacitor mismatch or the dynamic offset. We can make other analysis to further distinguish which one is the critical error.

V. Conclusion

This paper investigates some error sources and their corresponding effects on the SAR ADC linearity performance. The errors can be categorized into four types to combine the effects of: 1) capacitor mismatch; 2) voltage-dependent parasitic capacitors or the nonlinearity of sampling switch; 3) DAC's incomplete settling or comparator's memory effect; and 4) the reference voltage undershoot or the coupling issue. As a result, we can identify the individual effect of the error on the nonlinearity of the SAR ADC by a systematic check flow. In subsequence, behavior model simulations, spice simulations, and measurements are performed to verify the comprehensive cause–effect analysis. The simulation for each error source is given explicitly to verify the error individually, and good agreements between analyses and experiments are obtained. From the analyzed types of errors, circuit designers and test engineers can identify the causes of error from the observed syndromes and try to remove their effects according to the recommended solution guidelines of this paper.

Appendix I

This appendix shows the detail derivation of (8) and (9). They can be formulated, respectively, from (A.1) and (A.2) by charge conservation, where Q_{Sample} and $Q_{\text{Conversion}}$ are the charges at the sampling phase and conversion phase,

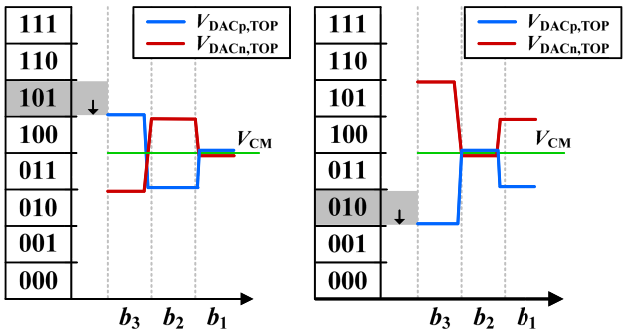

Fig. 24. Top plate voltages during the bit conversion for different input voltages. (a) Lower bound voltage of $B = 101$. (b) Lower bound voltage of $B = 010$.

respectively. For the SAR ADC operated with the top-plate sampling, we obtain the following relationships:

ADC_{top}:

$$\begin{aligned} Q_{\text{Sample}} &= (V_{\text{INP}} - V_{\text{ref}}) \times \left[\sum_{k=1}^{N-1} (C_k + C_{k,p})\right] \\ &\quad + (V_{\text{INP}} - 0) \times C_{P,\text{TOP}} \\ Q_{\text{Conversion}} &= \sum_{k=1}^{N-1} \{[V_{\text{DAC,TOP}}(V_{\text{INP}}) - \bar{b}_{k+1} V_{\text{ref}}] \\ &\quad \times (C_k + C_{k,p})\} \\ &\quad + [V_{\text{DAC,TOP}}(V_{\text{INP}}) - 0] \times C_{P,\text{TOP}} \\ \text{Apply } Q_{\text{Sample}} &= Q_{\text{Conversion}} \\ \Rightarrow V_{\text{DAC,TOP}}(V_{\text{INP}}) &= V_{\text{INP}} - \frac{V_{\text{ref}}}{C_{\text{Total}}} \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) \end{aligned}$$

where

$$C_{\text{Total}} = C_{P,\text{TOP}} + \sum_{k=0}^{N-1} (C'_k), \quad C'_k = C_k + C_{k,p}. \tag{A.1}$$

Next, for the SAR ADC operated with the bottom-plate sampling, we obtain the following relationships:

ADC_{bot}:

$$\begin{aligned} Q_{\text{Sample}} &= (V_{\text{CM}} - V_{\text{INP}}) \times \left[\sum_{k=0}^{N-1} (C_k + C_{k,p})\right] \\ &\quad + (V_{\text{CM}} - 0) \times C_{P,\text{TOP}} \\ Q_{\text{Conversion}} &= \sum_{k=1}^{N-1} \{[V_{\text{DAC,BOT}}(V_{\text{INP}}) - b_{k+1} V_{\text{ref}}] \\ &\quad \times (C_k + C_{k,p})\} \\ &\quad + [V_{\text{DAC,BOT}}(V_{\text{INP}}) - V_{\text{CM}}] \times C'_0 \\ &\quad + [V_{\text{DAC,BOT}}(V_{\text{INP}}) - 0] \times C_{P,\text{TOP}} \\ \text{Apply } Q_{\text{Sample}} &= Q_{\text{Conversion}} \\ \Rightarrow V_{\text{DAC,BOT}}(V_{\text{INP}}) &= V_{\text{CM}} + \sum_{k=1}^{N-1} \left[\left(\frac{C'_k}{C_{\text{Total}}}\right) \times (b_{k+1} V_{\text{ref}} - V_{\text{INP}})\right] \\ &\quad + \frac{C'_0}{C_{\text{Total}}} \times (V_{\text{CM}} - V_{\text{INP}}). \end{aligned} \tag{A.2}$$

APPENDIX II

To obtain the code width CW(B) by considering the gain error, (12) is concluded from four conditions as

$$\begin{aligned}\mathrm{CW}(B)=&\begin{cases}[\alpha_x(V_{\mathrm{INP}})\times(\beta+1)-\alpha_1(V_{\mathrm{INP}})\times\beta]\times V_{\mathrm{LSB}} \\ \qquad\qquad \text{when } b_N=1, b_1=1 \\ [\alpha_1(V_{\mathrm{INP}})\times(\beta+1)-\alpha_x(V_{\mathrm{INP}})\times\beta]\times V_{\mathrm{LSB}} \\ \qquad\qquad \text{when } b_N=1, b_1=0 \\ [\alpha_1(V_{\mathrm{INP}})\times(\beta+1)-\alpha_x(V_{\mathrm{INP}})\times\beta]\times V_{\mathrm{LSB}} \\ \qquad\qquad \text{when } b_N=0, b_1=1 \\ [\alpha_x(V_{\mathrm{INP}})\times(\beta+1)-\alpha_1(V_{\mathrm{INP}})\times\beta]\times V_{\mathrm{LSB}} \\ \qquad\qquad \text{when } b_N=0, b_1=0\end{cases} \\ =&(-1)^{b_1\oplus b_N} \\ &\times\begin{Bmatrix}\alpha_x(V_{\mathrm{INP}})\times[\beta+1-(b_1\oplus b_N)] \\ -\alpha_1(V_{\mathrm{INP}})\times[\beta+(b_1\oplus b_N)]\end{Bmatrix}\times V_{\mathrm{LSB}}\end{aligned}$$

where

$$\beta=\sum_{i=1}^{N-1}(b_i\oplus\bar{b}_N)\times 2^{i-1}. \tag{A.3}$$

APPENDIX III

When considering the capacitor mismatch, the code width CW(B) can be easily obtained by calculating the difference between the distances from the V_{CM} to the upper bound $V_{\mathrm{up}}(B)$ and the lower bound $V_{\mathrm{low}}(B)$, i.e., $\mathrm{CW}(B)=[V_{\mathrm{up}}(B)-V_{\mathrm{CM}}]-[V_{\mathrm{low}}(B)-V_{\mathrm{CM}}]$. According to the values of b_N and b_1, there are four conditions expressed as

$$\begin{aligned}\mathrm{CW}(B)=&\frac{V_{\mathrm{ref}}}{\sum_{k=0}^{N-1}(C'_k)} \\ &\times\begin{cases}\sum_{k=x}^{N-1}[S(b_{k+1})\times C'_k]-\sum_{k=1}^{N-1}[S(b_{k+1})\times C'_k] \\ \qquad\qquad \text{when } b_N=1, b_1=1 \\ \sum_{k=1}^{N-1}[S(b_{k+1})\times C'_k]-\sum_{k=x}^{N-1}[S(b_{k+1})\times C'_k] \\ \qquad\qquad \text{when } b_N=1, b_1=0 \\ \sum_{k=1}^{N-1}[S(\overline{b_{k+1}})\times C'_k]-\sum_{k=x}^{N-1}[S(\overline{b_{k+1}})\times C'_k] \\ \qquad\qquad \text{when } b_N=0, b_1=1 \\ \sum_{k=x}^{N-1}[S(\overline{b_{k+1}})\times C'_k]-\sum_{k=1}^{N-1}[S(\overline{b_{k+1}})\times C'_k] \\ \qquad\qquad \text{when } b_N=0, b_1=0\end{cases}\end{aligned} \tag{A.4}$$

where the $S(b_{k+1})$ denotes the sign (plus or minus) of the C'_k because the bit b_{k+1} determines the switching of C'_k. The $S(b_{k+1})$ is defined and represented as

$$S(b_{k+1})=\begin{cases}+1, & \text{when } b_{k+1}=1 \\ -1, & \text{when } b_{k+1}=0\end{cases}=-(-1)^{b_{k+1}}. \tag{A.5}$$

Then, (A.4) can be simplified as

$$\begin{aligned}\mathrm{CW}(B)=&\frac{V_{\mathrm{ref}}}{\sum_{k=0}^{N-1}(C'_k)} \\ &\times\begin{cases}-\sum_{k=1}^{x-1}[S(b_{k+1})\times C'_k], & \text{when } b_N=1, b_1=1 \\ \sum_{k=1}^{x-1}[S(b_{k+1})\times C'_k], & \text{when } b_N=1, b_1=0 \\ \sum_{k=1}^{x-1}[S(\overline{b_{k+1}})\times C'_k], & \text{when } b_N=0, b_1=1 \\ -\sum_{k=1}^{x-1}[S(\overline{b_{k+1}})\times C'_k], & \text{when } b_N=0, b_1=0.\end{cases}\end{aligned} \tag{A.6}$$

Equation (A.6) can be further simplified using the well-known exclusive OR symbols for a more general representation

$$\begin{aligned}\mathrm{CW}(B)=&-(-1)^{b_1\oplus b_N}\sum_{k=1}^{x-1}[S(b_{k+1}\oplus\overline{b_N})\times C'_k] \\ &\times\frac{V_{\mathrm{ref}}}{\sum_{k=0}^{N-1}(C'_k)}.\end{aligned} \tag{A.7}$$

Finally, we can substitute (A.5) into (A.7) to obtain (13), which is also repeated as follows:

$$\mathrm{CW}(B)=(-1)^{b_1\oplus b_N}\sum_{k=1}^{x-1}[(-1)^{b_{k+1}\oplus\overline{b_N}}\times C'_k]\times\frac{V_{\mathrm{ref}}}{\sum_{k=0}^{N-1}(C'_k)}. \tag{A.8}$$

APPENDIX IV

This appendix gives the detailed derivation to prove that the linear voltage-dependent capacitor has no influence on the linearity of the differential-input SAR ADC, which is mentioned in Section IV-B.

The differential input voltage of SAR ADC, i.e., $V(B)=V_{\mathrm{INP}}-V_{\mathrm{INN}}$, can be utilized to denote the lower bound of code B. Therefore, the residue voltages on the top plates of the differential DAC, denoted by $V_{\mathrm{DACp,TOP}}$ and $V_{\mathrm{DACn,TOP}}$, will be the common-mode voltage (V_{CM}) in the conversion phase for bit b_1 or b_x. For example, if code $B=101$ or 010, b_2 is the changing bit, then the $V_{\mathrm{DACp,TOP}}$ and $V_{\mathrm{DACn,TOP}}$ are equal to V_{CM} in the conversion phase for bit b_1 when $B=101$, while the $V_{\mathrm{DACp,TOP}}$ and $V_{\mathrm{DACn,TOP}}$ are equal to V_{CM} in the conversion phase for bit b_2 when $B=010$ (see Fig. 24).

We can obtain the following equation because the top plates of the differential DAC will be either $V_{\mathrm{CM},b1}$ in the conversion phase for bit b_1, or $V_{\mathrm{CM},bx}$ in the conversion phase for bit b_x:

$$V_{\mathrm{DACp,TOP}}(V_{\mathrm{INP}})=V_{\mathrm{DACn,TOP}}(V_{\mathrm{INN}})=V_{\mathrm{CM},b1}\text{ or }V_{\mathrm{CM},bx}. \tag{A.9}$$

The code width of code B can be formulated as

$$\mathrm{CW}(B)=V(B+1)-V(B). \tag{A.10}$$

We assume that the relationship between the capacitance and the voltage is linear as follows:

$$C_{\text{Total}}(V) = a_1 \times V + a_2 \tag{A.11}$$

where a_1 and a_2 are two constant numbers. According to (10) and (A.9), the following are obtained:

$$\begin{aligned} V_{\text{DACp,TOP}}(V_{\text{INP}}) &= V_{\text{DACn,TOP}}(V_{\text{INN}}) \\ &\Rightarrow \frac{V_{\text{INP}} \times C_{\text{Total}}(V_{\text{INP}})}{C_{\text{Total}}(V_{\text{DACp,TOP}})} - \frac{V_{\text{ref}}}{C_{\text{Total}}(V_{\text{DACp,TOP}})} \\ &\quad \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) \\ &= \frac{V_{\text{INN}} \times C_{\text{Total}}(V_{\text{INN}})}{C_{\text{Total}}(V_{\text{DACn,TOP}})} - \frac{V_{\text{ref}}}{C_{\text{Total}}(V_{\text{DACn,TOP}})} \\ &\quad \times \sum_{k=1}^{N-1} (C'_k \times \overline{b}_{k+1}). \end{aligned}$$

Remove the denominators of both sides since they are ideally the same $C_{\text{Total}}(V_{\text{DACp,TOP}}) = C_{\text{Total}}(V_{\text{DACn,TOP}})$

$$\begin{aligned} &V_{\text{INP}} \times C_{\text{Total}}(V_{\text{INP}}) - V_{\text{ref}} \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) \\ \Rightarrow\ &= V_{\text{INN}} \times C_{\text{Total}}(V_{\text{INN}}) - V_{\text{ref}} \times \sum_{k=1}^{N-1} (C'_k \times \overline{b}_{k+1}). \end{aligned}$$

Then, the input voltage and the reference voltage are, respectively, gathered together on both sides of the equal sign

$$\begin{aligned} &V_{\text{INP}} \times C_{\text{Total}}(V_{\text{INP}}) - V_{\text{INN}} \times C_{\text{Total}}(V_{\text{INN}}) \\ &= V_{\text{ref}} \times \sum_{k=1}^{N-1} (C'_k \times b_{k+1}) - V_{\text{ref}} \times \sum_{k=1}^{N-1} (C'_k \times \overline{b}_{k+1}) \\ &= V_{\text{ref}} \times \sum_{k=1}^{N-1} [C'_k \times (b_{k+1} - \overline{b}_{k+1})] \\ &= V_{\text{ref}} \times \sum_{k=1}^{N-1} [-C'_k \times (-1)^{b_{k+1}}]. \end{aligned}$$

Substitute (A.11) into the above equation to obtain the following:

$$\begin{aligned} &V_{\text{ref}} \times \sum_{k=1}^{N-1} [-C'_k \times (-1)^{b_{k+1}}] \\ &= V_{\text{INP}} \times (a_1 \times V_{\text{INP}} + a_2) - V_{\text{INN}} \times (a_1 \times V_{\text{INN}} + a_2) \\ &= a_1 \times (V_{\text{INP}} + V_{\text{INN}}) \times (V_{\text{INP}} - V_{\text{INN}}) + a_2 \times (V_{\text{INP}} - V_{\text{INN}}) \\ &= a_1 \times (2V_{\text{CM}}) \times V(B) + a_2 \times V(B). \end{aligned}$$

The lower bound voltage of code B is obtained as follows:

$$\begin{aligned} V(B) &= \frac{V_{\text{ref}} \times \sum_{k=1}^{N-1} [-C'_k \times (-1)^{b_{k+1}}]}{a_1 \times (2V_{\text{CM}}) + a_2} \\ &= \frac{V_{\text{ref}} \times \sum_{k=1}^{N-1} [-C'_k \times (-1)^{b_{k+1}}]}{C_{\text{Total}}(2V_{\text{CM}})}. \end{aligned}$$

The constant in the denominator induces a static gain error and the linearity is maintained. Substitute V_B into (A.6), then the code width of code B is

$$\begin{aligned} \text{CW}(B) &= V(B+1) - V(B) = \frac{2C_1 \times V_{\text{ref}}}{C_{\text{Total}}(2V_{\text{CM}})} \\ &= A_{\text{const}} \times V_{\text{LSB}}. \end{aligned}$$

This shows that all code widths are equal and the DNL and INL values are zero after removing the static gain error term A_{const}.

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