A Primary-Auxiliary Temperature Sensing Scheme for Multiple Hotspots in System-on-a-Chips

Peng-Yu Chen, Guan-Ying Huang, Ya-Ting Shyu, and Soon-Jyh Chang

***Abstract*— A primary-auxiliary temperature sensing scheme for system-on-a-chip application is proposed in this paper. Taking advantage of the high accuracy and linearity of the analog primary temperature sensors and low production cost of the digital auxiliary temperature sensors, this sensing scheme monitors multiple hotspots in a highly integrated system chip with small area and low power. A cost efficient calibration strategy based on the difference of calibration complexity and sensitivity to the MOSFET aging between the primary and auxiliary temperature sensors is also presented in this paper. Both the temperature sensor prototypes are designed and fabricated with a 90-nm CMOS process technology. The core area of the primary/auxiliary temperature sensors is 0.039/0.001 mm^2, and consumed energy per conversion is 20.06/0.136 nJ/S with a 1 V supply voltage and 100-kS/s conversion rate. The performance of the temperature sensors and the accuracy improvement of the proposed calibration method are proved with the measurement results.**

***Index Terms*— Multiple hotspots, SAR ADC, primary-auxiliary, temperature sensing, MOSFET aging.**

I. Introduction

With the development of CMOS process, the number of system-on-a-chip (SoC) system chips with multiple high-speed cores and functional designs increases. In the meanwhile, highly integrated chips result in more heat generation. Due to the limitation of heat dissipation, overheating of the chips is a serious problem because the temperature over the throttle point may destroy the chips and even do harm to human bodies, especially at certain areas with high frequency switching activity or high power density. These localized high-temperature areas are called hotspots. Thermal/power management is crucial for system performance and energy efficiency. As an important component of the thermal/power management, a temperature sensing system on a system chip monitors all the hotspots. Traditional temperature sensors utilize off-chip components, and the measurable hotspot location is restricted. On-chip smart temperature sensors are attractive for their benefits of easy interfacing with other on-chip functional blocks and low production cost. These sensors report immediate thermal conditions to the thermal management unit in order to monitor system reliability and performance as a result of temperature variation [1], [2]. Moreover, the off-chip cooling systems can also tune their operation level according to the on-chip thermal massages [3].

High accuracy is the first main concern of many researches on smart temperature sensors in the past years. One well-known structure was accomplished by using bipolar junction transistors (BJT) as the temperature signal source and utilizing a sigma-delta analog-to-digital converter ($\Sigma\Delta$ ADC) to digitize the signal [4]. A large number of conversion cycles are still needed even when a second-order $\Sigma\Delta$ modulator is chosen. This kind of signal conversion also needs a timing control circuit with careful design to guarantee the correct operation in extreme temperature conditions [5]. Though high accuracy as $\pm$0.25 °C can be achieved by these temperature sensor, the area of the temperature sensors is several mm^2, which is too large for system integration. Reference [6] shows a temperature sensor with a zoom ADC, which combines the benefits of successive approximation register (SAR) and $\Sigma\Delta$ ADCs, to reduce conversion cycles and simply the modulator design. The core area is shrunk under 1 mm^2 as well. To improve the accuracy of the zoom ADC, a wider comparing range for fine conversion is proposed [7], [8]. To further decrease the power consumption, a temperature sensor with a modified sampling scheme and a modulator is proposed [9]. These analog sensors are highly accurate (error <0.2 °C) in general, with the penalties of higher circuit complexity and thus larger chip area. The corresponding conversion rate is low, and many off-chip digital processing circuits, such as decimation filter and digital back-end circuit, are usually needed to fulfill the function or calibration of the smart temperature sensors.

After the research of high accuracy, for the purpose of low production cost and high integration potential, there are the other series of temperature sensors structures, which are based on the delay of digital logic gates. One implementation uses the pulse width formed by a temperature-sensitive delay line as the temperature signal, and a time-to-digital converter (TDC) digitizes the temperature-modulated pulse width [10]. The main drawback of this structure is the conversion time of the TDC is too long, and a modified version, which uses SAR logic to compare a temperature dependent delay line

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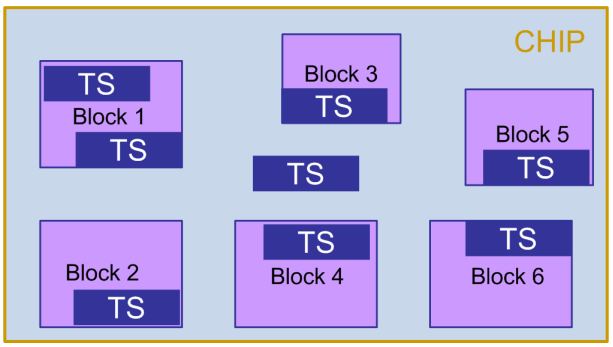

Fig. 1. System chip with multiple hotspots.

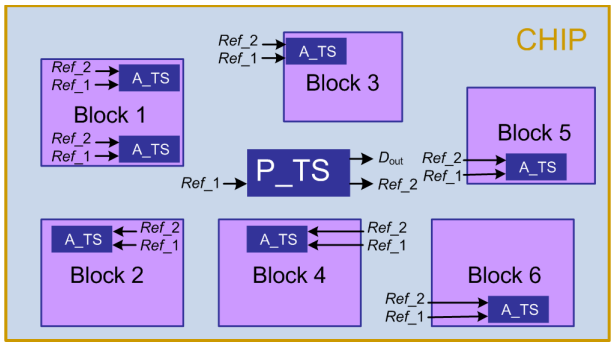

Fig. 2. System chip with the primary-auxiliary sensing scheme.

and a constant one [11], is proposed. Though this modification saves the conversion time, many delay cells are still needed to form the delay lines, and they occupy the most area of the temperature sensor. A temperature sensor with a cyclic delay line, which combines a short delay line and a cycle counter, drastically reduces the delay cells needed [12]. Another counter triggered by a reference clock signal is utilized to quantize the pulse width. The cyclic delay line can be replace with a ring oscillator and a timing amplifier [13], and the total gate count of the pulse generator is further reduced. Though these time domain digital sensors usually outperform the analog ones in terms of power consumption and area, they also have larger inaccuracy and nonlinearity than the analog ones do. To improve the accuracy of the digital temperature sensor, a more careful calibration process is often necessary. Furthermore, the propagation delay of the delay cells, due to the negative/positive bias temperature instability (N/PBTI) effect, would degrade with time [2], [14]. These digital temperature sensor structures may need re-calibration after a period of time, and another cost is thus introduced.

For temperature sensor design, linearity, accuracy, and product cost need careful consideration. In a system chip with multiple functional blocks, as shown in Fig. 1, multiple temperature sensors are needed for reporting real-time thermal conditions of the hotspots, so the total calibration cost would be an additional critical design criterion. Using all temperature sensors with aforementioned analog structures can promise the qualities of the measurements, but the feasibility is limited by the total area occupied by the sensing system. A previously presented solution is setting temperature sensing elements remotely over the whole chip and utilizing the same $\Sigma\Delta$ ADC to convert all the temperature-dependent signals into digital codes [15]. This sensing scheme drastically reduces the total area, but it needs complex remote sensing techniques and compensation mechanisms to avoid errors which come from the parasitic resistors in the path connecting the temperature sensing elements and the ADC. Moreover, the thermal gradient becomes larger with the higher and higher operation speed [2], and the gradients at different blocks vary for different instructions or functions in modern system chips. The number of remote sensing elements with this sensing scheme is limited by the maximum conversion rate of the ADC and the maximum thermal gradients of the hotspots.

In this paper, we propose a primary-auxiliary temperature sensing scheme for monitoring the system chips with multiple hotspots. The main temperature sensing scheme is depicted in Section II. Two kinds of temperature sensor structures are presented in Section III, and the design philosophy is to enhance the area and power efficiency for system integration. A calibration scheme which guarantees the performance of all the temperature sensors in the system chip and reduces the calibration/re-calibration cost in the whole life time of the thermal monitoring system is proposed in Section IV. The proof-of-concept circuits have been fabricated in a standard 90-nm CMOS process and their measurement results are given in Section V. A brief conclusion is drawn in Section VI.

II. Main Temperature Sensing Scheme

Fig. 1 presents a SoC system chip with multiple functional blocks. As shown in this picture, the structures of all on-chip temeprature sensors are the same in the conventional temperature sensing scheme. As mentioned above, if we want to monitor all the hotspots with the analog temperature sensors for sufficient accuracy and simple calibration process, the total chip area and power consumption of the measuring system will be considerable for the highly linear and temperature-dependent signal source and accurate analog-to-digital conversion. Moreover, while the supply voltages decreases with the process progress, the design of analog circuit in this kind of temperature sensor becomes more complicated. On the contrary, if all the temperature sensor structures are digital ones, we need to carefully calibrate all the temperature sensors and this may be resource- and time-consuming. Both the two solutions mentioned above introduce much cost in the SOC integration.

A primary-auxiliary temperature sensing scheme is proposed here, and the main concern of it is to monitor the thermal condition of the multiple hotspots in a system chip in an efficient way. The temperature sensor arrangement of the proposed scheme is shown in Fig. 2. A temperature sensing system, which includes one primary temperature sensor (P_TS) and multiple auxiliary temperature sensors (A_TSs), monitors all the hotspots in the system chip. The analog P_TS uses the BJT transistors as the temperature sensing elements and a SAR ADC to convert the temperature-dependent signal

Fig. 3. Flow diagram of a smart temperature sensor.

into output digital codes. In our proposed calibration process, the P_TS has a sufficient accuracy and linearity after a simple one-point calibration with an external temperature reference *Ref*_1. The reason that a one-point calibration is sufficient for the P_TS will be explained in Section IV. A.

Multiple remote digital A_TSs are located at the hotspots of the important functional blocks. These A_TSs are composed of simple digital logic gates and highly efficient on power consumption and area. The accuracy and linearity of the A_TSs is inferior to those of the P_TS, so a second-point calibration is need for the A_TSs except the one-point calibration with *Ref*_1. During the second-point calibration process, the P_TS after one-point calibration serves as an on-chip reference for its sufficient accuracy. When the P_TS serves as a temperature reference, the digitized *Ref*_2 reference suffers much less from the parasitic resistance. Moreover, The conversion of the A_TSs is independent of that of the P_TS, so the number of the A_TSs is not limited by the operation rate of the P_TS. After this initial calibration, both the P_TS and A_TSs have sufficient accuracy, and much calibration cost can be saved. However, after a long time of using, the accuracy of the A_TSs may degrade due to the N/PBTI effect. A subsequent calibration is also presented in Section IV, and this calibration can keep the accuracy of the A_TSs during the entire lifetime of the system chip. The other advantage that we take the P_TS as the on-chip reference is the accuracy of the digital reference temperature message from the P_TS would not degrade with the change of parasitic condition of the signal path in the chip. With this primary-auxiliary temperature sensing scheme, we can reduce the total area and power consumption of the temperature sensing system and simplify the calibration process as well.

The main design concept of the P_TS and the A_TS utilized in the proposed sensing scheme is to meet the medium resolution requirement (about 1 °C/LSB) with as small area and low power consumption as possible in the 0 to 100 °C temperature range, which is suitable for the thermal monitoring of the system chips.

III. Temperature Sensor Structures

As shown in Fig. 3, a smart temperature sensor converts a temperature-dependent signal to output digital code, and the accuracy of the output code is affected by both the signal source and signal conversion method. Both the P_TS and A_TS structures in the proposed temperature sensing scheme are illustrated as follow.

A. Primary Temperature Sensor

The P_TS is mainly composed of two parts: an analog front-end circuit and a single-ended SAR ADC. The front-end

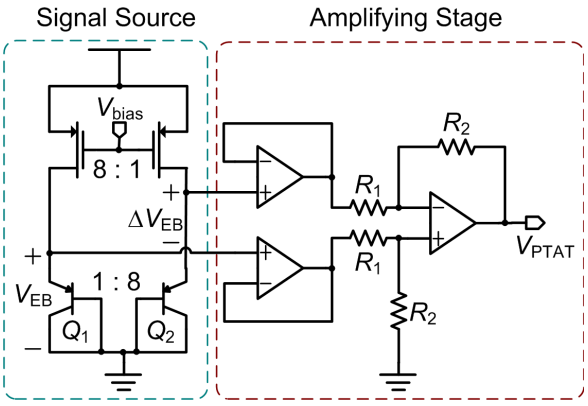

Fig. 4. Analog front-end circuit.

circuit generates a temperature-dependent voltage, and the power-efficient SAR ADC converts this signal into output digital code. Compared with the NPN BJT and the MOSFET transistors in sub-shreshold region [16], [17], PNP substrate BJT transistors are commonly used as the signal source for its compatibility with the general CMOS process. Fig. 4 shows the structure of the analog front-end, which involves a signal source stage and an amplifying stage. Two kinds of temperature-dependent voltages can be extracted from the signal source. One is the emitter-base voltage of the BJT transistor V_{EB}, whose value can be described by the following equation:

$$V_{EB}(T) = V_T \ln\left(\frac{I_{Q1}}{I_S(T)}\right) \tag{1}$$

where $V_T = kT/q$ is the thermal voltage of diodes, k is Boltzmann constant, q is the electron charge, T is the absolute temperature in Kelvins, I_S is the transistor's saturation current, and I_{Q1} is the current flowing through Q_1 As a result of the strong temperature dependency of I_S, V_{EB} is complementary to the absolute temperature (CTAT) and has a negative temperature coefficient of approximately −2 mV/ °C. The value of V_{EB} depends on the absolute values of both I_S and I_{Q1}, and therefore varies with the process spread or imposed mechanical stress [18]. This non-ideality of V_{EB} introduces offset and gain errors into the sensor output, and thus a complicated calibration method is needed for compensate the both errors.

In this work, instead of using V_{EB} as the measure of temperature, we utilize the voltage difference of two BJT transistors ΔV_{EB}, which can be derived as

$$\Delta V_{EB} = V_T \ln(N) \tag{2}$$

where N is the current density ratio between the two BJT transistors. This voltage difference only depends on the current density ratio, making the temperature variation of ΔV_{EB} an accurate measure of temperature. A sufficient accuracy can be achieved with careful design and layout consideration. Moreover, ΔV_{EB} is highly linear compared with V_{EB}, which suffers from the non-linear curvature. Though ΔV_{EB} is a good temperature signal, one drawback of it is that this voltage difference is too small for SAR ADC conversion. In this work, the area ratio of BJT transistor Q_1 to Q_2 is 1:8, and the current

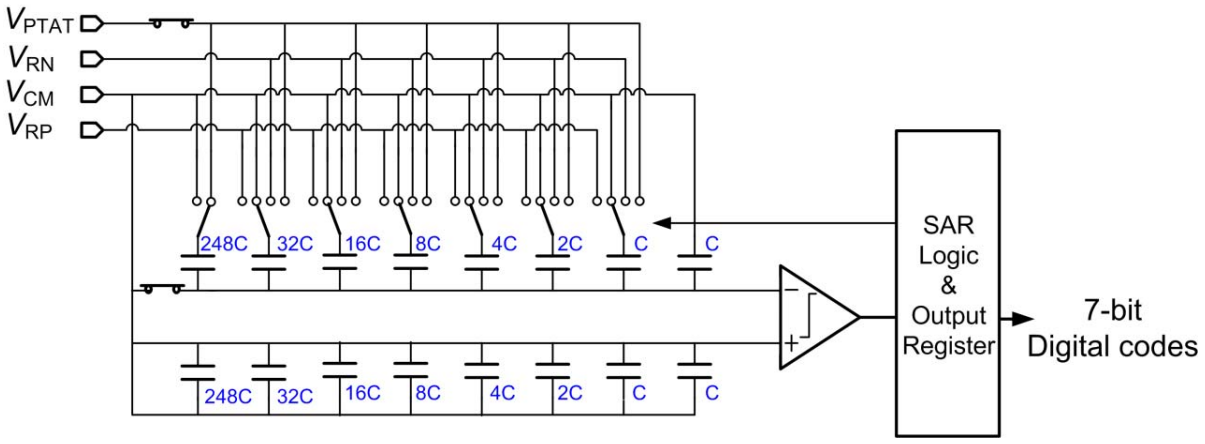

Fig. 5. 7-bit asynchronous SAR ADC structure.

ratio I_{Q1}:I_{Q2} is 8:1. N is thus 64, and the variation of ΔV_{EB} is only 36.3 mV from 0 to 100 °C. An amplifying stage is thus utilized, and the single-ended output of the amplifying stage V_{PTAT} is:

$$V_{PTAT} = \Delta V_{EB} \cdot \frac{R_2}{R_1} \tag{3}$$

where R_2/R_1 is the voltage gain of the amplifying stage. The choice of the voltage gain must meet two criteria: 1) the voltage range of V_{PTAT} must meet the input range of the SAR ADC and 2) the equivalent voltage resolution must be available for the SAR ADC. R_2/R_1 is set to 4.4 in this work. After the amplifying, V_{PTAT} has a voltage variation of 160 mV in the temperature range, and the equivalent voltage resolution is 1.6 mV/LSB. Two unit-gain buffers are used to avoid loading effect since the output impedance of the signal source is quite small.

V_{PTAT} is then quantized with an asynchronous single-ended 7-bit SAR ADC, as shown in Fig. 5. For moderate resolution and conversion rate application, the SAR structure is widely known for its energy efficiency. Furthermore, SAR ADC is an amplifier-free architecture. In other words, SAR ADC does not require high gain and high bandwidth amplifiers, which is necessary in $\Sigma\Delta$ ADCs, to guarantee the linearity. A high-performance amplifier consumes large power, and suffers from short channel effect and low supply voltage in advanced process [19]. The proposed SAR ADC uses asynchronous timing controller to avoid the requirement of a high-speed clock generator [20].

Fig. 6 shows the double-tail dynamic comparator for ADC, which consists of an input stage followed by a regenerative latch stage. The double tail dynamic comparator typically offers less current in the differential input stage to reduce offset and provides a large current in the regenerative latch stage for fast regeneration. The reset operation of the comparator is controlled by a clock signal *CLK* [21]. When the conversion is finished, both the capacitor array and the comparator are reset and wait for the next conversion. Therefore, the comparator has virtually no power dissipation when the comparator is not active. In the advanced processes, the conversion rate of the SAR ADC can easily reach the scale of 10 MS/s. That is,

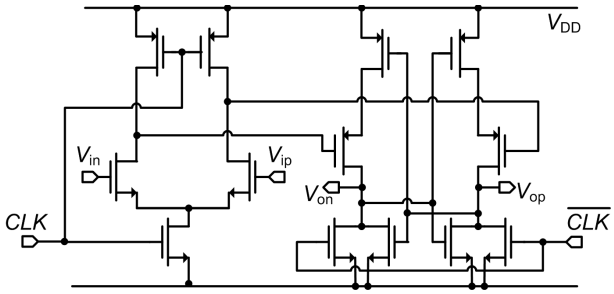

Fig. 6. Two-stage dynamic comparator.

for the temperature sensor whose conversion rate is usually below 100 kS/s, the comparator is switched to the rest mode in the most of the time with the aid of the asynchronous timing control. The reset operation saves the quiescent current of the SAR ADC, and the average power of the P_TS can be reduced.

To fit the 160-mini-volt input range, we need two extra reference voltages for switching. The reference voltage V_{RP}/V_{RN} is equal to the common mode voltage V_{CM} plus/minus 102.4 mV. Providing these two reference voltages would increase the design complexity. In this design, we use the supply voltage and the ground level as the references. A capacitor of 248 capacitance units is added for reference voltage scaling. To reduce the effect of the kickback noise during signal comparison, an identical dummy capacitor array is connected to the non-inverted terminal of the comparator.

For higher resolution application, the area of traditional MIM capacitor array would be made larger to enhance the linearity. However, that would result in the larger capacitor array area. Moreover, the minimum unit capacitor of the MOM capacitor is restricted by the design rule, and the total capacitance C_{total} (312*unit capacitance) at the input terminal would be far larger than the recommended capacitance according to the thermal noise Err_{noise} definition:

$$Err_{noise} = \sqrt{\frac{kT}{C_{total}}} < \frac{1}{2}V_{LSB} \Leftrightarrow C_{total} > \frac{4kT}{V_{LSB}^2} \tag{4}$$

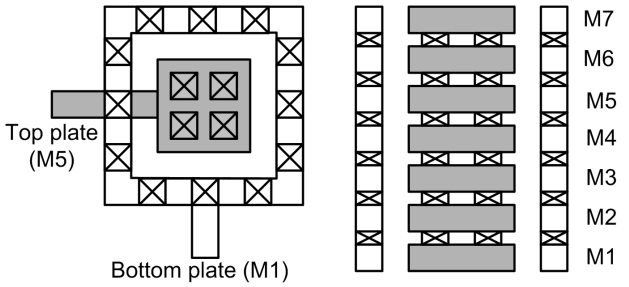

Fig. 7. Three-dimensional MOM capacitor structure.

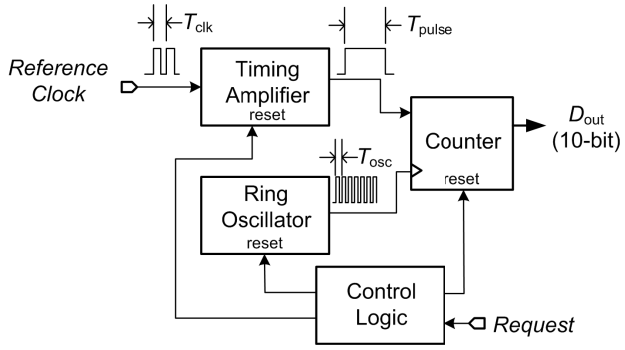

Fig. 8. Block diagram A_TS.

where T is the resistor's absolute temperature in Kelvins. In order to lower capacitive load for the PATA signal voltage buffer and to reduce required current consumption, a metal-oxide-metal (MOM) capacitor structure is adopted for the implementation of the capacitor array [22]. As shown in Fig. 7, the bottom-plate is similar to a frame enclosing the pillared top-plate, and the capacitance is generated by coupling capacitance between metal lines. Hence, the unit capacitance can be changed by adjusting the coupling capacitance. The size of the unit capacitor cell is 1.41*1.41 μm, and the unit capacitance is about 1.5 fF. To prevent inducing error to reference scaling during the signal conversion, the top-plate is shielded by the bottom-plate, so almost no parasitic capacitor is generated at the top-plate node when we forming a capacitor array in which all the top-plates of unit capacitors are connected together. The total input capacitance of the SAR ADC is about 0.94 pF. To reduce the parasitic capacitance of the routing, the binary-weighted capacitor array is laid out based on a one-dimensional matching placement. Moreover, the greatly regular arrangement of unit capacitors further benefits the process matching, and no calibration circuit manipulated in this design.

B. Auxiliary Temperature Sensor

Fig. 8 shows the block diagram of the auxiliary temperature sensor. The temperature-sensitive output clock of the ring oscillator is used to trigger a counter to measure the length of a pulse. Only simple logic gates are used here, and high area efficiency can be expected. We assume square-law behavior for the CMOS devices and thereby ignore the effects of velocity saturation and other non-idealities. The period of the

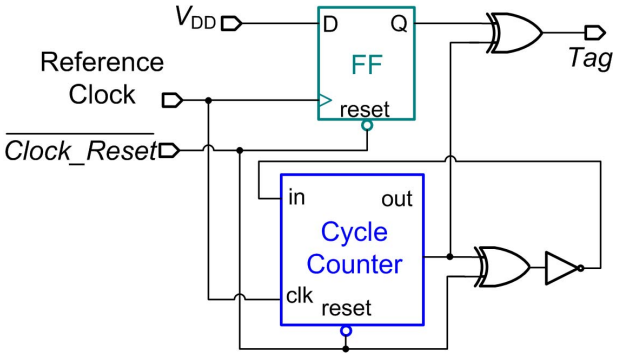

Fig. 9. Block diagram of the timing amplifier.

inverter-based ring oscillator can be derived as

$$T_{osc} = 2 \cdot M \cdot T_P \tag{5}$$

where T_P is the equivalent propagation delay of the inverters, and M is the stage number of the ring oscillator. For an inverter with equivalent NMOS and PMOS, the propagation delay T_P can be derived as

$$\begin{aligned} T_P &= (T_{PLH} + T_{PHL})/2 \\ &= \frac{(L/W)C_L}{\mu C_{ox}(V_{DD} - V_T)} \ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right) \end{aligned} \tag{6}$$

where L, W are the length and width of the MOSFETs, C_L is the effective load capacitance of the inverter, and

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{km}, km = -1.2 \sim -2.0, \tag{7}$$

$$V_T(T) = V_T(T_0) + \alpha(T - T_0), \alpha = -0.5 \sim -3.1\ \text{mv/K}. \tag{8}$$

In the case of V_{DD} much larger than V_T, the thermal effect of the propagation delay will be dominated by the mobility μ. That is, the thermal coefficient of T_P, and thus T_{osc}, will become positive. Because we use the clock signal of the ring oscillator as the clock signal of the counter to measure the length of a constant pulse the output code has a CTAT behavior. The constant pulse is generated with a low-speed reference clock and a timing amplifier, and the structure of the timing amplifier is in the Fig. 9. The output of the timing amplifier *Tag* rises to high level after the reset function is disabled. The reference clock trigger the cycle counter till the counter output is equal to a given parameter k, whose value is 7 in this work, and then *Tag* returns to low level. The pulse width of *Tag* is T_{pulse}:

$$T_{pulse} = k \cdot T_{clk}. \tag{9}$$

When the *Request* signal is activated, the counter starts to count the number of oscillations of the ring oscillator during T_{pulse}. The output code of the A_TS D_{out} is

$$D_{out} = T_{pulse}/T_{osc} = k \cdot T_{clk}/T_{osc}. \tag{10}$$

Because the period variation of the delay cell with temperature is small, a longer pulse width is needed for the resolution of 1 °C/LSB, and more output bits are required to accommodate the longer pulse width. We use a 10-bit counter in this work, and the reference clock has a frequency

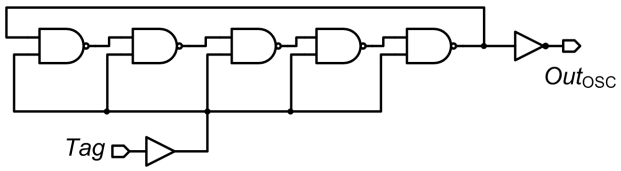

Fig. 10. NAND-gate-based ring oscillator.

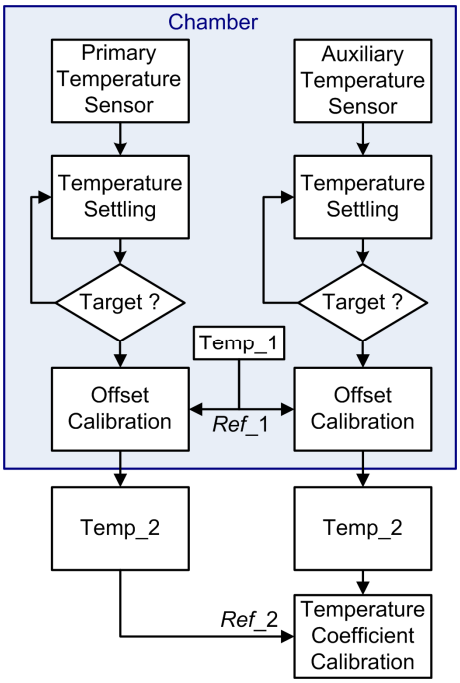

Fig. 11. Flow diagram of the proposed calibration method.

of 10 MHz. The structure of the ring oscillator is shown in the Fig. 10. Instead of inverters, the oscillator is composed of NAND gates. When *Tag* is in high level, the ring oscillator operates as an inverter-based one. After the conversion is over, *Tag* turns off the oscillator. The power consumption of the A_TSs can be further reduced in this way. With the advanced process, the resolution of the A_TS structure increases with the same low-speed reference clock since the propagation delay of the delay cells decreases with the process as well.

IV. Calibration Method

In this work, we propose a temperature sensor calibration strategy, which combines an initial calibration and a subsequent calibration, to guarantee the performance of both the P_TS and A_TSs during the whole lifetime of the system chip. The initial and the subsequent calibration procedures are based on two kinds of feature differences between the P_TS and the A_TSs, and they are described individually in the following.

A. Initial Calibration

The flow diagram of the initial calibration procedure is depicted in Fig. 11. At first, we set all the sensors at a reference temperature Temp_1, which is near the ambient temperature, in a stable environment like a programmable thermal chamber. In this stage, all temperature sensors use external temperature message *Ref*_1 to fulfill the calibration, as Fig. 2 shows. Assume the heat generated by the temperature sensors is negligible, and the chip temperature would be basically equal to Temp_1 after the thermal equilibrium. This temperature message Temp_1 is then used through *Ref*_1(Temp_1) for all temperature sensors, and the offset errors of one temperature sensors D_{offset} can be found:

$$D_{\text{offset}} = Ref\_1(\text{Temp\_1}) - \text{D}_{\text{out}}(\text{Temp\_1}) \tag{11}$$

where D_{out} is the output code of the temperature sensor. For the P_TS, *Ref*_1 is 22+Temp_1, and for the A_TSs, *Ref*_1 is 720 –Temp_1. All temperature sensors, which include the P_TS and A_TSs in the system chip, are one-point calibrated. The offset errors of all the temperature sensors can be eliminated.

The error of the P_TS is mainly contributed by several error sources. The first is the offset errors of the amplifying stage and the comparator, which are caused by the circuit mismatch. This kind of error is signal-independent, and can be seen as a constant error in the individual chip. A simple one-point calibration can compensate these errors. The error due to the infinite gain of the amplifier is the other possible error source. The maximum voltage variation occurs at node V_{PTAT} of the front-end circuit. In the temperature range from 0 to 100 °C, the voltage range of V_{PTAT} is only ±80 mV and is near the output operation point of the amplifier, so the equivalent error or non-linearity is negligible. According to the discussion above, we know that the main error of the P_TS is just offset error, which can be compensated by the previously mentioned one-point calibration. After this simple calibration, because the temperature coefficient of V_{PTAT} is decided by the current density ratio of the BJTs and the resistance ratio of the resistors of the amplifying stage, which suffers more slightly from the process variation compared with the absolute value of the element parameters, the P_TS has a sufficient accuracy without gain error compensation.

On the other hand, a second-point calibration is needed for gain error compensation of the A_TSs. The reason can be found from the discussion of subsection III-B. Since that both the absolute value and the temperature coefficient of the period of the delay cells in the ring oscillator vary with the process spread, there would be offset and gain error in the output codes of the A_TSs. This second-point calibration should be done to the A_TSs at another temperature point near the throttle point for accurate timing for thermal condition warning. Because the output resolution of the A_TSs is about 1 °C per code, the first-order temperature coefficient error E_{TC} of an A_TSs can be found by

$$E_{\text{TC}} = \frac{Ref\_1(\text{Temp\_1}) - \text{Ref\_2}(\text{Temp\_2})}{D'_{\text{out}}(\text{Temp\_1}) - \text{D}'_{\text{out}}(\text{Temp\_2})} \tag{12}$$

where D'_{out}(Temp_1) and D'_{out}(Temp_2) are the output codes of the A_TS after the one-point calibration, *Ref*_1(Temp_1) is the reference code at Temp_1 form external reference, and *Ref*_2(Temp_2) is the reference code at Temp_2 from the P_TS. D'_{out}(Temp_1) is already measured and available. In this stage, the reference thermal message at Temp_2 is calculated

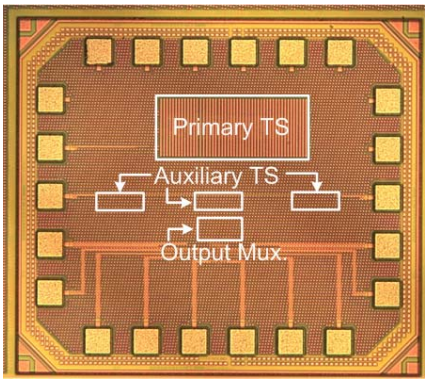

Fig. 12. Chip photo of the primary and auxiliary temperature sensors.

with the aid of the P_TS, which has sufficient accuracy after the calibration at Temp_1. The output codes of the ATSs D''_{out} after the two-point calibration can be derived as:

$$D''_{\text{out}} = (D_{\text{out}} + D_{\text{offset}}) \times E_{\text{TC}} \tag{13}$$

Because the temperature message for the second-point calibration is from the on-chip P_TS, the consistence of the thermal condition of the P_TS and A_TSs can be confirmed. Neither accurate external reference temperature nor a well-control environment for the second-point calibration of the A_TSs is needed for the second-point calibration, and thus it can be just done at a heating plate instead of the programmable thermal chamber. In this way, the calibration cost will be drastically reduced.

B. Subsequent Calibration for A_TSs

The other difference between the P_TS and the A_TSs is the sensitivity to the MOSFET aging. In its whole lifetime, the system chip can keep calibrating the A_TSs with this difference and need no external reference source or tester. For the P_TS, as seen in (2), the temperature signal source is based on the thermal voltage, which suffers little impact from the MOSFET aging. Moreover, in spite of the current through the current sources may vary with time, the current ratio is constant instead. The characteristics of the P_TS mentioned above make it possible to calibrate the A_TSs with the aid of the P_TS. Every time when the whole system start up, or during the wake-up operation procedure after the stand-by state of the system chip, the P_TS can serve as a constant temperature reference for the A_TSs. Due to the N/PBTI effect, the threshold voltage of the MOSFETs in the ring oscillator may differ, and thus T_{OSC} change as well [23]. According to (5), the period error E_{period} is

$$E_{\text{Period}} = \frac{T'_{\text{OSC}}}{T_{\text{OSC}}} \approx \frac{(V_{\text{DD}} - V_{\text{T}})}{(V_{\text{DD}} - V'_{\text{T}})} \tag{14}$$

where V'_{T} is the threshold voltage of the MOSFETs in the ring oscillator after a period of time. Since the temperature coefficient of the A_TSs mainly depends on the mobility of the MOSFET, E_{period} can be seen as another temperature

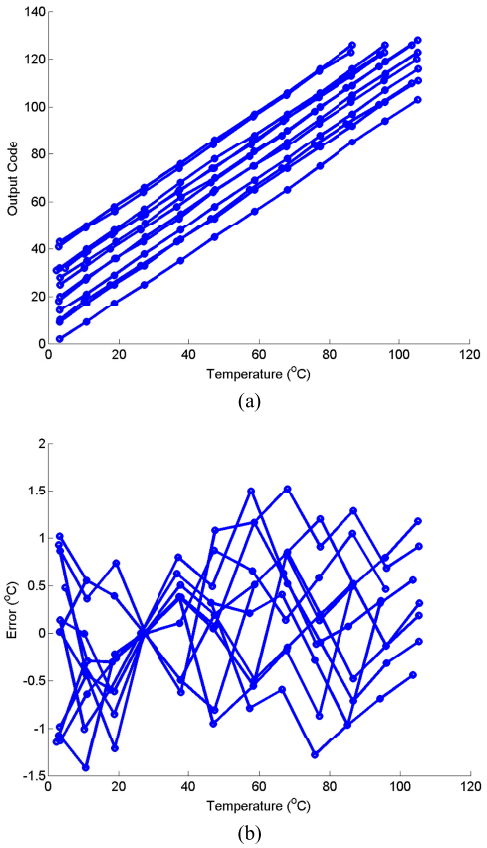

Fig. 13. Measurement results of the primary temperature sensors: (a) original output codes and (b) output errors after the one-point calibration.

coefficient error. At testing temperature Temp_3, we derive E_{period} as

$$E_{\text{Period}} = \frac{k \cdot T_{\text{clk}} / D''_{\text{out}}(\text{Temp\_3})}{k \cdot T_{\text{clk}} / Ref\_2(\text{Temp\_3})} = \frac{Ref\_2(\text{Temp\_3})}{D''_{\text{out}}(\text{Temp\_3})} \tag{15}$$

where D''_{out}(Temp_3) and Ref_2(Temp_3) is the readout and the reference code of the A_TS at Temp_3. After we find E_{period}, the compensated output code D'''_{out} is derived as:

$$\begin{aligned} D'''_{\text{out}} &= D''_{\text{out}} \times E_{\text{Period}} = (D_{\text{out}} + D_{\text{offset}}) \\ &\quad \times E_{\text{TC}} \times E_{\text{Period}} = (D_{\text{out}} + D_{\text{offset}}) \times E_{\text{Total}}. \end{aligned} \tag{16}$$

The subsequent calibration uses the similar technique as the second-point calibration of the initial calibration, so the extra calibration effort can be minimized. The initial and subsequent calibrations guarantee the performance of every temperature sensor in the thermal condition monitoring system during the whole chip life time.

V. Experiment Results

The proposed P_TS and A_TS structures were implemented in the standard 90 nm CMOS process. A chip photograph with floor plan explanation is shown in Fig. 12. One P_TS and three A_TSs are in the chip. The core area of the P_TS is 0.039 mm^2, and that of the ATS is only 0.001 mm^2. The output pins are switched between the P_TS and A_TSs by

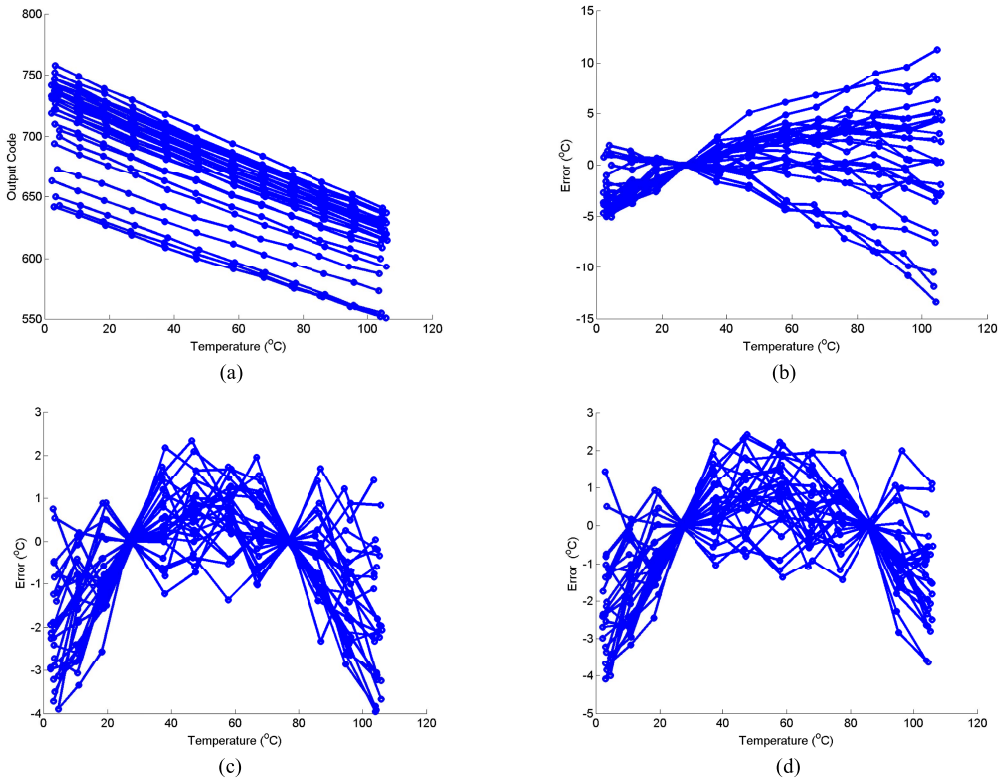

Fig. 14. Measurement results of the auxiliary temperature sensors: (a) original output codes; (b) output errors after the one-point calibration; (c) output errors after the two-point calibration at 30/80 C; and (d) output errors after the two-point calibration at 30/90 °C.

an output multiplexer. From the area difference, we can know that the primary-auxiliary temperature sensing scheme saves much chip area by replacing most P_TSs with the A_TSs. The default supply voltage for all temperature sensors is 1.0 V. The function of the both temperature sensors is fulfilled on-chip, and digital computation during the proposed calibration process is implemented off-chip for flexibility.

Totally 13 samples chips are measured with temperature variations and the output codes of the P_TS are shown in Fig. 13(a). In the ideal case, the output would vary from 22 to 122 in the temperature range from 0 to 100 °C. The resolution of the output code is 1 °C/LSB. The offset errors of the P_TS are in the range of −18 °C to 23 °C. The offset errors of some P_TSs are larger than what we expected, so some theses P_TSs saturate at high temperature point (>80 °C). An 8-bit ADC with the same voltage resolution can easily prevent the saturation due to the offset errors. Because the actual conversion time of the SAR ADC is much shorter than the conversion period of the P_TS, increasing the bit number doesn't affect the operation of the P_TS. After a one-point calibration, the offset errors are eliminated, and the errors at different temperatures are shown in Fig. 13(b). The output error is within −1.4/1.5 °C after the one-point calibration. The power consumption with a 100 kS/s conversion rate is 205.5 μW at 26 °C, and the energy per conversion is 2.06 nJ/S. The power consumption of the SAR ADC is only 30 μW, and the main power consumption is contributed by the front-end circuit. For low-conversion-rate application, we can shut down the front-end circuit when the thermal conversion is fulfilled for higher power efficiency.

Fig. 14(a) displays the output codes of the A_TS before calibration. 27 samples from 13 sample chips are tested for performance verification. In the ideal case, the output code varies from 720 to 620 in the temperature range with a 10 MHz reference clock from 0 to 100 °C. In real measuring environment, however, the output frequency of the ring oscillator is lower than expected. This frequency offset may result from the extra parasitic capacitors at the internal nodes of the ring oscillator. To get a similar output code range, we take an external clock signal whose frequency is 7.5 MHz as the reference of the A_TS. The offset errors of the A_TSs are in the range of −77 to 38. After a one-point calibration, the offset errors are eliminated, and the errors at different temperatures are shown in Fig. 13(b). The output error is within −13.4/11.3 °C after the one-point calibration. Because the temperature coefficients of the curves have differences with process spread, there are still gain errors in the output codes. After the two-point calibration at 30 and 80 °C, the errors at different temperatures are shown in Fig. 13(c). The output errors are within −3.9/2.3 °C after the gain error compensation.

To prove the feasibility of the calibration method proposed in Section III, the other two-point calibration is done at 30 and 90 degree for the ATSs. Fig. 13(d) shows the output errors of the ATSs at different temperatures after the 30/90-°C calibration. The output errors are within −4.1/2.4 °C and just

TABLE I
COMPARISON TABLE

	This work		JSSC 2013 [9]	JSSC 2009 [15]	JSSC 2010 [11]	TCAS-I 2011 [13]
	Analog	Digital				
CMOS Technology	90 nm	90 nm	160 nm	32 nm	350 nm	220/180 nm
Category	Voltage	Time	Voltage	Voltage	Time	Time
Supply voltage	1.0 V	1.0 V	1.5-2.0 V	1.05 V	3.3 V	2.5 V
Resolution	1 °C	1 °C	0.02 °C	<0.45 °C	0.0918 °C	0.133 °C
Error	-1.4/1.5 °C	-3.9/2.3 °C	±0.15 °C (3σ)	< 5 °C	-0.25/0.35 °C (3σ)	-0.7/+0.6
Calibration	1-point	2-point	1-point	1-point	2-point	1-point
Temperature range	0-100 °C	0-100 °C	-55-125 °C	-10-110 °C	0-90 °C	0-100 °C
Power consumption	205.5 μW	13.62 μW	6.8 μW	1.6 mW	36.7 μW	175 μW
Conversion rate	100 kS/s	100 kS/s	188 S/s	1.2 kS/s	2 S/s	4.4 kS/s
Energy per conversion	2.06 nJ/S	0.136 nJ/S	36.17 nJ/S	1.33 μJ/S	18.35 μJ/S	39.77 nJ/S
Core area	0.039 mm^2	0.001 mm^2	0.08 mm^2	0.02 mm^2	0.6 mm^2	N.A.*

*: realized in FPGA

slightly larger than those with the 30/80-°C calibration. This comparison proves that the proposed PTS-aided calibration is available. The power consumption with a 100 kS/s conversion rate is 13.62 μW at 26 °C, and the energy per conversion is only 0.136 nJ/S. The measuring results prove the power efficiency of the A_TS structure and the benefit on the total power consumption of the primary-auxiliary temperature sensing scheme.

Table I lists the performance comparison of the proposed temperature sensors and several existing works [9], [11], [13], [15]. The measurement results and comparison table show that the primary temperature sensor with a SAR ADC occupies small chip area without external digital circuit, and it senses the thermal condition in an energy-efficient manner. The chip area and power consumption of the auxiliary is even more economical. With the proved features of high conversion rate and low energy per conversion, the application field of the proposed sensing scheme can be very wide with proper design strategies. For high performance system chips which have rapid temperature variation, we can increase the conversion rate of the sensors to catch the instant thermal condition. For the portable device application, in which power efficiency is the first priority, the conversion rate can be lowered for higher power efficiency. In the meanwhile, the total producing cost of the temperature sensing system with one primary and multiple area-efficient auxiliary temperature sensors can be drastically reduced. Moreover, the proposed calibration method makes the both temperature sensors have sufficient accuracy for system chip monitoring application after the initial calibration, and the performance of all the sensors can remain with the aid of the simple on-chip subsequent calibration. The proposed primary-auxiliary temperature sensing scheme is thus suitable for multi-block integration application in the SoC system chip.

VI. CONCLUSION

A primary-auxiliary temperature sensing scheme based on the corporation of two kinds of temperature sensors is proposed in this paper for monitoring multiple hotspots in the SoC system chip. An accurate analog primary temperature sensor structure with SRA ADC, which is suitable for advanced process, can serve as an on-chip temperature reference for all the other temperature sensors. A small and low cost auxiliary temperature sensor structure is presented to enhance the fabrication efficiency. Both the temperature sensors are designed in a 90-nm CMOS process. With the proposed calibration scheme, the offset errors of all the temperature sensors and the gain errors of the auxiliary temperature sensors are eliminated, and the performance degration of the auxiliary temperature sensors due to MOSFET aging can be compensated with the propose subsequent calibration as well. The both temperature sensor structures are very power-efficient, and the primary temperature sensor acheives an overall inaccuracy of $-1.4/1.5$ °C after a one-point calibration. The auxiliry temperature sensor acheives an overall inaccuracy of $-3.9/2.3$ °C after a two-point calibration. With the proposed sensing scheme composed of one primary and multiple auxiliary temperature sensors, all the hotspots in a highly integrated system chip can be monitored with a small area and low power consumption.

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