INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2014
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.2014

A capacitance-ratio quantification design for linearity test in differential top-plate sampling sar ADCS

An-Sheng Chao[1,*,†], Cheng-Wu Lin[1], Hsin-Wen Ting[2] and Soon-Jyh Chang[1]

[1]*Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan*
[2]*Department of Electronics Engineering, National Kaohsiung University of Applied Sciences, Kaohsiung, Taiwan*

SUMMARY

Successive approximation register (SAR) analog-to-digital converters (ADCs) are widely used due to their low power consumption and area cost. However, testing SAR ADCs on an embedded chip is costly. This paper proposes a capacitance-ratio quantification design for the linearity test of differential top-plate sampling SAR ADCs. First, the pattern generator controls the switches connected to the bottom plate of capacitors to create a voltage difference proportional to a certain capacitance ratio on the top plates to be quantified. Then, the proposed mechanism quantifies the capacitance ratio via the auxiliary transistors connected to the input pair of the comparator in the SAR ADC. The capacitance ratios are recorded to construct the differential nonlinearity (DNL) and integral nonlinearity (INL) using the derived construction principles, which simplifies the implementation of the output response analyzer. Thus, the test time and area cost can be reduced with these two proposed mechanisms. For characterizing the DNL, the error between the results obtained using the proposed method and those obtained using conventional linear ramp histogram method is from −0.10 to 0.11 least significant bits (LSBs). For the INL, the estimation error is from −0.19 to 0.11 LSBs. Moreover, a test time reduction of about 76% is achieved at the expense of an 18.54% area overhead for the capacitance-ratio quantification mechanism. Copyright © 2014 John Wiley & Sons, Ltd.

Received 11 March 2014; Revised 20 May 2014; Accepted 15 July 2014

KEY WORDS: differential nonlinearity (DNL); integral nonlinearity (INL); successive approximation register (SAR) analog-to-digital converter (ADC)

1. INTRODUCTION

With advances in CMOS technology, successive approximation register (SAR) analog-to-digital converters (ADCs) have received attention due to their excellent power efficiency and low-voltage potential [1] compared to those of pipeline and cyclic ADCs. Thus, SAR ADCs are widely adopted in many applications, such as biomedical monitoring and power management [2–5]. In these applications, SAR ADCs are often integrated with other components, such as pre-amplifiers, multiplexers, filtering circuits, and digital circuits for post signal processing, in a system-on-chip (SoC) environment. Researchers have attempted to further reduce the power consumption of SAR ADCs to increase the energy efficiency of SoCs. Various architectures and switching techniques have been proposed to reduce the power consumption of SAR ADCs [6–8]. Differential top-plate sampling SAR ADCs have faster conversion rates with lower area overhead and power consumption, achieved by halving the capacitance [7], compared to those of conventional bottom-plate sampling SAR ADCs [6].

SAR ADCs are widely used in SoC environment, and the nonlinearity distorts the differential nonlinearity (DNL), integral nonlinearity (INL), and even the effective number of bits (ENOB) [9].

*Correspondence to: An-Sheng Chao, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan.
†E-mail: sonpp945@sscas.ee.ncku.edu.tw

Copyright © 2014 John Wiley & Sons, Ltd.

For example, SAR ADCs are used inside the 3-D imager, and the linearity of the SAR ADCs dominates the performance of the imager [10]. The linearity of the SAR ADCs should be verified in the pre- and post-bond stages [10]. However, verifying the linearity of SAR ADCs in SoC environment is difficult due to the limited accessibility, observability, and pin count. In practical ADC testing task with automatic test equipment (ATE), the test time for static linearity test is even as large as 88% of the whole test time [11]. Moreover, in typical SoCs, analog circuits make up a small portion but require a lot test costs and test time [11]. Thus, reducing linearity test time can reduce testing cost effectively. Analog design-for-testability (DfT) circuits and built-in self-test (BIST) designs are likely adopted to reduce SoC testing costs.

Several works have shown techniques for alleviating these problems. The loopback architecture consisting of an ADC and a digital-to-analog converter (DAC) has been used to verify the linearity of the ADC by scaling and offsetting the DAC output [12]. This technique is not viable for some applications due to the lack of a current-steering DAC. Selective code measurement reduces the test time by measuring only some selective codes. This method requires a programmable piece-wise linear ramp stimulus, which is provided by the off-chip automatic test equipment (ATE) [13, 14]. Nevertheless, the implementation of the on-chip piecewise linear ramp is costly. A SAR DfT circuit reduces internal steps from 10 to 4 for halving the test time [11]. This DfT circuit still requires the linear ramp stimulus. Another technique measures the major carrier transitions (MCTs) of the capacitor-based DAC to estimate the linearity of SAR ADCs to reduce test time [15]. This method is only suitable for single-ended SAR ADCs since the additional design-for-testability DAC (d-DAC) is connected to the negative input terminal of the comparator as a small-swing stimulus. This technique was further improved [16] for applications to differential bottom-plate sampling SAR ADCs by connecting the d-DAC to the dummy capacitor of the capacitor array in the SAR ADC. However, the capacitance of the dummy capacitor in the SAR ADC must be enlarged to cover all MCT ranges, which may complicate the layout of the capacitor array.

The present study proposes an on-chip linearity test for differential top-plate sampling SAR ADCs that uses two mechanisms. In the first mechanism, the capacitor-ratio quantification circuit quantifies the capacitance ratios. Then, the DNL and INL are estimated by the quantified capacitance ratios. According to a previous study [17], the linearity of SAR ADCs is dominated by the capacitor mismatch error in the capacitor array. Thus, a self-calibrating dynamic comparator [18] is augmented to quantify the capacitance ratios in the capacitor-based DAC in SAR ADCs. Then, the quantified capacitance ratios are extended to construct the DNL and INL based on the derived mapping rule, which is different from those in conventional differential bottom-plate sampling SAR ADCs. These two simple mechanisms greatly reduce the required test time compared to that of the conventional linear ramp histogram method [19].

The rest of this paper is organized as follows. Section 2 introduces the concepts of the proposed linearity testing method. The considerations of the hardware implementation of the proposed method are discussed in Section 3. Simulation results that verify the viability of the proposed testing method are shown in Section 4. Finally, conclusions are made in Section 5.

2. OVERVIEW OF PROPOSED TESTING METHOD

The concepts of the two proposed mechanisms are detailed in this section, including the relation between the capacitance ratios and the DNL and the modification of a self-calibrating dynamic comparator for quantifying the capacitance ratios in SAR ADCs. Then, the proposed architecture is detailed. The construction of the DNL based on the capacitance ratios is also introduced.

2.1. Relation between capacitance ratios and DNL

The relation between capacitance ratios and the DNL varies with SAR ADC structures. Three basic SAR ADC structures are shown in Figure 1. Various structures have been developed based on these three architectures [2–8].

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

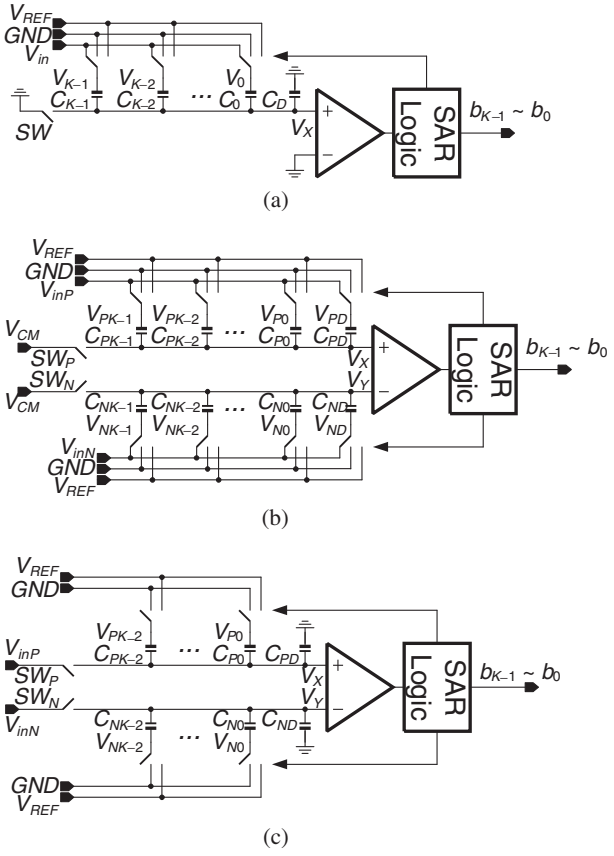

Figure 1. (a) Conventional single-ended SAR ADC, (b) differential bottom-plate sampling SAR ADC, (c) differential top-plate sampling SAR ADC.

The conventional K-bit single-ended bottom-plate sampling SAR ADC [20], which includes a binary-weighted capacitor array, a comparator, and a SAR logic circuit, is shown in Figure 1(a). The thick (thin) line of the capacitor represents the bottom (top) plate. Every analog-to-digital conversion contains three steps: sample, hold, and bit cycling. In the sample step, all the bottom plates of the capacitors are connected to input voltage V_{in}, and all the top plates are connected to *GND* through the switch *SW*. Thus, the input voltage is sampled in the capacitor array. Next, in the hold step, the switch *SW* is open, and all the bottom plates are connected to *GND*. The voltage on the top plates is $V_X = -V_{in}$. In the bit cycling step, the voltage V_{K-1} changes to the reference voltage V_{REF}, and:

$$V_X = -V_{in} + \frac{C_{K-1}}{C_{total}} V_{REF} = -V_{in} + \frac{1}{2} V_{REF} \tag{1}$$

where $C_{total} = 2^K C_D = 2^K C_0$. The capacitance ratio related to C_{K-1} is defined as $(C_{K-1} / C_{total})V_{REF}$. If V_X is negative, V_{K-1} is left connected to V_{REF} and the first output bit b_{K-1} is logical 1. Otherwise, V_{K-1} is connected to *GND* and b_{K-1} is logical 0. This operation repeats K times until the end of one conversion.

From the above conversion method, the transition voltages of the single-ended bottom-plate sampling SAR ADC can be expressed as:

$$V_{THSB}(i)|_{i=0,\cdots,2^K-1} = \frac{b_{K-1}[i]C_{K-1} + b_{K-2}[i]C_{K-2} + \cdots + b_0[i]C_0}{C_{total}} V_{REF} = \frac{\sum_{j=0}^{K-1} b_j[i]C_j}{C_{total}} V_{REF} \tag{2}$$

where the digital output code $i = 2^{K-1}b_{K-1}[i] + 2^{K-2}b_{K-2}[i] + \ldots + 2^0 b_0[i]$ and $b_{K-1}[i]$ … $b_0[i]$ are binary bits. This equation implies that a certain output code maps to a unique capacitance ratio in a single-ended SAR ADC.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

The differential bottom-plate sampling SAR ADC is shown in Figure 1(b) [7]. Every conversion still needs three steps: sample, hold, and bit cycling. The operation is similar to that of the single-ended bottom-plate sampling SAR ADC, but in the bit cycling step, the capacitor switching is complement on the positive and negative capacitor arrays. If voltage $V_{PK\text{-}1}$ changes from voltage V_{REF} to ground *GND*, voltage $V_{NK\text{-}1}$ changes from ground *GND* to voltage V_{REF}. If voltage $V_{PK\text{-}1}$ changes from ground *GND* to voltage V_{REF}, voltage $V_{NK\text{-}1}$ changes from voltage V_{REF} to ground *GND*. Every capacitor pair ($C_{PK\text{-}1}$-$C_{NK\text{-}1}$, $C_{PK\text{-}2}$-$C_{NK\text{-}2}$, …, C_{P0}-C_{N0}, and C_{PD}-C_{ND}) operates in the same manner. Hence, the transition voltage of the differential bottom-plate sampling SAR ADC is:

$$\begin{aligned} V_{THDB}(i) &= \left(\frac{b_{K-1}[i]C_{PK-1} + \cdots + b_0[i]C_{P0}}{C_{PTDB}} - \frac{\overline{b_{K-1}[i]}C_{NK-1} + \cdots + \overline{b_0[i]}C_{N0}}{C_{NTDB}} \right) V_{REF} \\ &= \left(\frac{\sum_{j=0}^{K-1} b_j[i]C_{Pj}}{C_{PTDB}} - \frac{\sum_{j=0}^{K-1} \overline{b_j[i]}C_{Nj}}{C_{NTDB}} \right) V_{REF} \end{aligned} \tag{3}$$

where $C_{PTDB} = C_{PK-1} + \ldots + C_{P0} + C_{PD}$ and $C_{NTDB} = C_{NK-1} + \ldots + C_{N0} + C_{ND}$. The variable i is the digital output in decimal format and $b_j[i]$ is the jth bit of the digital output code in binary format, where $j = 0, \ldots, K-1$ from the least significant bit (LSB) to the most significant bit (MSB).

The architecture of the differential top-plate sampling SAR ADC is depicted in Figure 1(c) [7]. One distinctive difference between differential top-plate and bottom-plate sampling SAR ADCs is the total capacitance. This difference is due to the different switching mechanisms in these two architectures. In bottom-plate sampling SAR ADCs, one conversion requires three steps, namely sample, hold, and bit cycling, as mentioned above, but that for top-plate sampling SAR ADCs requires only two steps, namely sample and bit cycling. The MSB is obtained from the first comparison result without switching on the bottom plates. If the minimum unit capacitance is C_{min}, i.e. $C_{P0} = C_{N0} = C_{PD} = C_{ND} = C_{min}$, then the total capacitance in the K-bit differential bottom-plate sampling SAR ADC $C_{bot(total)}$ in Figure 1(b) is:

$$\begin{aligned} C_{bot(total)} &= C_{PTDB} + C_{NTDB} = C_{PK-1} + \cdots C_{P0} + C_{PD} + C_{NK-1} + \cdots C_{N0} + C_{ND} \\ &= 2\left(2^{K-1} + \cdots 2^0 + 2^0\right) C_{PD} = 2^{K+1} C_{PD} \end{aligned} . \tag{4}$$

In contrast, the total capacitance in the top-plate sampling SAR ADC $C_{top(total)}$ in Figure 1(c) is:

$$\begin{aligned} C_{top(total)} &= C_{PTDT} + C_{NTDT} = C_{PK-2} + \cdots C_{P0} + C_{PD} + C_{NK-2} + \cdots C_{N0} + C_{ND} \\ &= 2\left(2^{K-2} + \cdots 2^0 + 2^0\right) C_{PD} = 2^K C_{PD} \end{aligned} \tag{5}$$

where $C_{PTDT} = C_{PK-2} + \ldots + C_{P0} + C_{PD}$ and $C_{NTDT} = C_{NK-2} + \ldots + C_{N0} + C_{ND}$. For K-bit binary-weighted SAR ADCs, the total capacitance in top-plate sampling SAR ADCs is one half that of bottom-plate sampling SAR ADCs, as evidenced by comparing (4) and (5). Hence, the conversion rate, switching power, and area overhead of the capacitors are greatly reduced. These properties are favorable for implementing SAR ADCs in a SoC environment. Some previous designs for testability in bottom-plate sampling SAR ADCs [15] should be modified for this capacitor arrangement. The proposed test method implements the linearity test in two steps: (1) quantifying the capacitance ratios and (2) extending the capacitance ratios to estimate the DNL. Thus, the DNL/INL can be verified in a short test time with simple hardware, low area overhead, and small conversion rate degradation.

Due to the halved capacitor array, the transition voltages of the top-plate sampling SAR ADCs are not as regular as the transition voltages in (3). The transition voltages of the K-bit top-plate sampling SAR ADC in Figure 1(c) are shown in Figure 2. The left column shows the analog input range of $V_X - V_Y$ from $-V_{REF}$ to V_{REF}. The middle column shows the digital output of this SAR ADC from 0 to $2^K - 1$ in binary format. The right column shows the transition voltages $V_{THDT}(i)$, $i = 0, \ldots, 2^K - 1$,

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

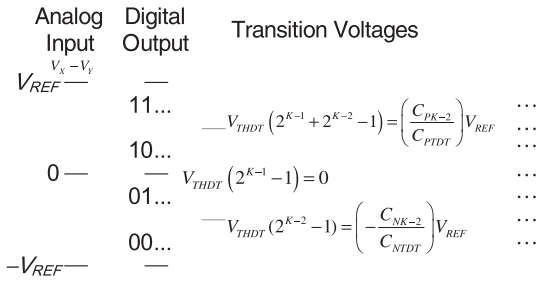

Figure 2. Relation between capacitance ratio and transition voltage.

between consecutive two digital codes. Using a previously developed algorithm [7], the MSB is observed by comparing two sampled voltages, namely V_X and V_Y. If $V_X > V_Y$, the MSB is logical 1. Otherwise, the MSB is logical 0. Thus, $V_X - V_Y = 0$ is the transition voltage for code $2^{K-1}-1$. If $V_X > V_Y$, the second bit is observed by comparing V_Y and $V_X - (C_{PK-2} / C_{PTDT})V_{REF}$. Hence, the transition voltage $V_{THDT}(2^{N-1}+2^{N-2}-1)$ is $(C_{PK-2} / C_{PTDT})V_{REF}$. With a similar operation, $V_{THDT}(2^{N-2}-1)$ is $(C_{NK-2} / C_{NTDT})V_{REF}$. Other transition voltages are observed in the same manner. The transition voltages can be defined as:

$$\begin{aligned} V_{THDT}(i) &= \overline{b_{K-1}[i] \oplus b_{K-1}[i+1]} \left(b_{K-1}[i] \frac{C_{PK-2}}{C_{PTDT}} + \overline{b_{K-1}[i]} \frac{C_{NK-2}}{C_{NTDT}} \right) V_{REF} \\ &+ \cdots + \overline{b_1[i] \oplus b_1[i+1]} \left(b_1[i] \frac{C_{P0}}{C_{PTDT}} + \overline{b_1[i]} \frac{C_{N0}}{C_{NTDT}} \right) V_{REF} \end{aligned} \tag{6}$$

The exclusive-NOR (XNOR) operation is used to determine whether a certain capacitance ratio is related to the transition voltage in every term. For the first term, if the value of the XNOR operation $\overline{b_{K-1}[i] \oplus b_{K-1}[i+1]}$ is 1, the capacitance ratio (C_{PK-2}/C_{PTDT}) and (C_{NK-2}/C_{NTDT}) are involved in the calculation of the transition voltage $V_{THDT}(i)$. If the value is 0, the two capacitance ratios are excluded from the calculation. Similarly, if the binary bit $b_{K-1}[i]$ is 1, the capacitance ratio (C_{PK-2}/C_{PTDT}) is related to $V_{THDT}(i)$ and (C_{NK-2}/C_{PTDT}) is not. If the binary bit $b_{K-1}[i]$ is 0, the capacitance ratio (C_{NK-2}/C_{PTDT}) is related to $V_{THDT}(i)$ and (C_{PK-2}/C_{PTDT}) is not. The same rules are applied to the remaining terms.

The DNL is linearly related to the transition voltage difference $W(i)$ of two consecutive transition voltages, which is expressed as:

$$\begin{aligned} W(i) &= V_{THDT}(i) - V_{THDT}(i-1) \\ &= b_{K-1}[i] \cdot \overline{b_{K-2}[i]} \cdots \overline{b_0[i]} \left(\frac{C_{PK-2}}{C_{PTDT}} - \frac{C_{NK-3}}{C_{NTDT}} - \cdots - \frac{C_{N0}}{C_{NTDT}} \right) V_{REF} \\ &+ \overline{b_{K-1}[i]} \cdot b_{K-2}[i] \cdots b_0[i] \left(\frac{C_{NK-2}}{C_{NTDT}} - \frac{C_{PK-3}}{C_{PTDT}} \cdots - \frac{C_{P0}}{C_{PTDT}} \right) V_{REF} + \cdots \\ &+ b_1[i] \cdot \overline{b_0[i]} \left(\frac{C_{P0}}{C_{PTDT}} \right) V_{REF} + \overline{b_1[i]} \cdot b_0[i] \left(\frac{C_{N0}}{C_{NTDT}} \right) V_{REF} \\ &+ b_{K-1}[i] \cdot b_{K-2}[i] \cdots b_0[i] \left(\frac{C_{PD}}{C_{PTDT}} \right) V_{REF} + \overline{b_{K-1}[i]} \cdot \overline{b_{K-2}[i]} \cdots \overline{b_0[i]} \left(\frac{C_{ND}}{C_{NTDT}} \right) V_{REF} \end{aligned} \tag{7}$$

Thus, the average transition voltage difference W_A, differential nonlinearity $DNL(i)$, and integral nonlinearity $INL(i)$ are, respectively, expressed as:

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

$$W_A = \frac{1}{2^K} \sum_{i=0}^{K-1} W(i), \tag{8}$$

$$DNL(i) = \frac{W(i) - W_A}{W_A} = \frac{W(i)}{W_A} - 1, \tag{9}$$

$$INL(i) = \sum_{j=0}^{i} DNL(j). \tag{10}$$

2.2. *Capacitance-ratio quantification*

The low-noise self-calibrating dynamic comparator [18] cancels offset. The offset cancellation mechanism is reviewed briefly below. The low-noise self-calibrating dynamic comparator is augmented to provide the capacitance-ratio quantification mechanism as shown in Figure 3(a). The voltage difference proportional to a certain capacitance ratio is quantified by this augmented mechanism.

The proposed architecture contains a comparator, offset compensation current sources, namely M_{C1} and M_{C2}, and a charge pump circuit. The offset of the comparator is modeled as voltage source V_{offset}. Voltage difference V_N is proportional to a certain capacitance ratio in the capacitor array in the SAR ADC. The offset reduction mechanism is similar to a previously reported offset calibration process [18]. During the offset reduction and capacitance-ratio quantification periods, the signal *Cal* is logical 1. The input switches are disconnected from the input signals (V_{IP}, V_{IN}) and connected to common-mode voltage V_{CM}. In the detailed circuit shown in Figure 3(a), the input pair ($M1$ and $M2$) receives input differential signals (V_{IPD} and V_{IND}). Transistors $M3$, $M4$, and $M5$ are switches

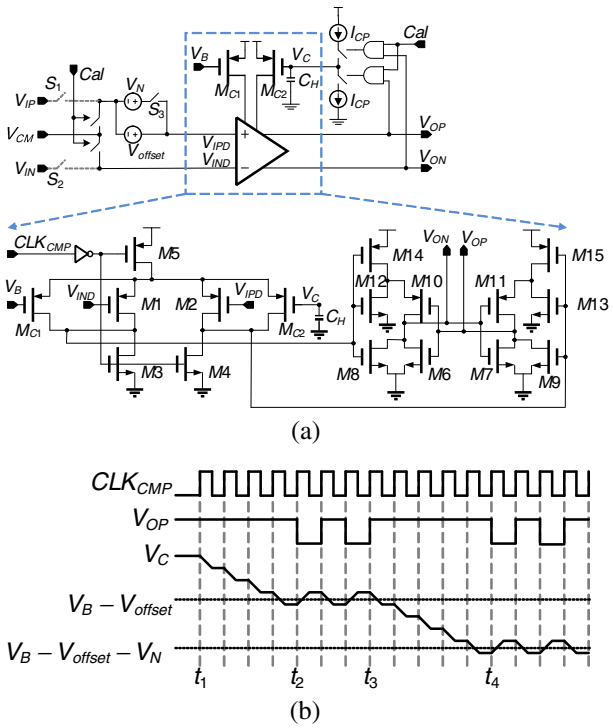

Figure 3. (a) Augmented self-calibrating dynamic comparator for offset reduction and capacitance-ratio quantification, and (b) waveform of offset reduction and capacitance-ratio quantification.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

controlled by clock CLK_{CMP}. The remaining transistors ($M8$–$M15$) are combined to be a latch pair to enhance the output signals (V_{OP} and V_{ON}). Transistors M_{C1} and M_{C2} are connected to the output nodes of the input pair ($M1$ and $M2$) in the comparator to inject the compensation current and are assumed to be ideal and identical to the input pair. The gate of transistor M_{C1} is connected to V_B to set the common-mode voltage of the charge pump circuit. Node V_C connected to load capacitor C_H is initially set to V_B at time t_1 in Figure 3(b), and then the charge pump circuit charges or discharges C_H according to the output of the comparator (V_{OP} and V_{ON}). If V_{offset} is 0, S_3 is disconnected, and $V_{IPD} = V_{IND} = V_B$, then V_C is equal to V_{CM} due to the negative feedback loop (comparator, charge pump, and M_{C2}) and V_{OP} toggles between logical 1 and 0 alternatively. If V_{offset} is positive and switch S_3 is open, the steady state of the negative loop is disturbed, and V_C is adjusted automatically to reach another steady state. In the convergence process, the output V_{OP} is logical 1, and V_C approaches $V_B - V_{offset}$ with an average discharge rate of $\Delta V = I_{CP} \times T_{CMP} / C_H$, where I_{CP} and T_{CMP} are the charging/discharging current and the period of comparator clock CLK_{CMP}, respectively. When V_C equals ($V_B - V_{offset}$) at time t_2, the offset is cancelled, and V_{OP} changes between logical 1 and 0 alternatively. After the offset reduction process, the capacitance-ratio quantification starts, and switch S_3 is closed at time t_3. If voltage difference V_N is positive, the charge pumps toggle again until V_C is below $V_B - V_{offset} - V_N$ at time t_4. With the above operation and by recording the comparator clock count at two time intervals, namely t_1–t_2 and t_3–t_4, offset voltage V_{offset} and V_N can be quantified to be 4 and 5, respectively. These two values are the counts of [$V_{offset}/\Delta V$] and [$V_N/\Delta V$], respectively, where the brackets represent the quantified results. By applying this method to differential SAR ADCs, all of the capacitance ratios can be quantified.

2.3. Built-in self-test architecture

The BIST design supports two operation modes, namely normal and test modes. In normal mode, the SAR ADC, including the comparator, capacitor arrays, and a SAR logic circuit, is activated as shown in Figure 4(a). In test mode, the SAR ADC, quantification unit (QU), pattern generator (PG), and

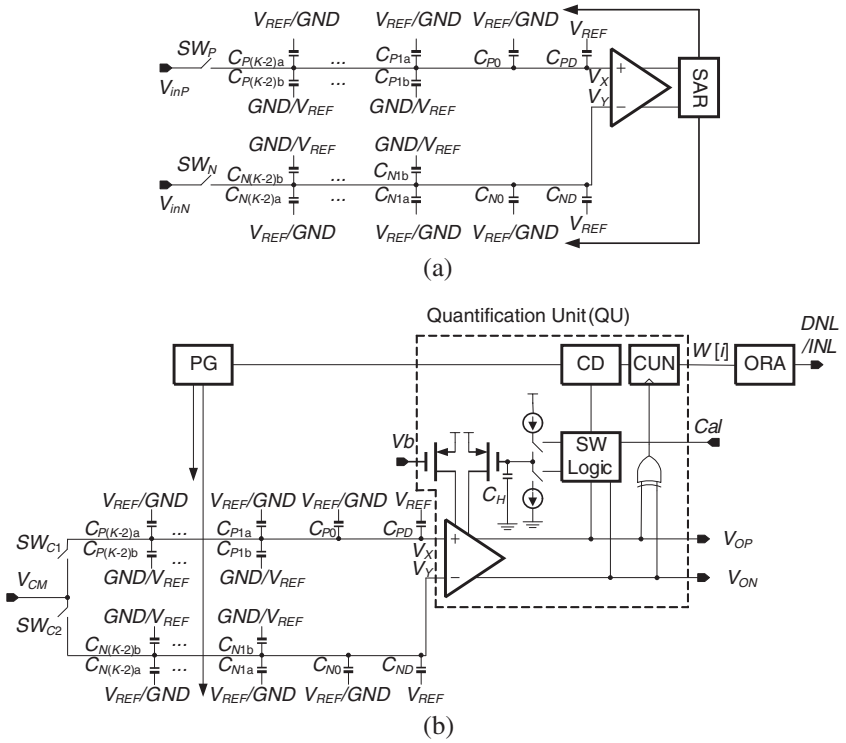

Figure 4. (a) SAR ADC in the normal mode, and (b) the proposed design for testability combined with pattern generator and output response analyzer for a built-in self-test design.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

output response analyzer (ORA) are enabled and all the inputs are connected to common-mode voltage V_{CM} through SW_{C1} and SW_{C2} periodically, as shown in Figure 4(b). The detailed operation is described in Section 2.4.

Switches SW_P, SW_N, SW_{C1}, and SW_{C2} are bootstrapped switches [21] for sampling input signals. The linearity of bootstrapped switches is often higher than the resolution of the SAR ADC to suppress the sampling nonlinearity. Similar to the split-capacitor array [22], every capacitor except C_{P0}, C_{PD}, C_{N0}, and C_{ND} is split into two equal sub-capacitors to perform splitting switching. Capacitors $C_{P(K-2)a}$ and $C_{N(K\text{-}2)b}$ are effectively the MSB capacitor C_{PK-2} in the K-bit top-plate sampling SAR ADC in Figure 1(c). The other split capacitors are effectively the corresponding capacitors in Figure 1(c). With this switching method, the input nodes of the comparator, namely V_X and V_Y, are always near the common-mode voltage during the bit cycling step to reduce the dynamic offset of the comparator [23]. The QU contains the self-calibrating comparator, quantification detector (QD), and counter (CUN). The QD, comparator, and SAR logic circuit are discussed in Section IV.

2.4. DNL estimation from capacitance ratios

According to the ideal analog-to-digital transfer curve [24], the transition voltage difference between successive code transitions should be equal to one LSB, ideally. If the transition voltage is smaller (larger) than one LSB voltage, the code width is linearly less (more) than the average code width. The transition voltages of top-plate sampling SAR ADCs are defined in (7). The transition voltage difference $W(i)$ in (7) also represents the code width in units of voltage. Most of the transition voltage difference $W(i)$ is the combination of several capacitance ratios. For example, in a 3-bit SAR ADC, $W(4) = W_{MCP1} = (C_{P1} \;/\; C_{PTDT} - C_{N0} \;/\; C_{NTDT})V_{REF}$, where W_{MCP1} denotes the transition voltage difference composed by the merged capacitance ratios with leading capacitor C_{P1} (the largest capacitor among the merged capacitors). In the proposed method, every merged capacitance ratio with a certain leading capacitor is unique. The timing diagram in test mode and the switching mechanism for W_{MCP1} in a K-bit SAR ADC BIST design are shown in Figure 5. In Figure 5(c), the conversion rate of the SAR ADC is R times as fast as clock CLK_R, which triggers the PG. The

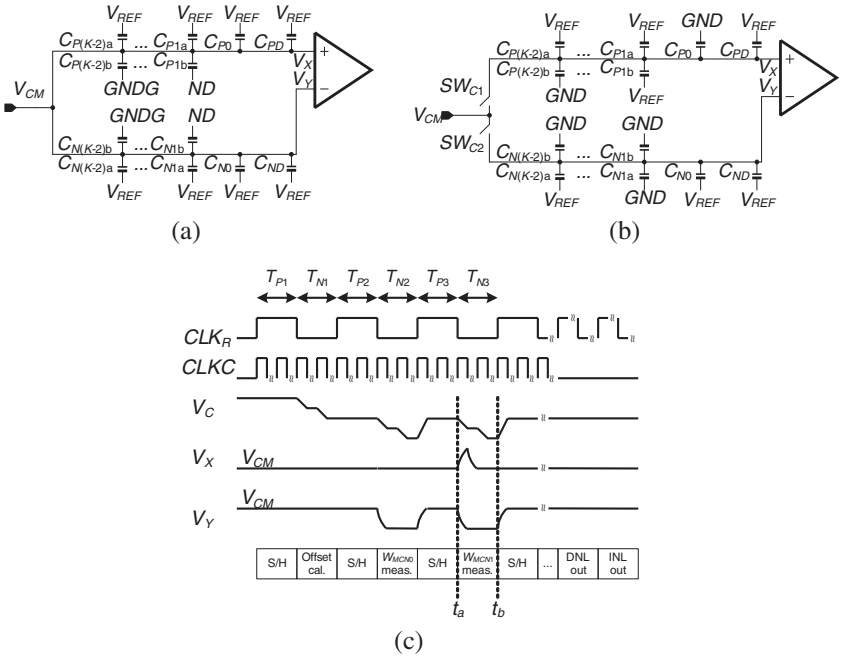

Figure 5. (a) Capacitor setup for sample and hold steps in test mode, (b) capacitor setup for evaluating merged capacitance ratio in measurement phase of test mode, and (c) waveform and timing diagram of the proposed BIST design in test mode.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

comparator is controlled by clock signal *CLKC*, which is often *K*-times faster than the conversion rate of the SAR ADC. The value of *R* is designed to give sufficient time to charge/discharge load capacitor C_H in the QU. Initially, in time intervals T_{P1}, T_{N1}, and T_{P2}, the top plates of the capacitors are all connected to common-mode voltage V_{CM}, and all the bottom plates are connected as shown in Figure 5(a). In time interval T_{N1}, the comparator offset is calibrated. In time interval T_{N2}, the top plates are disconnected from V_{CM}. The bottom plate of C_{N0} is switched from V_{REF} to *GND* and voltage V_Y drops from V_{CM} to $V_{CM} - (C_{N0}/C_{NTDT})V_{REF}$. Then, the QU is activated automatically to quantify the difference W_{N0} as 2. In time interval T_{P3}, the capacitors are reset to sample V_{CM}, as shown in Figure 5(a). In time interval T_{N3}, the top plates are disconnected from V_{CM} again and the capacitor setup is that shown in Figure 5 (b). The bottom plates of C_{N1a} and C_{P0} are switched from V_{REF} to *GND*, and the bottom plate of C_{P1b} is switched from *GND* to V_{REF}. Thus, V_Y changes from V_{CM} to $V_{CM} - (C_{N1} / C_{NTDT} + C_{P0} / C_{PTDT})V_{REF}$ and $V_X - V_Y = (C_{N1} / C_{NTDT} - C_{P0} / C_{PTDT})V_{REF}$ is quantified by the QU. Through, other switching mechanism achieves the same voltage difference $V_X - V_Y$, e.g. a switching mechanism letting $V_X = (C_{N1} / C_{NTDT})V_{REF}$ and $V_X = (C_{P0} / C_{PTDT})V_{REF}$. The above setup keeps voltages V_X and V_Y near common-mode voltage V_{CM} to reduce the input common-mode noise. After the merged capacitance ratios are all quantified, the ORA starts to generate the quantified merged capacitance ratio $W[i]$ value of every output digital code i according to (7). Meanwhile, the average of $W[i]$, W_{AVG}, is also calculated and the *DNL*[i] can be evaluated in sequence. In the proposed BIST design, the ORA outputs *W*[i] and W_{AVG} instead of *DNL*[i] for reducing the hardware cost of the floating-point divider in (11). The INL of every digital code *INL*[i] can be expressed as (12). The ORA outputs the value $I[i] = INL[i-1]W_{AVG} + W[i] - W_{AVG} = I[i-1] + W[i] - W_{AVG}$ instead of $INL[i]$. By this method, the hardware is simplified, and some basic checks can be realized, such as the minimum/maximum examination of the DNL/INL. If accurate $DNL[i]$ and $INL[i]$ are required, the on-chip digital signal processor (DSP) or some other arithmetic unit can calculate $(W[i] - W_{AVG})/W_{AVG}$ and $I[i]/W_{AVG}$ for every $DNL[i]$ and $INL[i]$, respectively.

$$DNL[i] = \frac{W[i]}{W_{AVG}} - 1 \tag{11}$$

$$\begin{aligned} INL[i] &= \sum_{j=0}^{i} DNL[j] = \frac{1}{W_{AVG}} \sum_{j=0}^{i} (W[j] - W_{AVG}) \\ &= \begin{cases} \dfrac{1}{W_{AVG}}(I[i-1] + W[i] - W_{AVG}), i > 0 \\ \dfrac{W[i] - W_{AVG}}{W_{AVG}}, i = 0 \end{cases} \end{aligned} \tag{12}$$

3. IMPLEMENTATION OF BUILDING BLOCKS

The DfT circuit for a 10-bit top-plate sampling SAR ADC is primarily composed of the SAR ADC and QU. The DfT circuit, PG, and ORA complete the BIST design. Considerations of these circuit blocks are detailed in this section.

3.1. SAR ADC

The SAR ADC is composed of three main building components, namely the comparator, the capacitor arrays, and the SAR logic circuit. The comparator is introduced in Section 3.2. The capacitor array is implemented using the split-capacitor architecture mentioned in Section 2.3. For the area consideration, minimum unit capacitor C_{min} is implemented using a metal–oxide–metal (MOM) capacitor [7] instead of a metal–insulator–metal (MIM) capacitor. The SAR logic circuit is similar to the digital control circuit proposed in a previous study [7].

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

3.2. Quantification unit

The comparator and quantification detector are depicted in Figure 6. The self-calibrating comparator [18] is augmented as shown in Figure 6(a). The comparator contains a double latch comparator ($M1$-15), compensation transistors (M_{C1} and M_{C2}), and a charge pump circuit. The double latch remains unchanged, and the input pair of the comparator is modified to be p-type transistors to avoid the body effect. The voltage difference between the source and the body of each input transistor ($M1$ and $M2$) is set to be zero by employing a separated N-well layer in the p-substrate CMOS technology. The charge pump is extended to provide two charging paths and two discharging paths. The *Valid* signal is generated to trigger the quantification detector shown in Figure 6(b) and the SAR logic circuit. The quantification detector contains two quantification detector cells (QDCs). One QDC generates the *CUN_EN* signal to define the enable duration of the counter shown in Figure 4(b). The other QDC generates the *RST_EN* signal for resetting the counter.

The detailed voltage waveform on V_C is shown in Figure 6(c). Comparator clock *CLKC* activates and resets the comparator alternatively. The *Valid* signal toggles with a constant phase delay to *CLKC*. Before time t_a, voltage V_C varies slightly. Fine current sources I_{FU} and I_{FD} are designed for compensating the perturbation caused by switching the coarse current sources on and off. In addition, the ratio of fine charging current I_{FU} to fine discharging current I_{FD} is almost 1. At time t_a, the voltage difference ($V_X - V_Y$) increases due to the change of the test pattern, the signal *CUN_EN* enables the counter, and the QU compensates for the difference by decreasing voltage V_C with the coarse charging current I_{CD} until the quantification detector pulls down signal *CUN_EN* at time t_x. The counter records the count of *CLKC* during the positive period of signal *CUN_EN*. Thus, the voltage difference of $V_X - V_Y$ is quantified as 4 in this example. The coarse currents are disabled between times t_x to t_b, and the amplitude of voltage V_C is small. The rising edge of signal CLK_R at

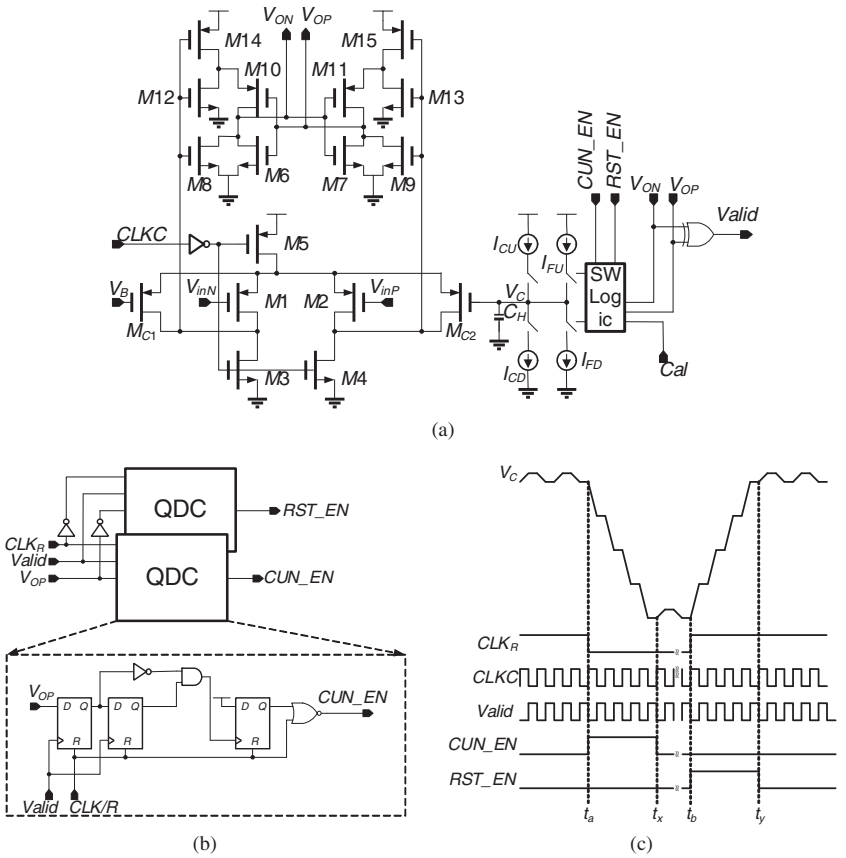

Figure 6. (a) Augmented self-calibrating comparator, (b) quantification detector, and (c) detailed waveform on internal node V_C.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

time t_b resets the QU. Then, voltage V_C goes back to the common-mode voltage via coarse charging current I_{CU} until the falling edge of *RST_EN* at time t_y.

3.3. Pattern generator

The PG for the merged capacitance ratio W_{MCP1} was introduced in Section 2.4. The control signal for every merged capacitance ratio is implemented by a counter and read-only memory due to the complexity of split-capacitor switching. The PG is implemented with 1510 transistors.

3.4. Output response analyzer

The ORA provides two functions: (1) construction of the hit counts for the DNL/INL and (2) generation of pass/fail for the pre-defined DNL/INL boundaries. By extending the quantified merged capacitance ratios according the reconstruction rule in (11), the quantified merged capacitance ratio $W[i]$, which is also the hit count, for every digital code i can be constructed. For a 10-bit SAR ADC, the DNL construction can be implemented by 19 multiplexors (MUXs). The relation in (7) is rewritten in the quantified form as:

$$W[i] = S_{K-1}[i]\left(\frac{C_{NK-2}}{C_{NTDT}} - \cdots - \frac{C_{N0}}{C_{NTDT}}\right)V_{REF} + S'_{K-1}[i]\left(\frac{C_{PK-2}}{C_{PTDT}} - \cdots - \frac{C_{P0}}{C_{PTDT}}\right)V_{REF} + \cdots + S_1[i]\left(\frac{C_{P0}}{C_{PTDT}}\right)V_{REF} + S'_1[i]\left(\frac{C_{N0}}{C_{NTDT}}\right)V_{REF} + S'_0[i]\left(\frac{C_{PD}}{C_{PTDT}}\right)V_{REF} + S_0[i]\left(\frac{C_{ND}}{C_{NTDT}}\right)V_{REF} \tag{13}$$

where $S_j[i]$ is the product of the binary bits in each term in (7), and $S'_j[i]$ is the one's complement of S_j, where $j = 0, \ldots, K-1$. The control signals for MUXs ($S_0[i], \ldots, S_{K-1}[i]$) are as defined in (13). The inputs of the MUXs are 20 quantified merged capacitance ratios, $W_{MCP0} \ldots W_{MCP9}$, $W_{MCN0} \ldots W_{MCN9}$, as mentioned in Section 2.4. Thus, the hit counts $W[i]$, $i = 0, \ldots, 1023$, are constructed after 1024 clock cycles.

The average hit count W_{AVG} is also calculated in the construction process by the shift function in the 16-bit accumulator. The accumulator comprises by 16 D-flip flops (DFFs), 6 full adders (FAs), and 10 half adders (HAs). The constructed hit count $W[i]$ is connected to the lowest 6 bits of the accumulator, and the average hit count is ready at the highest 6 output bits at the end of the construction sequence.

When W_{AVG} is ready, hit count $I[i]$ for the INL is constructed using the relation $I[i] = I[i-1] + W[i] - W_{AVG}$ derived from (12). The bit count of the FA and DFF arrays is increased to 8 bits for the peak-to-peak hit count of the INL. The ORA is implemented with 11934 transistors.

The PG and ORA may be integrated with other digital parts in the SoC environment to reduce the area cost further.

4. SIMULATION RESULTS AND DISCUSSIONS

To verify the feasibility of the proposed capacitance-ratio quantification mechanism, the mechanism was embedded in a 1-V 10-bit 10-MHz top-plate sampling SAR ADC as a DfT circuit.

The algorithm for DNL construction was realized at the transistor level and incorporated into the ORA circuit. The PG and ORA circuits were designed at the transistor level to complete the BIST design in the SoC environment. The area overhead, dynamic performance, and static performance were evaluated.

4.1. Area overhead

The DfT circuit for the 10-bit 1-V 10-MS/s differential top-plate sampling SAR ADC was implemented in the 0.18-μm CMOS technology for the post-layout simulation as shown in Figure 7. The area of every component is listed in Table I. The area of the SAR ADC was estimated by summing the area of two main blocks, namely the analog block ($85 \times 161\ \mu m^2$) and the digital block ($251 \times 328\ \mu m^2$).

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

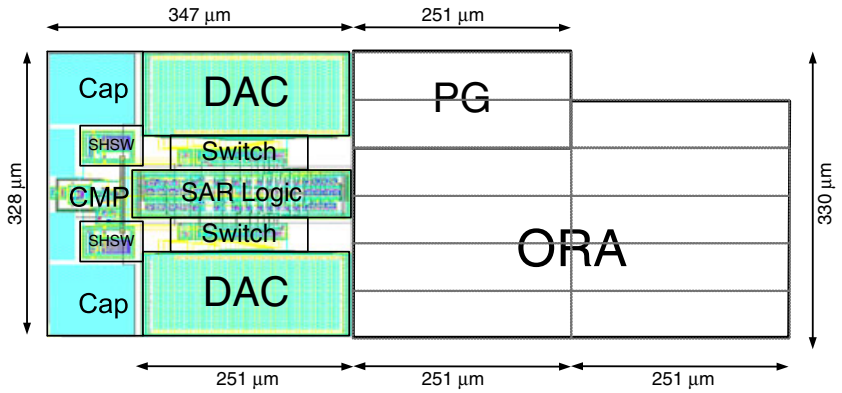

Figure 7. Layout of proposed DfT circuit, PG, and ORA in the proposed BIST design.

Table I. Summary of occupied area.

Component	Area (μm^2)
Bootstrapped switch	$60 \times 38 \times 2$
DAC	$241 \times 101 \times 2$
Switch	$126 \times 20 \times 2$
Comparator	85×58
Comparator with QU	100×328
SAR logic circuit (1366 transistors)	251×55
SAR ADC circuit	$85 \times 161 + 251 \times 328$ (100%)
SAR ADC DfT circuit	347×328 (118.54%)
PG (1510 transistors)	$251 \times 55 \times 2$[a]
ORA (11934 transistors)	$251 \times 55 \times 9$[a]
SAR ADC BIST design	849×330 (295.85%)

[a]Estimated by comparing the transistor count with that of SAR logic circuit.

The analog block contained two bootstrapped switches and a comparator. The digital block included the SAR logic circuit and capacitor arrays. In the DfT circuit, the comparator was combined with the QU. The area of the DfT circuit was $347 \times 328\,\mu m^2$, which is 118.54% the area of the SAR ADC. The PG and ORA were implemented at the transistor level. The areas of the PG (1510 transistors) and ORA (11934 transistors) were estimated by comparing the transistor count with that of the SAR logic circuit (1366 transistors). The area of the SAR logic circuit was used as the area unit ($251 \times 55\,\mu m^2$) for the PG and ORA. The PG is two area units, and the ORA is 9 area units. The area of the BIST design was estimated by combining the areas of the DfT circuit, PG, and ORA as $(347 + 251 + 251) \times (55 \times 6)\,\mu m^2 = 280\,170\,\mu m^2$, as shown in Figure 7. The simulations were performed by the HSpice simulator.

4.2. *Dynamic performance*

The ENOB of the SAR ADC is 9.84 bits at the Nyquist rate. The figure-of-merit (FOM) is 20.46 fJ/conv.-step according to the following equation [7]:

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min(2 \times ERBW, f_s)} \tag{14}$$

where f_s is the conversion rate, and ERBW is the effective resolution bandwidth.

The proposed quantification method has a small impact on the SAR ADC under test. The conversion rate reaches 10 MHz. The area of the proposed DfT circuit is 132.33% that of the SAR ADC in a previous study [25]. That SAR ADC [25] has a capacitor array arrangement similar to that used in this work. The increase of the FOM is mainly due to the modification in the comparator. The other specifications are listed in Table II.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Table II. Specifications of this work.

Technology (nm)	180
Resolution (bit)	10
Supply (V)	1
Conversion rate (MHz)	10
ENOB (bit)	9.84
Area (mm^2)	0.1138
DNL (LSB)	0.10/−0.07
INL (LSB)	0.10/−0.07
FOM (fJ/conversion-step)	20.46

4.3. Static performance for on-chip verification

To verify the feasibility of the proposed BIST design, two testing configurations were used, namely woMisCap and MisCap. In the woMisCap configuration, all the capacitors in the DACs were designed to be binary-weighted for the normal SAR ADCs. To examine the proposed capacitance-ratio quantification method further, an additional capacitor was added to create capacitor mismatch error in the MisCap configuration. The capacitance of the second MSB capacitors (C_{P7a} and C_{N7a}) was increased by minimum capacitance C_{min}, i.e. $C_{P7a} = C_{N7a} = (64+1)C_{min}$, as shown in Figure 8. Besides the mismatch capacitor configuration, supply voltage V_{Mis} of the mismatch capacitors could be adjusted independently. V_{Mis} was set to 0.5 V for the moderate capacitor mismatch environment and to 1 V for the missing code and wide code environment. Thus, three test setups were compared, namely woMisCap, MisCap at $V_{Mis} = 0.5$ V, and MisCap at $V_{Mis} = 1$ V. The linear ramp histogram method [19] and the capacitance-ratio quantification method were compared. The designed hit counts per code in the two methods were both 16 for consistency.

The simulation results for the woMisCap setup are shown in Figure 9. The peak DNL and INL values obtained using the linear ramp histogram method are 0.09/−0.08 LSB and 0.07/−0.10 LSB, respectively, by observing Figure 9(a) and Figure 9(b). The peak DNL and INL values using the capacitance-ratio quantification method are 0.07/−0.06 LSB and 0.09/−0.28 LSB, respectively, by observing Figure 9 (c) and Figure 9(d). The rounded peak DNL error and INL error of the two methods are 0.11/−0.10 LSB and 0.11/−0.19 LSB, respectively, by observing Figure 9(e) and Figure 9(f).

The results for the MisCap setup at $V_{Mis} = 0.5$ V and $V_{Mis} = 1$ V are shown in Figure 10. The peak DNL and INL values obtained using the linear ramp histogram method at $V_{Mis} = 0.5$ V are 0.54/−0.54 LSB and 0.73/−0.75 LSB, respectively, by observing Figure 10(a) and Figure 10(b). Compared to the woMisCap setup, the mismatched capacitor at $V_{Mis} = 0.5$ V enlarges the peak-to-peak DNL swing by roughly ±0.5 LSB. The peak DNL and INL values using the linear ramp histogram method at $V_{Mis} = 1$ V are 1.05/−1 LSB and 1.48/−1.44 LSB, respectively. The peak-to-peak DNL swing is further enlarged by roughly 2 LSB compared to that of the woMisCap setup. This setup was designed for verifying the proposed test method at the boundaries.

The peak DNL and INL values obtained using the capacitance-ratio quantification method at $V_{Mis} = 0.5$ V are 0.53/−0.59 LSB and 0.82/−0.82 LSB, respectively, by observing Figure 10(c) and

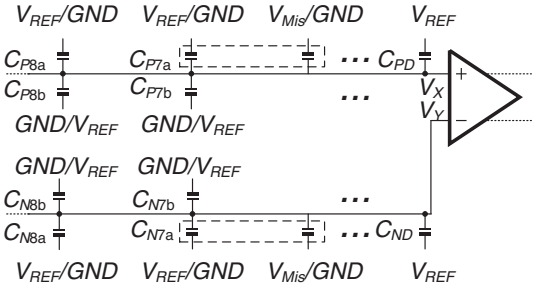

Figure 8. Mismatched capacitor array setup.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

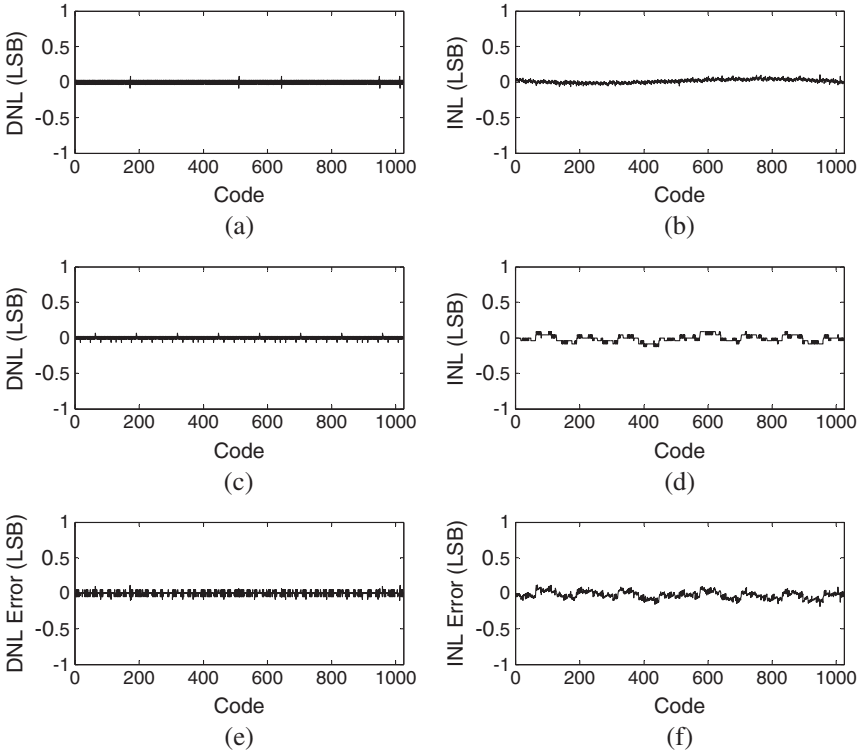

Figure 9. Results for woMisCap configuration. (a) DNL and (b) INL obtained by ramp stimulus. (c) DNL (d) INL obtained by capacitance-ratio quantification. (e) DNL and (f) INL errors between the two test methods.

Figure 10(d). The peak DNL and INL values obtained using the capacitance-ratio quantification method at $V_{Mis} = 1$ V are 0.95/−1 LSB and 1.49/−1.43 LSB, respectively.

The rounded peak DNL error and INL error at $V_{Mis} = 0.5$ V between the two methods are 0.20/−0.15 LSB and 0.25/−0.20 LSB, respectively, by observing Figure 10(e) and Figure 10(f). The rounded peak DNL and INL errors at $V_{Mis} = 1$ V are 0.18/−0.16 LSB and 0.21/−0.17 LSB, respectively, by observing Figure 10(g) and Figure 10(h).

4.4. Static performance with capacitor mismatch at process corners

Process variation may cause capacitor mismatch and transistor variation. The capacitor was implemented by the MOM capacitor [7]. Thus, an accurate statistical model for the capacitor is not available. However, the capacitor mismatch is the dominant factor for the static linearity of SAR ADCs. Because of the random mismatch error, the static linearity of SAR ADCs is often limited to be around 10 bits [17]. Thus, each capacitor in the capacitor array was modeled as a Gaussian random variable with a standard deviation (σ). The value of the standard deviation was estimated as $\sqrt{2^{10}}\sigma = C_{min}$, where C_{min} is the minimum unit capacitor in the 10-bit SAR ADC. The effect of the transistor mismatch was considered by introducing the transistor models at the process corners. Thus, in the post-layout simulation, 20 samples of SAR ADCs with randomly generated capacitance values were simulated for process corners, namely TT, FF, SS, SF, FS at 100 °C, and FF at −40 °C. The results for the linear ramp histogram method [19] and the proposed capacitance-ratio quantification method were compared. The DNL or INL error is the difference of the results between these two methods. The mean values of the DNL errors at 6 corners in the above sequence are 0.0409, −0.0174, 0.0014, −0.0312, 0.0483, and 0.0280 LSB, respectively. The standard deviations of the DNL errors are 0.2359, 0.2314, 0.2259, 0.2232, 0.2285, and 0.2311 LSB, respectively. The mean values of the INL errors are −0.0426, 0.0726, 0.1309, 0.1472, 0.0834, and 0.0553 LSB, respectively. The standard deviations of the INL errors are 0.2745, 0.2937, 0.2812, 0.2276, 0.2920, and 0.2872 LSB, respectively. The worst DNL error and INL error are found at the

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

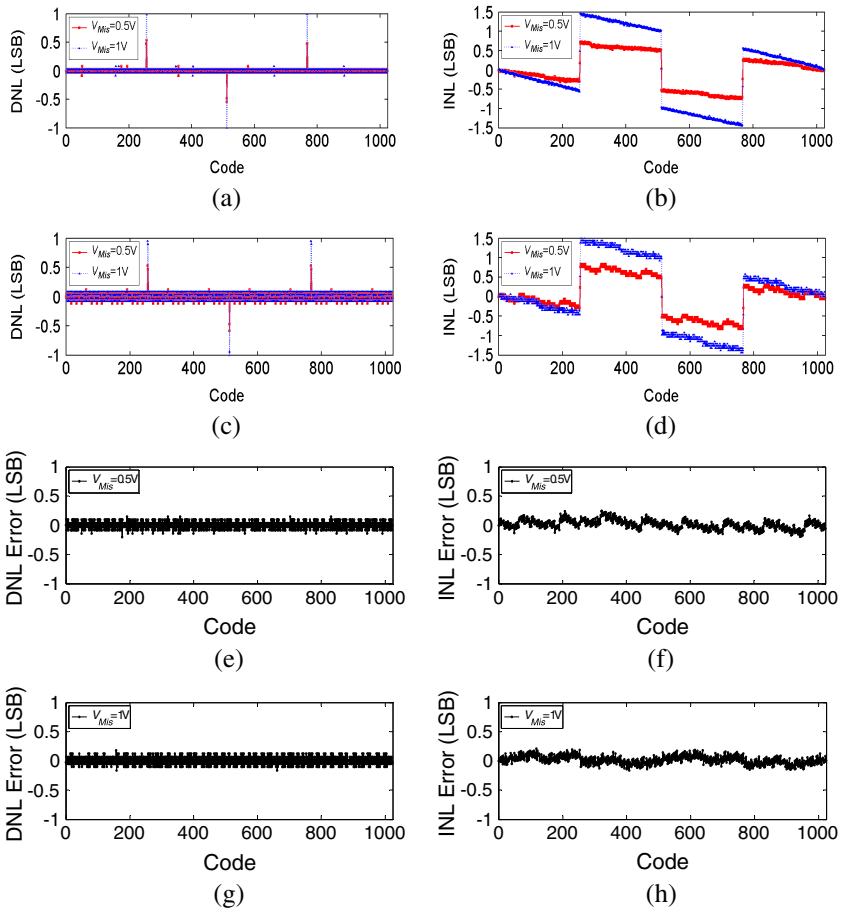

Figure 10. Results for MisCap configuration at $V_{Mis} = 0.5$ V and $V_{Mis} = 1$ V. (a) DNL and (b) INL obtained by ramp stimulus. (c) DNL and (d) INL obtained by capacitance-ratio quantification. (e) DNL and (f) INL errors between the two test methods at $V_{Mis} = 0.5$ V. (g) DNL and (h) INL errors between the two test methods at $V_{Mis} = 1$ V.

SF corner. The DNL error and INL error of every test samples at the SF corner are shown in Figure 11. The maximum DNL and INL errors are −0.5938 LSB and 0.5583 LSB, respectively. The DNL errors of the ninth and nineteenth samples in Figure 11 are larger than others due to the wide codes which is about 1.5 LSB.

The peak-to-peak DNL or INL errors of 20 samples at all corners were also averaged. The average peak-to-peak DNL and INL errors at different corners are similar. The results reveal that the transistor mismatch has minor impact on the DNL and INL errors. The average peak-to-peak DNL and INL errors at corners are from 0.32 to 0.38 LSB and from 0.41 to 0.52 LSB, respectively.

4.5. Comparator offset

The comparator offset may limit the measurement accuracy in some on-chip testing methods. In the proposed BIST design, the self-calibrating dynamic comparator is applied to quantify the capacitance ratios. The comparator offset is reduced at the beginning of the self-test sequence as shown in Figure 5(c). Thus, the impact of the comparator offset is reduced in the proposed BIST design.

4.6. Testable range

The testable range is limited by the test pattern and the QU. When the capacitor mismatch is small and the voltage difference $V_X - V_Y$ in Figure 4(b) is between 0 and 1 LSB, $V_X - V_Y$ can be quantified

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

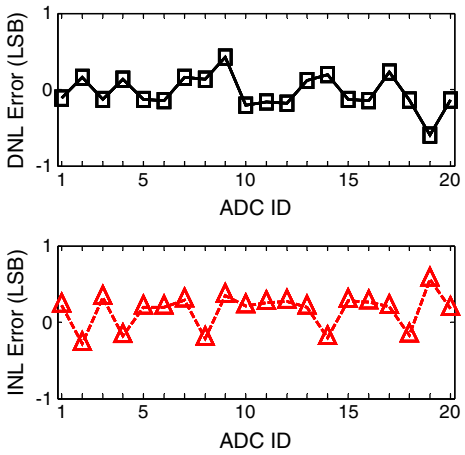

Figure 11. Maximum DNL and INL errors between linear ramp histogram method and proposed capacitance-ratio quantification method at SF corner.

properly and the peak DNL is limited by ±1 LSB. If the voltage difference $V_X - V_Y$ is zero, the peak DNL is ±1 LSB. If the voltage difference $V_X - V_Y$ is less than 0, the quantified value is always zero and great test error occurs. Thus, the testable range for the DNL is ±1 LSB. One special setup should be mentioned here. If the MSB capacitor is greater than the sum of the remaining capacitors in the positive or negative capacitor array by 1 or more LSB, the quantification mechanism still works and the wide code can be observed around code 2^{K-1} or $2^{K-1}-1$ because the voltage difference $V_X - V_Y$ is always greater than zero is this setup.

4.7. Test time estimation

A comparison of the test times of the conventional linear ramp histogram method, the selective code measurement, two designs for testability [11,16], and the proposed capacitance-ratio quantification for the DNL and INL is given in Table III. Here it is assumed that the digital signal processing time is ignored in these methods. For the linear ramp histogram method, every digital output code requires H_{AVG} hits, and every hit consumes clock period T_{CLK}. For the selective code measurement, it is assumed that the maximum INL error should be less than 3 LSBs [11]. Each of the K selective codes needs a 7-LSB ramp stimulus to ensure that the code under test is covered by the ramp, and each code needs H_{AVG} hits. The DfT circuit [11] reduces the amount of the bit cycling step from 10 to 4. Thus, the reduced test time is about 60% of the original test time in the linear ramp histogram method. The above three methods all need $(K+2)$-bit stimulus for a K-bit SAR ADC. The test time of the MCT-based bit-weight extraction technique [16] is $K(S+3)T_{CLK}$, where S is the resolution of the d-DAC. The value of S is 5 for a 10-bit SAR ADC [16].

For the proposed method, $2K$ merged capacitance ratios need to be quantified, each taking R clock periods. Additional R clock periods are preserved for the offset reduction. The test time of the

Table III. Comparison of the test time and stimulus.

Method	Test time	Test time for 10-bit SAR ADC	Stimulus for 10-bit SAR ADC
Linear ramp histogram [19]	$H_{AVG}\times 2^K \times T_{CLK}$	$20\times 1024\times T_{CLK}$	12-bit full-swing linear ramp
Selective code measurement [14]	$H_{AVG}\times 7\times K\times T_{CLK}$	$20\times 7\times 10\times T_{CLK}$	12-bit piecewise linear ramp
The DfT circuit for reducing linearity testing time [11]	$0.4\times H_{AVG}\times 2^K T_{CLK}$	$8\times 1024\times T_{CLK}$	12-bit linear ramp
MCT-based bit-weight extraction technique [16]	$K(S+3)T_{CLK}$	$10\times 8\times T_{CLK}$	Embedded 5-bit d-DAC
Proposed method	$(2K+1)RT_{CLK}$	$21\times 16\times T_{CLK}$	Embedded capacitor switching

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

proposed method is $(2K+1)\times R\times T_{CLK}$ seconds. Table III also lists the test time of three test methods for a 10-bit 10-MHz differential top-plate sampling SAR ADC, with R set to be 16. The test time of the proposed method is reduced by 76% in comparison with the selective code measurement and longer than that of the MCT-based bit-weight extraction technique. The core area overheads are not listed in the two previous designs for testability. The test errors are not compared due to different verification environments and simulators.

According to the test sequence in Figure 5(c), the comparator offset reduction and $2K$ merged capacitance-ratio quantification requires $(2K+1)\times R\times T_{CLK}$ seconds. In the DNL and INL construction steps, each step takes 2^K clock periods. Thus, the test time including construction time is $((2K+1)\,R+2^{K+1})T_{CLK}$ seconds.

5. CONCLUSION

A capacitance-ratio quantification design for the linearity test was proposed and implemented for a differential top-plate sampling SAR ADC. An offset self-calibrating dynamic comparator [18] is augmented to provide the capacitance-ratio quantification function. The derived DNL construction equation is simple and can be implemented on-chip with simple digital components. The proposed quantification and construction method enhances the feasibility of combining a DfT circuit with the PG and ORA for the BIST design in a SoC environment. This testing method requires less test time compared with those for the conventional linear ramp histogram method and the selective code measurement method.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude to the National Chip Implementation Center, Taiwan, R.O.C., for supporting the chip implementation and measurements. This work was supported in part by the grant of NSC-102-2221-E-006-263-MY3 from National Science Council (NSC), Taiwan.

REFERENCES

1. Fan H, Han X, Kobenge SB, Wei Q, Yang H. Design considerations for low power time-mode SAR ADC. *International Journal of Circuit Theory and Applications* 2014; **42**: 707–730.
2. Bonfanti A, Ceravolo M, Zambra G, Gusmeroli R, Borghi T, Spinelli AS, Lacaita AL. A multi-channel low-power IC for neural spike recording with data compression and narrowband 400-MHz MC-FSK wireless transmission. *Proceeding 40th IEEE European Sollid-State Circuits Conference* 2010; 330–333.
3. Huang GY, Chang SJ, Liu CC, Lin YZ. A 1-μm 10-bit 200-KS/s SAR ADC with a bypass window for biomedical applications. *IEEE Journal Solid-State Circuits* 2012; **47**:2783–2795.
4. Chiang CT, Chang WH. A 12-bit multi-channel dual-mode successive approximation ADC for power management bus (Pmbus) devices. *International Journal of Circuit Theory and Applications* 2013; **41**:498–513.
5. Rodriguez-Perez A, Delgado-Restituto M, Medeiro F. Impact of parasitics on even symmetric split-capacitor arrays. *International Journal of Circuit Theory and Applications* 2013; **41**:972–987.
6. Pang WY, Wang CS, Chang YK, Chou NK, Wang CK. A 10-bit 500-KS/s low power SAR ADC with splitting comparator for bio-medical applications. *Proceeding IEEE Asian Solid-State Circuits Conference* 2009:149–152.
7. Liu CC, Chang SJ, Huang GY, Lin YZ. A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal Solid-State Circuits* 2010; **45**:731–740.
8. Guerber J, Venkatram H, Gande M, Waters A, Moon UK. A 10-b ternary SAR ADC with quantization time information utilization. *IEEE Journal Solid-State Circuits* 2012; **47**:2604–2613.
9. Ting HW, Liu BD, Chang SJ. Histogram based testing method for estimating A/D converter performance. *IEEE Transactions on Instrumentation and Measurement* 2008; **57**:420–427.
10. Huang XL, Kang PY, Huang JL, Chou YF, Lee YP, Kwai DM. A pre- and post-bond self-testing and calibration methodology for SAR ADC array in 3-D CMOS imager. *IEEE European Test Symposium* 2011; 39–44.
11. Ogawa T, Kobayashi H, Uemori S, Tan Y, ITO S, Takai N, Yamaguchi TJ, Niitsu K. Design for testability that reduces linearity testing time of SAR ADCs. *IEICE Transactions on Electronics* 2011; **6**:1061–1064.
12. Huang XL, Huang JL. ADC/DAC loopback linearity testing by DAC output offsetting and scaling. *IEEE Transaction on Very Large Scale Integration Systems* 2011; **19**:1765–1774.
13. Goyal S, Chatterjee A, Atia M, Iglehart H, Chen CY, Shenouda B, Khouzam N, Haggag H. Test time reduction of successive approximation register A/D converter by selective code measurement. *Proceeding International Test Conference* 2005; 248–255.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

14. Goyal S, Chatterjee A. Linearity testing of A/D converters using selective code measurement. *Journal Electronic Testing: Theory and Applications* 2008; **24**:567–576.
15. Huang XL, Kang PY, Chang HM, Huang JL, Chou YF, Lee YP, Kwai DM, Wu CW. A self-testing and calibration method for embedded successive approximation register ADC. *Proceeding of Asia and South Pacific Design Automation Conference* 2011; 713–718.
16. Huang XL, Huang JL, Chen HI, Chen CY, Tsai TK, Huang MF, Chou YF, Kwai DM. An MCT-based bit-weight extraction technique for embedded SAR ADC testing and calibration. *Journal Electronic Testing: Theory and Applications* 2012; **28**:705–722.
17. Liu W, Huang P, Chiu Y. A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration. *IEEE Journal Solid-State Circuits* 2011; **46**:2661–2672.
18. Miyahara M, Asada Y, Paik D, Matsuzawa A. A low-noise self-calibrating dynamic comparator for high-speed ADCs. *Proceeding IEEE Asian Solid-State Circuits Conference* 2008; 269–272.
19. Burns M, Roberts GW. An Introduction to Mixed-Signal IC Test and Measurement. Oxford University Press: New York, 2001; 456–457.
20. Johns DA, Martin K. Analog Integrated Circuit Design. Wiley: New York, 1997; 492–498.
21. Abo AM, Gray PR. A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter. *IEEE Journal Solid-State Circuits* 1999; **34**:599–606.
22. Ginsburg BP, Chandrakasan AP. 500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC. *IEEE Journal Solid-State Circuits* 2007; **42**:739–747.
23. Jiang S, Do MA, Yeo KS, Lim WM. An 8-bit 200-MSample/s pipelined ADC with mixed-mode front-end S/H circuit. *IEEE Transactions on Circuits and Systems I: Regular Papers* 2008; **55**:1430–1440.
24. Razavi B. Principles of Data Conversion System Design. IEEE PRESS: New York, 1995; 244–246.
25. Liu CC, Chang SJ, Huang GY, Lin YZ, Huang CM. A 1-V 11fJ/conversion-step 10-bit 10MS/s asynchronous SAR ADC in 0.18 μm CMOS *Symposium on VLSI Circuits/Technical Digest of Technical Papers* 2010; 241–242.

Copyright © 2014 John Wiley & Sons, Ltd.

DOI: 10.1002/cta