IEICE TRANS. ELECTRON., VOL.E97–C, NO.6 JUNE 2014

PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

A Single Opamp Third-Order Low-Distortion Delta-Sigma Modulator with SAR Quantizer Embedded Passive Adder

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SUMMARY A third-order low-distortion delta-sigma modulator (DSM), whose third-order noise-shaping ability is achieved by just a single opamp, is proposed. Since only one amplifier is required in the whole circuit, the designed DSM is very power efficient. To realize the adder in front of quantizer without employing the huge-power opamp, a capacitive passive adder, which is the digital-to-analog converter (DAC) array of a successive-approximation-type quantizer, is used. In addition, the feedback path timing is extended from a nonoverlapping interval for the conventional low-distortion structure to half of the clock period, so that the strict operation timing issue with regard to quantization and the dynamic element matching (DEM) logic operation can be solved. In the proposed DSM structure, the features of the unity-gain signal transfer function (STF) and finite-impulse-response (FIR) noise transfer function (NTF) are still preserved, and thus advantages such as a relaxed opamp slew rate and reduced output swing are also maintained, as with the conventional low-distortion DSM. Moreover, the memory effect in the proposed DSM is analyzed when employing the opamp sharing for integrators. The proposed third-order DSM with a 4-bit SAR ADC as the quantizer is implemented in a 90-nm CMOS process. The post-layout simulations show a 79.8-dB signal-to-noise and distortion ratio (SNDR) in the 1.875-MHz signal bandwidth (OSR=16). The active area of the circuit is 0.35 mm^2 and total power consumption is 2.85 mW, resulting in a figure of merit (FOM) of 95 fJ/conversion-step.

key words: *delta-sigma modulator, DSM, opamp sharing, relaxed dynamic element matching (DEM) timing*

1. Introduction

Due to advances in the CMOS process and reductions in the supply voltage, although the operating speed of digital circuits has been increasing, the design difficulty of analog circuits has also been rising. The use of successive-approximation analog-to-digital converters (SAR ADCs) and delta-sigma modulators (DSMs) is thus becoming more popular, because they have the benefits of less analog circuits. Therefore, SAR ADCs are generally acknowledged as having the most power-efficient ADC structure in medium-resolution (8–10 bits) applications. DSMs have also become more attractive [1]–[5] as the requirements related to resolution and bandwidth in wireless communication continue to increase, since the matching requirement with regard to the analog component does not rise along with the desired resolution. Furthermore, DSMs can achieve a high resolution without the use of digital calibration. In more advanced processes, the transistor impedance is also falling, thus reducing the opamp gain. Compared with other opamp based ADCs, the single-loop DSMs just need a small opamp gain ($> OSR/\pi$) [6], and are more suitable to process evolution. Summarizing these features, DSMs can be seen as a very proper ADC structure that can achieve a high resolution, even with more advanced processes.

A low-distortion DSM [7], whose loop filter processes only the quantization noise component, was developed to reduce the opamp specifications for integrators, although it has the disadvantages of a tight constraint on feedback path timing and the need for either an extra active or passive adder in front of quantizer. An architecture, which allots a half clock cycle from the first integrator for the quantizer and DEM logic circuit in order to mitigate the timing limitation on the feedback path, has been proposed [2]. As a result, the quantizer can adopt other slow-speed or more power efficient ADCs, rather than being confined to flash ADCs.

It is well known that the opamp is the major source of power consumption in a DSM. In general, opamps occupy around 50% to 70% total power of a DSM. Many techniques have thus been proposed to save the number of amplifiers needed for keeping the same NTF or to enhance the noise shaping ability without the use of an extra amplifier. To avoid the use of an extra active adder, i.e. an extra opamp, for a low-distortion DSM, earlier studies [8], [9] remove the summing node from the quantizer input to the last integrator input. Other works [1], [10] respectively propose an integrator structure which can use an opamp to obtain a second-order shaping ability as the function of two cascade integrators. Moreover, the noise-coupling technique [11]–[14] is able to increase the order of NTF without any additional opamp.

Opamp sharing is a common approach for decreasing the amount of amplifier, power, and circuit area. However, sharing the opamp between the former and latter integrator is inefficient in a DSM, since the capacitor size for the latter one can be scaled down and the opamp performance is not completely exploited. Based on this, the work [15] allots distinct timing period to each integrator for realizing a third-order DSM by employing just one amplifier. The first integrator occupies the first half of the clock period; the second and third integrators share the second half one to efficiently exploit the opamp power among all three inte-

Manuscript received September 25, 2013.
Manuscript revised January 30, 2014.

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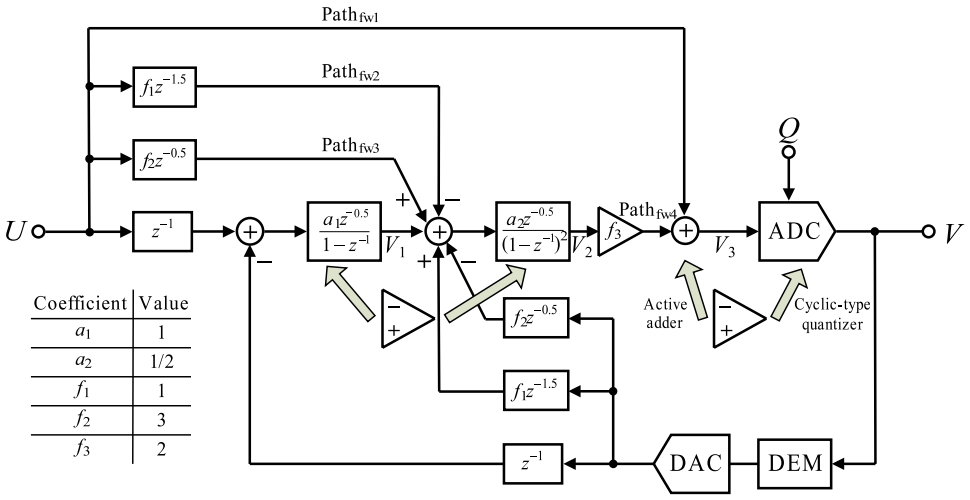
DOI: 10.1587/transele.E97.C.526



Coefficient	Value
a_1	1
a_2	1/2
f_1	1
f_2	3
f_3	2

Fig. 1 Previously proposed third-order low-distortion DSM.

grators. Another low-distortion DSM structure [16], which proposes a new structure to fully utilize the opamp power, which is usually determined by the first integrator, for the second integrator and solves the issue of feedback path timing outlined above. Nevertheless, the opamp power requirement is possibly determined by the second integrator rather than the first one, depending on the quantizer resolution and the unit-capacitor size for the DAC path of the second integrator input. To alleviate this problem, a simplified second integrator architecture is proposed in this work. Besides, some literatures [17], [18] have discussed the memory effect in pipelined ADCs when opamp sharing is used. However, the memory effect has not yet been discussed and analyzed in DSMs. Based on the mentioned above, this work focuses to propose a third-order DSM with minimum number of opamp for significantly reducing power dissipation and analyze the influence from the memory effect in the proposed DSM.

This paper presents a simplified version of the DSM architecture developed in [16], which preserves all advantages of that. The influence of the memory effect on the proposed DSM, caused by the use of opamp sharing, is also explored. In addition, in order to improve the circuit complexity and power consumption of [16], the quantizer is to adopt the embedded passive-adder SAR ADC being similar to the method in [19] and [20]. The rest of this paper is organized as follows. A brief review for the prior art of low-distortion DSM is given in Sect. 2. Simplification steps to get the proposed third-order DSM architecture and the memory effect are then presented and discussed in Sect. 3. Section 4 shows the details of the circuit including the loop filter and the embedded passive-adder SAR ADC, while post-layout simulations are shown in Sect. 5 to confirm the greater power-efficiency of the proposed system. Finally, conclusions of this work are presented in Sect. 6.

2. A Prior Art of Low-Distortion Delta-Sigma Modulator

In a DSM system, any noise and distortion appearing in the latter integrator is suppressed by the former integrator(s) [21], meaning that the capacitor size in the latter can be scaled down. Therefore, when opamp sharing is adopted between the integrators, the opamp power determined by the former integrator is greatly beyond the requirements of the latter, and thus is wasted during the latter integrator operation. Figure 1 shows the signal flow diagram of the previously proposed third-order low-distortion DSM [16], whose coefficients are also shown here. The goal of this work is to efficiently use the opamp power decided by the first integrator for the second one. Compared with a conventional second-order DSM, although the second integrator is more complex in [16], it is equivalent to two cascade integrators, thereby getting a higher order noise shaping for consuming the opamp power in an efficient way. In addition, the timing constraint for the quantizer and DEM is relaxed to half of the clock period. Due to this, a cyclic-type quantizer is utilized, in which the opamp is shared with the active adder in different clock phases.

However, the opamp power requirement of the second integrator may exceed that of the first one, being subject to the number of bits in the quantizer and the unit-capacitor size of the delayed DAC path in front of the second integrator. As the quantizer resolution increases one bit the required amount of thermometer-code DAC unit capacitor will double. In case that the minimum unit-capacitor size is fixed due to process constraints, both the total DAC capacitance and the capacitance of the other SC paths for the second integrator will double if the number of bits in the quantizer is increased by one. This leads to twice requirement of the opamp power.

3. Architecture of Proposed Third-Order DSM

3.1 Block Diagram and Timing Arrangement

As discussed in Sect. 2, the amplifiers specifications may be determined by the second integrator rather than the first one. In this section, we therefore attempt to simplify the DSM structure of Fig. 1, especially the second integrator. The simplified DSM structure also keeps all the advantages, such as low distortion, relaxed feedback path timing, and the third-order noise shaping ability just using two integrators, of the one shown in Fig. 1.

The process of structure simplification can be illus-

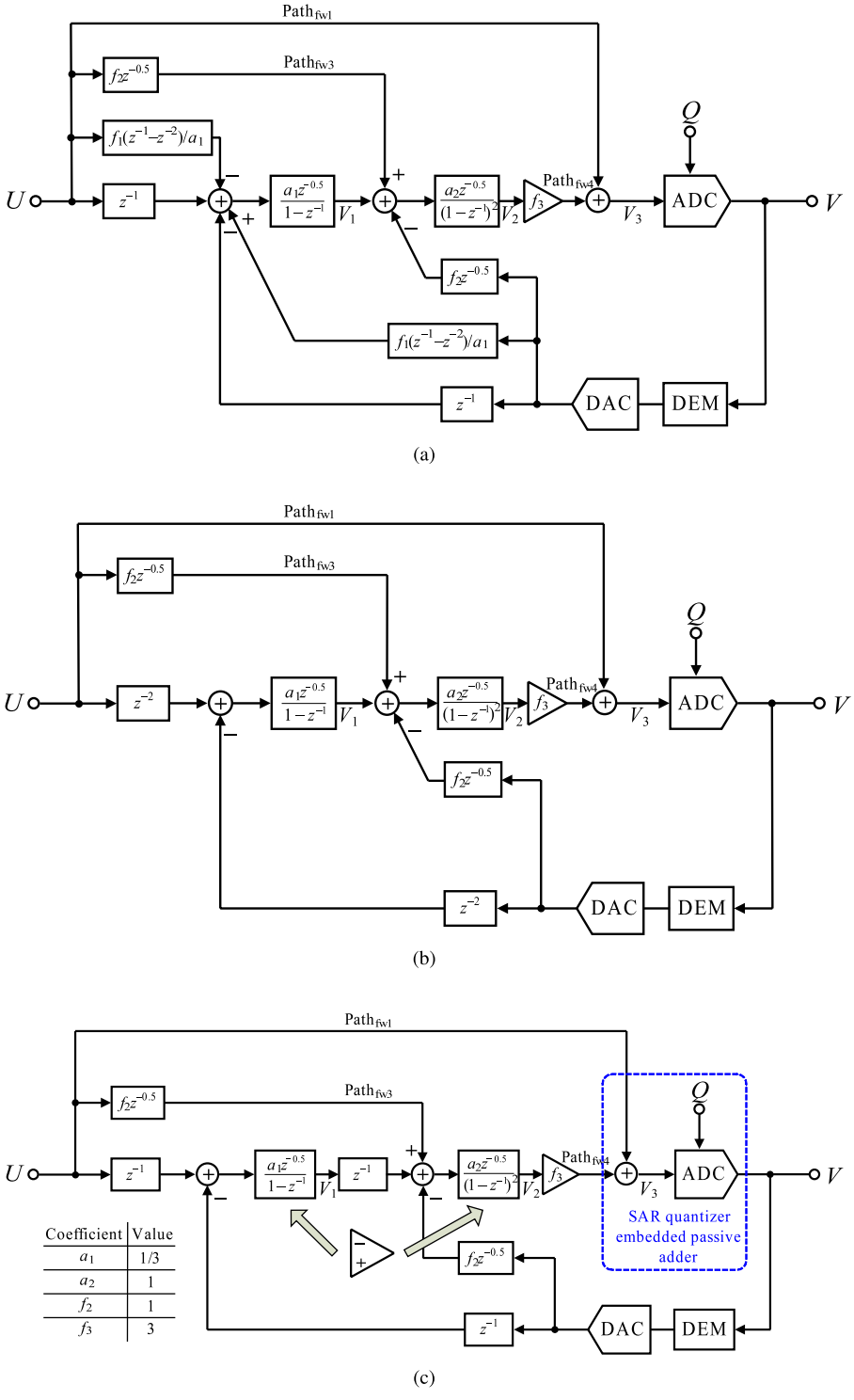
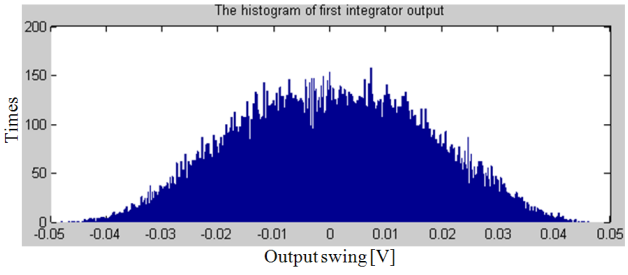


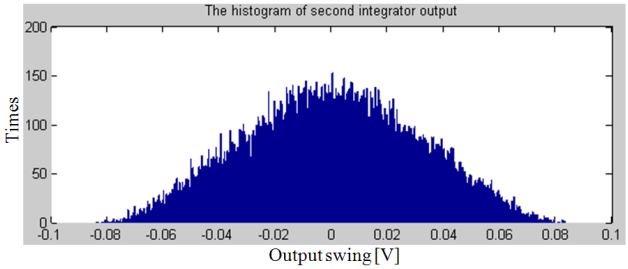
Fig. 2 Steps to acquire the proposed third-order low-distortion DSM.

trated as follow: In Fig. 1, the feedforward and feedback paths with $z^{-1.5}$ for the second integrator are transferred to the front of the first integrator. Dividing these two paths by the transfer function of the first integrator, they become the $f_1(z^{-1} - z^{-2})/a_1$ paths in the front of the first integrator, as shown in Fig. 2(a). As long as designing f_1 equals a_1, the terms of $-U{\cdot}f_1{\cdot}z^{-1}/a_1$ and $U{\cdot}z^{-1}$ can eliminate each other and the terms of $V{\cdot}f_1{\cdot}z^{-1}/a_1$ and $-V{\cdot}z^{-1}$ are also eliminated, as shown in Fig. 2(b). The analog z^{-2} delay has to be carried out in three switched-capacitor (SC) sampling paths with related clock phases [16]. To further simplify the structure, z^{-2} delay is firstly split into two cascade z^{-1} delays. One of z^{-1} delays is moved behind the first integrator. Such an arrangement has the advantage of saving the capacitor area because of the noise shaping from the first one. Figure 2(c) is the complete version of the proposed third-order DSM structure. Compared with that shown in Fig. 1, the proposed architecture simplifies the signal flow path for the second integrator, leading to an increased feedback factor (i.e., a decreased bandwidth requirement for the amplifier) and a decreased circuit area. On the other hand, $STF = 1$ and $NTF = (1 - z^{-1})^3$ are the same as in Fig. 1, so that the two integrators still process only the quantization noise components. The output signals of the integrators are the same as in the previous work [16]. In this paper, we set the first integrator gain, a_1, to 1/3 for further diminishing the output signal swing of the integrators, which is compensated by $f_3 = 3$. Figures 3(a) and (b) show the histograms of the simulated output range of the two integrators in the SIMULINK behavior model for 2^{15} samples. By choosing the above coefficients, the small output signal range of integrators within merely $V_{O,CM} \pm 87.5$ mV, i.e., the opamp output swing, is given in a 1.2-V reference voltage.

Figure 4 illustrates the corresponding timing diagram of the proposed DSM structure (Fig. 2(c)) where C_{fw1} and C_{fw3} mean the capacitors of the input feedforward paths, C_{fw4} is the feedforward capacitor from the second integrator output to the adder, C_{sj} represents the sampling capacitors of the integrators, C_{fj} is the integrating capacitors in the integrator j, and C_{sum} means the capacitor for summing Fig. 2(c)'s $Path_{fw1}$ and $Path_{fw4}$. The first and second integrators alternately carry out the integration in Φ_2 and Φ_1. During Φ_1, the feedforward paths, $Path_{fw1}$ and $Path_{fw4}$, assemble to do the signal summation. Within the whole Φ_2, the summed signal is then quantized and the dynamic element matching circuit (DEM) completes the operation. To further save power consumption, this paper adopts a SAR ADC as the quantizer, which combines the functions of the passive adder and quantization, instead of the cyclic ADC used in the prior work. Details of the SAR ADC will be elaborated later. Therefore, in the overall circuit including the integrators, the adder, and the quantizer, just one amplifier is required to realize the proposed third-order DSM.



(a)



(b)

Fig. 3 Histogram of each integrator's output: (a) first integrator and (b) second integrator.

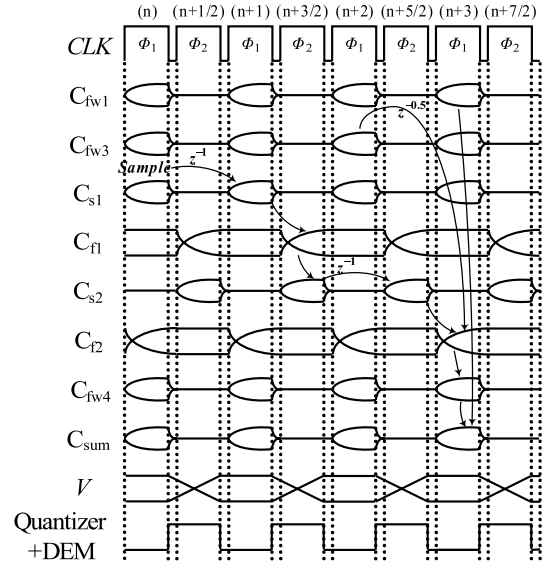


Fig. 4 Timing diagram of proposed third-order low-distortion DSM.

3.2 Exploration of the Opamp-Sharing Memory Effect on the Proposed DSM

Opamp sharing is often adopted in pipelined ADCs for retrenching power consumption and circuit area. However, in such technique there is a residual charge stored on the parasitic capacitance of the opamp inputs since the opamp gain is finite. Then, in the succeeding clock phase, this residual charge will influence the transfer function of the shared stage so that the performance of the ADC is degraded. This is called the memory effect, and this subsection will take

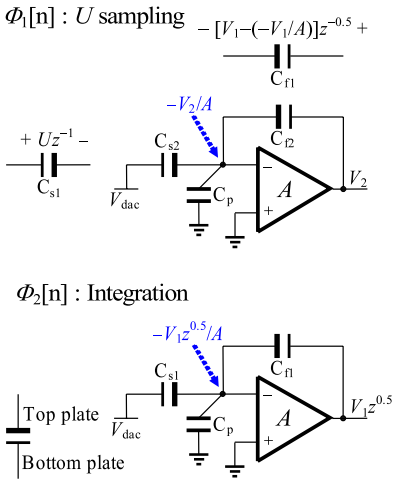


Fig. 5 First integrator configurations between two clock phases.

the memory effect into consideration for the proposed DSM, and show its impact on performance.

Figure 5 shows the first integrator configuration between two clock phases. During $\Phi_1[n]$ in Fig. 5, the second integrator is active while the first integrator is idle, so its integrating capacitor C_{f1}, which stores the integrated signal $[V_1 - (-V_1/A)]$ at the end of $\Phi_2[n-1]$, and the sampling capacitor C_{s1}, which stores the sampled input signal U at the end of $\Phi_1[n-1]$ for completing the z^{-1} delay in the modulator input, are floating. Note that during $\Phi_1[n]$, another sampling capacitor C_{s1}, which is not shown for simplification, is utilized to sample the input signal. The detailed circuit diagram of the first and second integrators is shown in Fig. 10. Considering the residual charge stored on the opamp input parasitic capacitance C_p and the finite opamp gain A, and applying the charge conservation law between $\Phi_1[n]$ and $\Phi_2[n]$, as illustrated in Fig. 5, the transfer function of the first integrator can be derived, as shown in Eq. (1).

$$\begin{aligned} &C_{s1}Uz^{-1} + C_{f1}\left(V_1 z^{-0.5} - \left(-\frac{V_1 z^{-0.5}}{A}\right)\right) + C_p\left(0 - \left(-\frac{V_2}{A}\right)\right) \\ &= C_{s1}\left(V_{dac}z^{-1} - \left(-\frac{V_1 z^{0.5}}{A}\right)\right) + C_{f1}\left(V_1 z^{0.5} - \left(-\frac{V_1 z^{0.5}}{A}\right)\right) \\ &\quad + C_p\left(0 - \left(-\frac{V_1 z^{0.5}}{A}\right)\right) \end{aligned} \tag{1}$$

By rearranging Eq. (1), the first integrator transfer function becomes:

$$\frac{V_1}{U - V_{dac}} = \frac{C_{s1}}{C_{f1}} z^{-1} \frac{C_{f1}A}{C_{f1}(A+1) + C_{s1} + C_p} \frac{z^{-0.5}}{1 - \frac{C_{f1}(A+1)}{C_{f1}(A+1)+C_{s1}+C_p} z^{-1}} \tag{2}$$

However, in addition to Eq. (2), there is an additional transfer function of V_1/V_2, which results from the V_2 component stored on C_p, as shown in Eq. (3).

$$\frac{V_1}{V_2} = \frac{C_p}{C_{f1}A} \frac{C_{f1}A}{C_{f1}(A+1) + C_{s1} + C_p} \frac{z^{-0.5}}{1 - \frac{C_{f1}(A+1)}{C_{f1}(A+1)+C_{s1}+C_p} z^{-1}} \tag{3}$$

The second term in Eq. (2) and Eq. (3) is the gain error, while the third term is the real integrator transfer function. Both

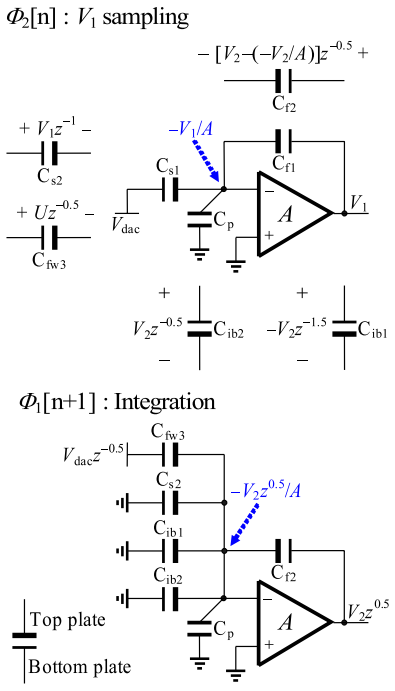


Fig. 6 Second integrator configurations between two clock phases.

terms include C_p, which is due to the remaining V_1 component being stored on C_p at the end of the integration of the first integrator. In the same way, the total charge for the second integrator in $\Phi_2[n]$ is equal to that in $\Phi_1[n+1]$. The operations of the two phases are illustrated in Fig. 6, which leads to the following charge conservation equation:

$$\begin{aligned} &C_{fw3}Uz^{-0.5} + C_{s2}V_1 z^{-1} + C_{ib2}V_2 z^{-0.5} - C_{ib1}V_2 z^{-1.5} \\ &\quad + C_{f2}\left(V_2 z^{-0.5} - \left(-\frac{V_2 z^{-0.5}}{A}\right)\right) + C_p\left(0 - \left(-\frac{V_1}{A}\right)\right) \\ &= C_{fw3}\left(V_{dac}z^{-0.5} - \left(-\frac{V_2 z^{0.5}}{A}\right)\right) + C_{s2}\left(0 - \left(-\frac{V_2}{A}\right)\right)z^{0.5} \\ &\quad + C_{ib2}\left(0 - \left(-\frac{V_2}{A}\right)\right)z^{0.5} + C_{ib1}\left(0 - \left(-\frac{V_2}{A}\right)\right)z^{0.5} \\ &\quad + C_{f2}\left(V_2 z^{0.5} - \left(-\frac{V_2 z^{0.5}}{A}\right)\right) + C_p\left(0 - \left(-\frac{V_2}{A}\right)\right)z^{0.5} \end{aligned} \tag{4}$$

After rearrangement, the second integrator transfer function can be expressed as the following two equations. In terms of $V_2/(U - V_{dac})$, the transfer function is:

$$\frac{V_2}{U - V_{dac}} = \frac{C_{fw3}}{C_{f2}} z^{-0.5} \frac{C_{f2}A}{C_{f2}(A+1) + C_{ib1} + C_{ib2} + C_{fw3} + C_{s2} + C_p} \frac{z^{-0.5}}{1 - \frac{C_{f2}(A+1)+C_{ib2}A}{C_{f2}(A+1)+C_{ib1}+C_{ib2}+C_{fw3}+C_{s2}+C_p} z^{-1} + \frac{C_{ib1}A}{C_{f2}(A+1)+C_{ib1}+C_{ib2}+C_{fw3}+C_{s2}+C_p} z^{-2}} \tag{5}$$

$$\frac{V_2}{V_1} = \frac{C_{s2}Az^{-1} + C_p}{C_{f2}A} \frac{C_{f2}A}{C_{f2}(A+1) + C_{ib1} + C_{ib2} + C_{fw3} + C_{s2} + C_p} \frac{z^{-0.5}}{1 - \frac{C_{f2}(A+1)+C_{ib2}A}{C_{f2}(A+1)+C_{ib1}+C_{ib2}+C_{fw3}+C_{s2}+C_p} z^{-1} + \frac{C_{ib1}A}{C_{f2}(A+1)+C_{ib1}+C_{ib2}+C_{fw3}+C_{s2}+C_p} z^{-2}} \tag{6}$$

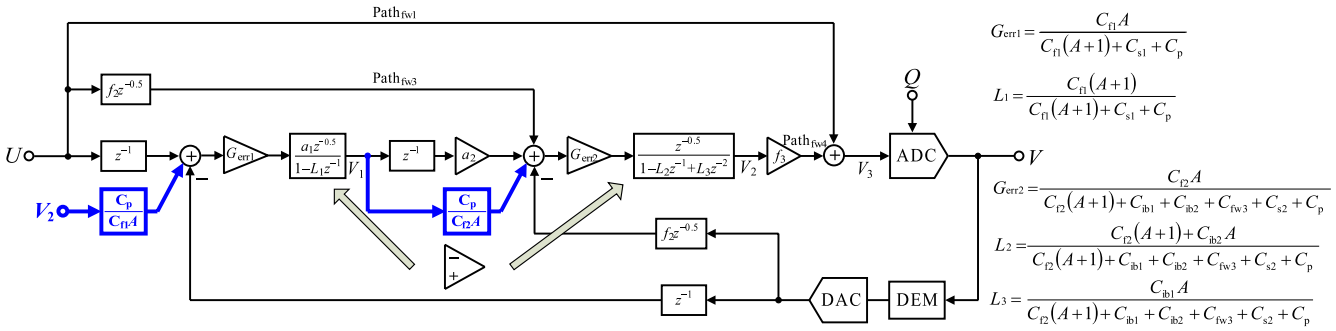


Fig. 7 Proposed DSM block diagram modeling the finite opamp gain and the memory effect.

Equation (6) is the transfer function of V_2/V_1. The numerator of its first term shows an additional C_p part that is contributed from the memory effect. The second term in Eq. (5) and Eq. (6) is the gain error, and the third term is the real integrator transfer function of a double integrator. Because of remaining V_2 component stored on C_p at the end of the integration of the second integrator, C_p also appears in the two terms has a slight influence on the integrator gain and the locations of the two poles of the double integrator (i.e., the two zeros of NTF).

Figure 7 shows the proposed DSM block diagram combined with the transfer functions of Eq. (2), Eq. (3), Eq. (5), and Eq. (6). The regions surrounded by bold line are to model the additional transfer function caused by the memory effect. To conveniently observe the influence on performance from the memory effect, Fig. 8 shows the simulation results for the DSM structure of Fig. 7 by the SIMULINK behavior model concerning the opamp finite gain A, kT/C noise, and various values for C_p. The range of C_p is assumed to be from 0.0 pF to 0.5 pF. In the circuit implementation, C_p consists of the gate parasitics of the opamp input differential pair and the layout routing. Moreover, A is set at 100, which is a reasonable assumption for a single-stage amplifier in single-loop DSMs. The simulations show that the SNDR varies only within 2.7 dB using the above conditions even if the capacitance of C_p is up to 0.5 pF. Also, the pre-layout simulation with an extra C_p capacitor located in the opamp input to model the layout routing is performed to manifest the influence of memory effect. Different to the parasitic capacitance set of the SIMULINK model, the capacitance of C_p is assumed from 0.0 pF to 0.4 pF in the transistor level simulation because the simulated gate parasitics of the opamp input differential pair is around 0.1 pF. Figure 9 illustrates the SNDR versus C_p value and depicts the same trend with the SIMULINK behavior model. Although the impact of the memory effect on SNDR is not serious when adopting the opamp sharing technique in the proposed DSM, this indicates that the layout routing connecting the opamp input and SC circuits should be minimized for minimizing the harm to performance.

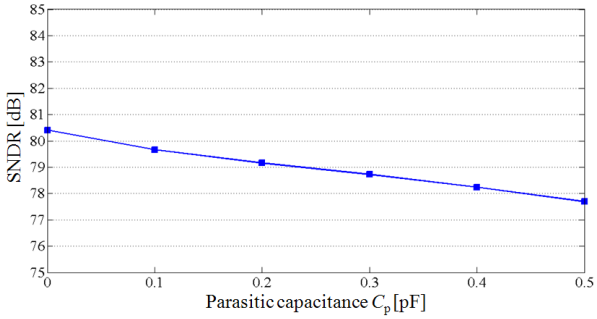


Fig. 8 SNDR versus C_p (SIMULINK behavior model).

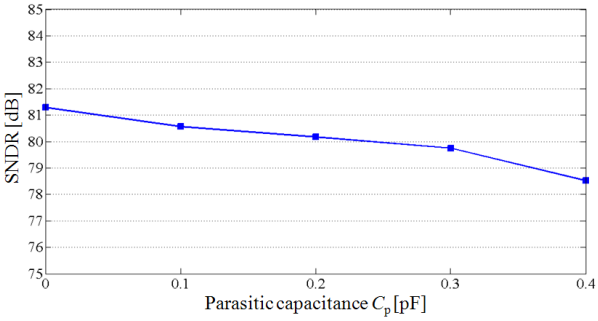


Fig. 9 SNDR versus C_p (transistor level simulation).

4. Details of the Circuit Implementation

4.1 Loop Filter

Figure 10 illustrates the schematic of the first and second integrators and the related clock signals to control the SC circuit for creating the analog delay. The subscript "d" indicates that the falling edge is slightly delayed. The two integrators are alternately active in Φ_2 and Φ_1 for sharing an amplifier. A double integrator [10], [16] is formed for the second one to enhance the noise shaping ability and effectively exploit the whole opamp power. As a result, the equivalent three cascade integrators in the proposed DSM can be performed by only an opamp. In order to further reduce the capacitor area and raise the feedback factor, the feedforward path, Path_{fw3} (C_{fw3}), and C_{s2} sampling path utilize the dif-

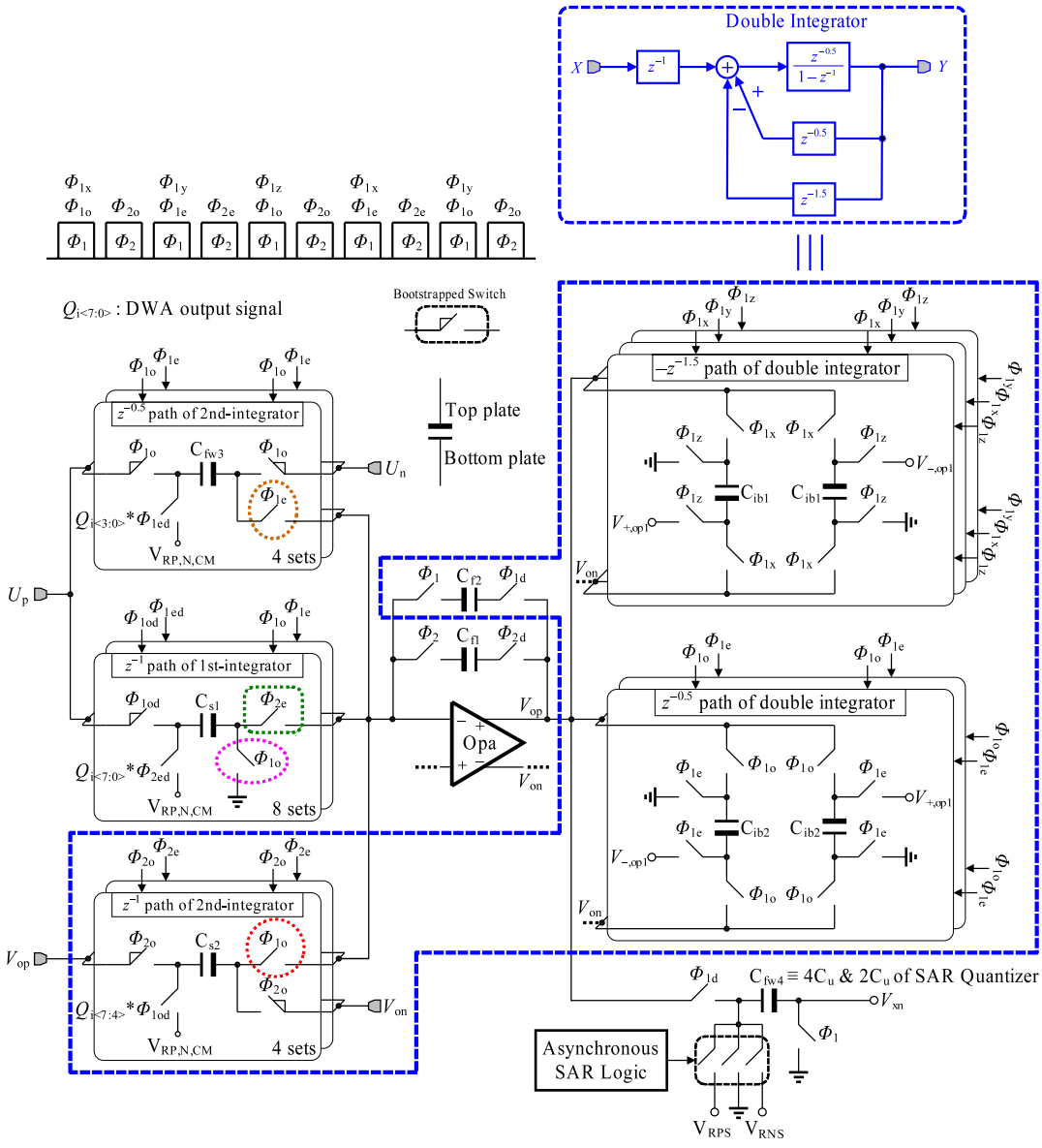


Fig. 10 Schematics of the first and second integrators.

ferential sampling scheme [22] (i.e., C_{s2} and C_{fw3} together act as the $f_2 \cdot z^{-0.5}$ DAC path in Φ_1). When this method is adopted, the modulator input signal and the output signal of the first integrator, which are individually stored on the parasitic capacitance at the top-plate of C_{fw3} and C_{s2}, will be also transferred to C_{f2}. Nevertheless, the effect can be seen as the coefficient variation, and is generally slight enough to be neglected in a single-loop DSM since the parasitic capacitance at the top-plate is much smaller than C_{f2}. In this design, C_{s1} is set to 1.2 pF depending on the selected SNDR (80 dB) specification and is chosen for an over design margin taking into account the process variation for capacitors. The size of the capacitors behind the first integrator is scaled down, and their relation is $2C_{s2} = 2C_{fw3} = 2C_{ib1} = 2C_{ib2} = C_{f2} = 0.16$ pF. The switches surrounded by the dotted line in Fig. 10 are the original 8 switches (4 switches) merged into an 8X-size (4X-size) switch, which can be done because the top plate of each unit capacitor in each SC set is always connected to the same potential or node. This merger of switches reduces the routing parasitic capacitance related to the switches. On the other hand, we propose a simplified DWA method based on merged-capacitor switching DAC array [23]. By this way, the size of DAC unit capacitor can be double, but the needed number of unit capacitors can be half, resulting in a constant value of total DAC capacitor array. Therefore, just 8 unit capacitors are needed for a 4-bit DAC.

4.2 Passive Adder and 4-bit SAR ADC

In the earlier work [16], an opamp between two adjacent clock phases is skillfully arranged for an active adder and a 4-bit cyclic-type quantizer to effectively use the opamp power. For further saving the number of required opamp

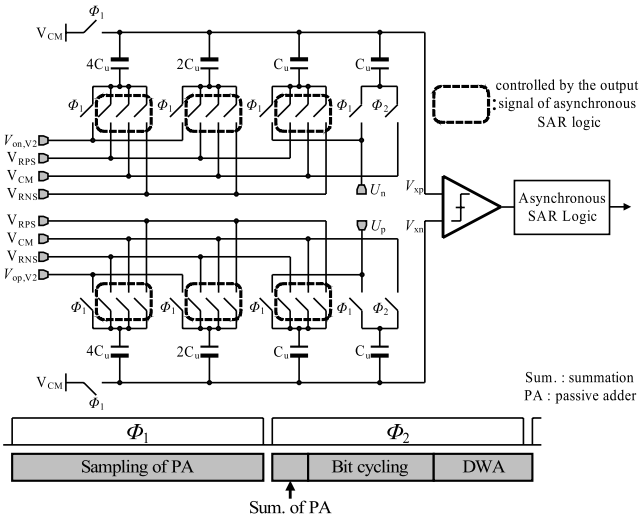
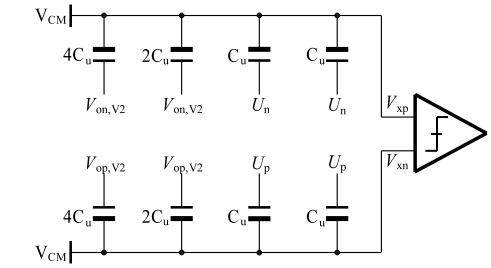
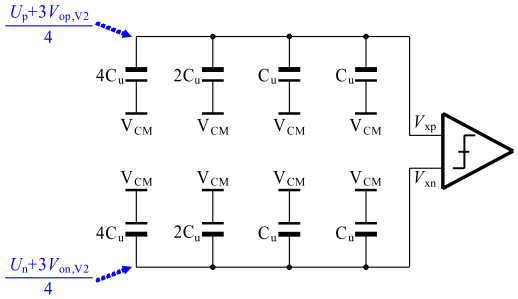


Fig. 11 Structure of the combined passive-adder SAR ADC.



(a)



(b)

Fig. 12 Implementation of passive summation: (a) sampling and (b) summation.

to decrease the total power consumption of DSM, this work adopts a combined passive-adder SAR ADC, as shown in Fig. 11. The switching method of the 4-bit SAR ADC is the same as with a V_{CM}-based SAR ADC [24]. The timing allotment as illustrated in Fig. 11 is that Φ_1 is for the signal sampling and Φ_2 is for both the quantization and DWA operation. Under a 60-MHz system frequency, when the bit cycling is completed, the remaining time before the next Φ_1 is more than enough for the use of DWA. Figure 12 illustrates the implementation of passive summation. During Φ_1, the two feedforward signals are sampled on the DAC array of SAR ADC by the bottom-plate sampling scheme, as

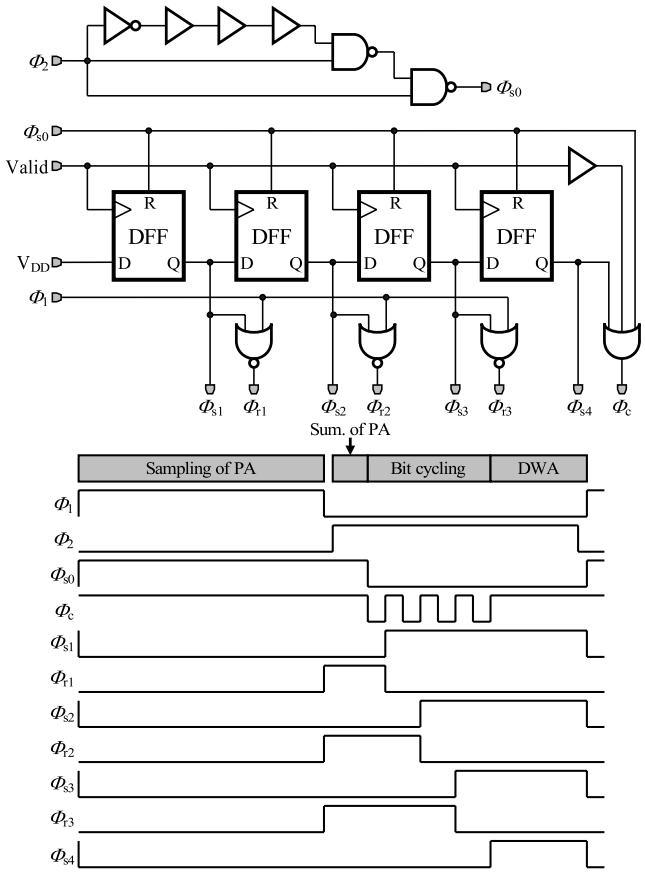


Fig. 13 Schematic and timing of asynchronous SAR logic.

shown in Fig. 12(a). According to the coefficient of the feedforward paths in Fig. 2(c), the input signal and the second integrator output signal are respectively stored in $2C_u$ (C_u & C_u) and $6C_u$ ($4C_u$ & $2C_u$), i.e., C_{fw4} in Fig. 10, where the value of C_u is 10 fF. The unit capacitor C_u is a metal-oxide-metal (MOM) finger sandwich capacitor. It is composed of metal 3 to metal 7, and occupies $3.9\,\mu\text{m} \times 4\,\mu\text{m}$. At the end of the summation phase, the two signals are summed on the top plate of the DAC array, as shown in Fig. 12(b). After the charge redistribution, the signal at the comparator input is as follows:

$$V_{xp(n)} = \frac{U_{p(n)} + 3V_{op(n),V2}}{4} \tag{7}$$

As a result, Eq. (7) shows a 1/4 attenuation factor for the summed signal when using this method. This attenuation can be compensated by using 1/4 the original reference voltage. In contrasted with the methods used in earlier literatures [19], [20], this summation approach can avoid the gain error, resulting from the parasitic capacitance in the node $V_{xp(n)}$, between the two feedforward signals. Compared with the conventional method for the active adder and the quantizer, the merged passive-adder SAR ADC is not only more power-efficient, due to saving an amplifier, but also more area retrenching, due to the area being the same with a purely V_{CM}-based SAR ADC.

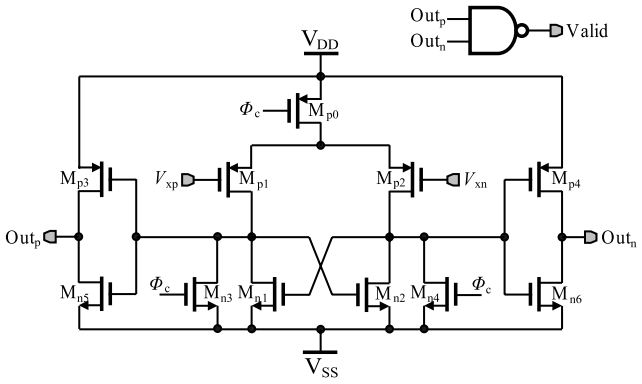


Fig. 14 Schematic of dynamic comparator.

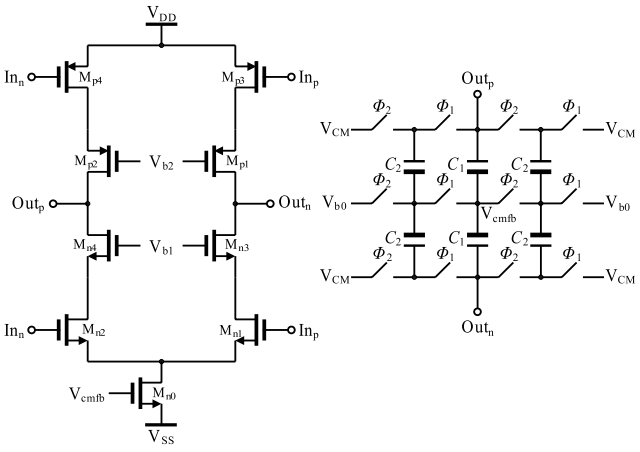


Fig. 15 Circuit diagram of class-AB telescopic amplifier.

In the designed SAR ADC, the asynchronous clocking circuit, similar to [25], is utilized to generate the control signals for DAC capacitor switching. Figure 13 shows a schematic of the asynchronous control logic and its timing. Clock Φ_{s0} is used to do the sampling and passive addition of the two feed-forward paths and Φ_c is the enabling signal of the comparator. Φ_{s1} to Φ_{s3} are the control signals for the switches, which are connected to reference voltages V_{RPS} and V_{RNS}, of the DAC capacitor array. Φ_{r1} to Φ_{r3} are the control signals for the switches, which are connected to the common voltage, of the capacitors $4C_u$, $2C_u$, and C_u. When the comparator makes the decision of the last bit, Φ_{s4} goes high and then it is to trigger the DWA logic. Moreover, a buffer inserted between the clock signal "Valid" and one of the inputs of the 3-input OR gate can prolong the usable DAC settling time. Figure 14 shows the circuit diagram of the dynamic comparator. While Φ_c is high, the comparator is off to save power and its outputs are reset to V_{DD}. When Φ_c goes from high to low, the comparator is enabled to amplify the difference between the inputs. After the comparison, the signal "Valid" created by the NAND gate outputs a high-level voltage to trigger the asynchronous SAR logic.

4.3 Operational Amplifier (opamp)

A wide-bandwidth telescopic amplifier is chosen due to benefiting from the narrow output swing of the two integrators (± 87.5 mV). Figure 15 shows the class-AB telescopic amplifier, which is the same as that in [16]. Because the differential input signal ($In_{p,n}$) is fed on both the NMOS and PMOS differential pairs, the equivalent transcoductance (G_m) of the class-AB amplifier changes from $G_m = g_{mn1,2}$ (for traditional telescopic amplifier) to $G_m = g_{mn1,2} + g_{mp3,4}$. Compared with the traditional telescopic amplifier in the same tail current, the amplifier possesses the capability of increased unity-gain bandwidth (around 1.5 time) and open-loop gain through the enhancement of the amplifier's equivalent transconductance.

5. Simulation Results

The proposed single opamp third-order low-distortion DSM

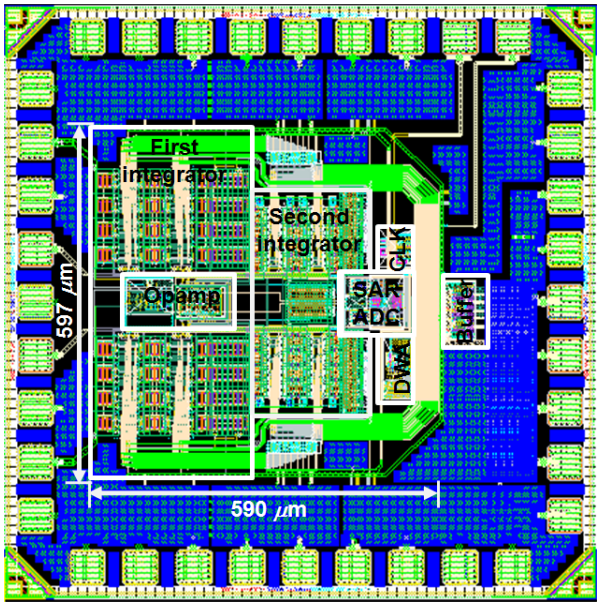


Fig. 16 Layout of the proposed third-order low-distortion DSM.

was implemented in a 90-nm 1P9M CMOS process. The layout of this design is shown in Fig. 16 and has an active area of 0.352 mm^2 (590 μm × 597 μm). The sampling frequency and the input signal bandwidth are 60 MHz and 1.875 MHz. Figure 17 illustrates the integrators' outputs in the transient simulation to present that the opamp output swing is within ± 87.5 mV. Both the analog and digital circuits use a 1.2-V power supply. In the post-layout simulation with 4096-point fast Fourier transform analysis, the SNDR reaches 79.8 dB at around 161-kHz input frequency, with a −6.3 dBFS signal power, as shown in Fig. 18. The relationship between the input signal amplitude and SNDR is shown in Fig. 19, and the dynamic range is over 75 dB. Figure 20 illustrates the percentage of power consumption for each block: the opamp consumes about 46.7% of the total power; the SAR ADC about 9.1%; and all the digital circuit, including the clock generator, the DWA logic, and

the D flip-flop array for creating the digital z^{-1} delay behind the DAC shown in Fig. 2(c), about 44.2%. Because of using single opamp, the analog power, including opamp and SAR ADC, is as low as the digital power.

Table 1 summarizes the post-layout simulation results and makes a comparison. The total power consumption is 2.85 mW. The calculated figure-of-merit (FOM) [16] is 95 fJ/conversion-step. Compared with other similar BW works, the post-layout simulations show an outstanding FOM. Of note, we emphasize that the calculated SNDR and FOM values of this paper and that of [16] do not include the thermal noise because it is not a chip's measurement.

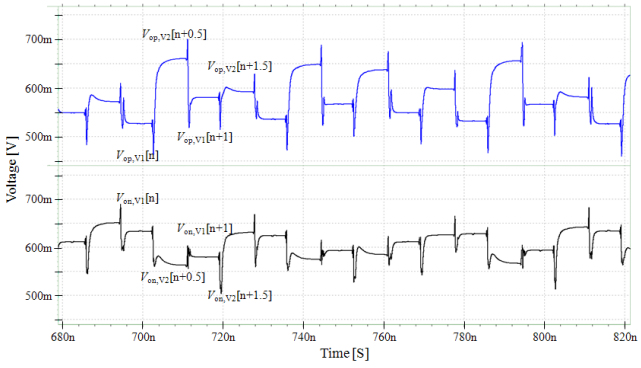


Fig. 17 Transient simulation of integrators.

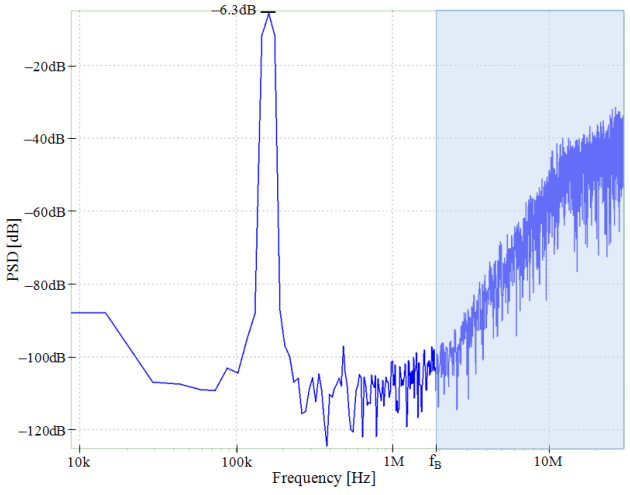


Fig. 18 Output spectrum for $f_{in} \approx 161$ kHz and −6.3 dBFS input signal amplitude.

6. Conclusion

A third-order low-distortion DSM was proposed that not

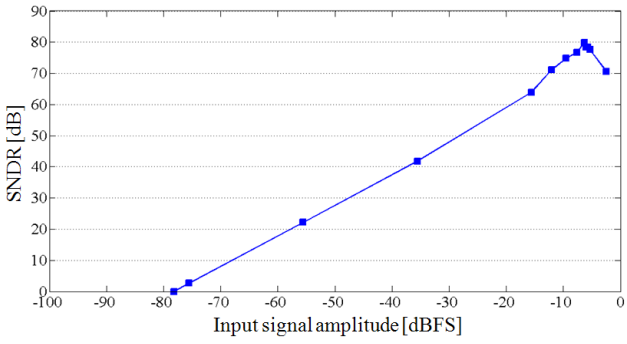


Fig. 19 SNDR versus input signal amplitude.

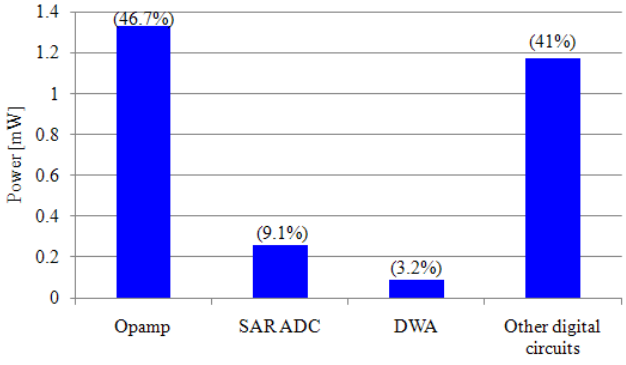


Fig. 20 Power distribution of proposed DSM.

Table 1 Performance summary and comparison.

Specification	Bos [3]			Bilhan [4]*	Maghari [5]	Nishida [13]	Rajaee [14]	Chao [16]*	This work**
Technology(nm)		90		90	180	180	180	90	90
Supply voltage(V)		1.2		1.2	1.5	1.8	1.2(A) / 1.5(D)	1.2	1.2
Sampling rate (MS/s)	50	90	80/320	60	50	40	25	80	60
OSR	250	90	20/80	15	24	20	8	16	16
Signal BW (MHz)	0.1	0.5	1.92	2	1.04	1	1.56	2.5	1.875
SNR (dB)	N/A	N/A	N/A	56	79.3	N/A	N/A	82.4	80.6
SNDR (dB)	77	76	65.5	N/A	78.2	75	75	81.97	79.8
Power (mW)	3.43	3.7	6.83	1.56	1.35 (A)	42.4 (A)	2.6 (A)	2.53 (A)	1.59 (A)
					1.55 (D)	16 (D)	3.75 (D)	1.64 (D)	1.26 (D)
FOM (pJ/conv.-step)	2.86	0.74	1.17	0.75	0.21	6.34	0.44	0.0815	0.095
Active area (mm^2)		0.076		N/A	0.44	3.42	3.79	N/A	0.35

* transistor-level simulation
** post-layout simulation

only simplifies an existing DSM architecture [16], but maintains all the advantages of a low-distortion DSM. Besides, the memory effect in the proposed DSM was explored and described in this paper. The proposed DSM is also able to overcome the timing bottleneck in the feedback path of the conventional low-distortion DSM. The time available for the quantizer and DEM is relaxed to half of the clock cycle so that the use of SAR-type quantizer, which needs many iterations to finish one conversion, is possible. Furthermore, a SAR ADC embedded passive adder is utilized to achieve the functions of both the quantizer and its input's adder, thus replacing the opamp-based active adder and saving power. For avoiding the gain error caused by the parasitic capacitance at the comparator input of SAR ADC, the passive adder samples the two feedforward signals on the bottom plate of DAC capacitor array, rather than the top plate of that. The results of post-layout simulation verify that the proposed single opamp third-order DSM presents the power efficient feature.

Acknowledgments

This work was supported by the National Science Council, Republic of China, under Grant Number NSC 102-2220-E-006-004.

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