

A Low-Cost Stimulus Design for Linearity Test in SAR ADCs

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SUMMARY The proposed stimulus design for linearity test is embedded in a differential successive approximation register analog-to-digital converter (SAR ADC), i.e. a design for testability (DFT). The proposed DFT is compatible to the pattern generator (PG) and output response analyzer (ORA) with the cost of 12.4% area of the SAR ADC. The 10-bit SAR ADC prototype is verified in a 0.18- μm CMOS technology and the measured differential nonlinearity (DNL) error is between -0.386 and 0.281 LSB at 1-MS/s.

key words: analog-to-digital converter (ADC), design for testability (DFT), pattern generator (PG), output response analyzer (ORA)

1. Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) are widely adopted in low-to-medium speed applications due to the low power consumption and small area overhead, especially in the system-on-a-chip (SoC) environment [1]. To test a SAR ADC in the SoC environment is becoming a challenging issue because of the limited input/output pin counts, observability, controllability, etc.

Many techniques, such as design for testability (DFT) [2] and built-in self-test (BIST) [3], have been proposed to alleviate the test effort for embedded ADCs in the SoC environment. These techniques require suitable on-chip stimuli. Designing a high-quality stimulus to test ADCs is a feasible solution [4]. This stimulus is applicable for most ADCs, but the area overhead is high for linearity test in SAR ADCs. The stimulus design may occupy additional 75% or more area of the SAR ADCs [4]–[7] in the 0.18- μm CMOS technology. This solution drastically imposes large testing cost.

In designing the stimuli, the output swing and resolution should also be considered. The output swing of the stimulus should cover the input swing of the ADCs under test. The resolution of the stimulus should be better than the resolution of the ADCs under test. For SAR ADCs, the input swing is often designed to be rail-to-rail, and 8- to 10-bit SAR ADCs are widely adopted [5]–[7]. Thus, designing a wide-range high-resolution stimulus for linearity

test in SAR ADCs is a challenging issue. To reach the resolution requirement, the sigma-delta modulation technique is considered, e.g. a 1-bit sigma-delta modulation based signal generation followed by a low-pass filter [3]. However, the output swing is still limited by the low-pass filter. Another compound stimulus based on the coarse and fine digital-to-analog converters (DACs) is proposed to fulfill the output swing requirement [8]. The capacitor array in the SAR ADC is modified to implement the coarse DAC. An additional narrow-swing fine DAC is connected to the negative terminal of the comparator to enhance the accuracy of the stimulus. This method is only for single-ended SAR ADCs, and the modification on the negative terminal of the comparator may introduce some offset into the comparator.

In this paper, a digitally-controlled small-area stimulus for linearity test in a SAR ADC is proposed. The stimulus is based on the coarse-fine architecture for the resolution and swing considerations. Only the digital components (SAR logic and switches) are modified and the sensitive analog components (comparator and capacitor arrays) are unchanged. The embedded stimulus is implemented as the design for testability (DFT) with small area in comparison with the previous work [4]. This proposed DFT is also further combined with the pattern generator (PG) and output response analyzer (ORA) to verify the feasibility of the fully-digital built-in self-test (BIST) for the SAR ADC in the SoC environment.

The rest of this paper is organized as follows. Section 2 describes the basic principles for the proposed DFT circuit. Section 3 illustrates the designed building blocks in detail. Then the measurement results are shown in Sect. 4. Finally, conclusions are made in Sect. 5.

2. Architecture and Design Concept of The Proposed Embedded Stimulus

First, in the normal mode, the operation of conventional differential SAR ADCs (sampling on bottom plates) is defined. The proposed embedded stimulus is generated in the test mode by modifying the operation of conventional SAR ADCs. Then, the operations of the SAR ADC (sampling on top plates) in the normal mode and test mode are also revealed for further verification. Moreover, the decision of parameters, the impact of nonlinearity, and the application for 10- to 16-bit SAR ADCs are discussed.

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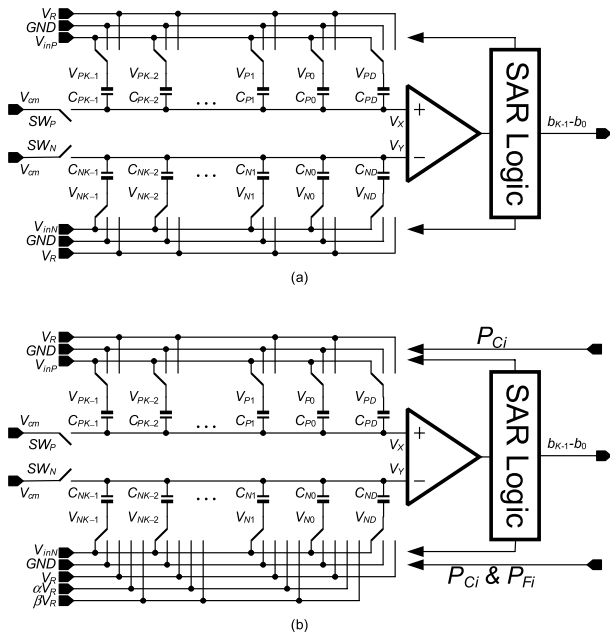


Fig. 1 (a) The architecture of the conventional differential SAR ADC (sampling on bottom plates). (b) The proposed DFT in the SAR ADC (sampling on bottom plates).

2.1 Operation and Modification of Conventional SAR ADCs (Sampling on Bottom Plates)

To achieve high accuracy, fully differential architectures are often adopted due to the tolerance for the power, substrate and common-mode noise [9].

The architecture of the conventional K -bit differential SAR ADC (sampling on bottom plates) with the output digital code $b_{K-1} - b_0$ in the normal mode is shown in Fig. 1(a) [9]. The comparator, SAR logic and capacitor arrays are included in the conventional SAR ADC. In one capacitor, the thick solid line is the bottom plate, and the thin line is the top plate. The bottom plates are connected to the reference voltage V_R , the ground GND , or one of the inputs V_{inP}/V_{inN} . In the normal mode, three steps (sample, hold, and bit-cycling) are in every analog-to-digital conversion. In the sample step, the top plates of all capacitors are connected to the common-mode voltage V_{cm} , i.e. $V_X = V_Y = \frac{V_R}{2}$, through switches SW_P and SW_N . The bottom plates of the positive and negative capacitor array are connected to positive input (V_{inP}) and negative input (V_{inN}), respectively. In the hold and bit-cycling steps, the operations in the positive and negative capacitor array are complement. For simplicity, only the operation in the positive capacitor array are listed. In the hold step, the top plates are all disconnected from V_{cm} , V_{PK-1} is connected to V_R , and the rest bottom-plate voltages (V_{PK-2}, \dots, V_{P0} , and V_{PD}) are connected to GND . Thus, the input voltages are stored on the top plates, i.e. $V_X - V_Y = V_{inN} - V_{inP}$. In the bit-cycling step, if $V_X < V_Y$, the first output bit b_{K-1} is logical 1. Otherwise, b_{K-1} is logical 0 and V_{PK-1} is set to be GND . Then, $V_{PK-2} = V_R$ and

another comparison starts. This process repeats for K times until all of the output bits ($b_{K-1} - b_0$) are evaluated.

In the test mode, the proposed embedded stimulus is activated as shown in Fig. 1(b). By comparing Fig. 1(a) and Fig. 1(b), only some additional switches and power sources (αV_R and βV_R) are required for the generation of the embedded stimulus. The generation is combined with the three steps (sample, hold, and bit-cycling) in an analog-to-digital conversion. Every voltage of the embedded stimulus is defined by digital patterns (P_{Ci} and P_{Fi}) in the sample step and held on the bottom plates in the hold step according to the following mechanism. Then, the voltage is digitalized by bit-cycling step.

In the sample step, the whole negative capacitor array (DAC) are divided into coarse and fine DACs (CDAC and FDAC) by dividing the supply voltage V_R into two parts, i.e. αV_R and βV_R . The coarse supply ratio α and the fine supply ratio β are below or equal to one ($\alpha, \beta \leq 1$) and $\alpha + \beta = 1$. The top plates are connected to the common-mode voltage V_{cm} through switches (SW_P or SW_N) and the bottom plates of the dummy capacitors (C_{PD} and C_{ND}) are connected to V_R . The bottom-plate voltages of the rest capacitors are defined by the following equations

$$V_{Pi} = P_{Ci} \cdot V_R \quad i = 0, \dots, K-1 \quad (1)$$

$$V_{Ni} = \overline{P_{Ci}} \cdot \overline{P_{Fi}} V_R + \overline{P_{Ci}} P_{Fi} \cdot \alpha V_R + P_{Ci} \overline{P_{Fi}} \cdot \beta V_R \quad (2)$$

$$i = 0, \dots, K-1$$

where P_{Ci} , and P_{Fi} are the binary coarse pattern and the binary fine pattern for the capacitor C_i , respectively. The voltage on the bottom plate in the positive capacitor array V_{Pi} is only controlled by the coarse pattern according to (1). The voltage (V_{Ni}) is the combination of the coarse pattern voltage (V_R or αV_R) and the fine pattern voltage (βV_R) by (2). This arrangement is due to the complement switching on the positive and negative capacitor arrays and the voltage setup in the hold step. The two parameters α and β are defined for the ratios to the maximum supply V_R in the coarse and fine capacitor arrays, respectively. When the switches and voltages are all set, the hold step is activated. Thus, the top plates of the two capacitor arrays hold the designed voltage according to the following equations

$$V_X = \frac{1}{2}(V_R - V_{PK-1}) - \sum_{i=0}^{K-2} \frac{C_{Pi}}{C_{PT}} \cdot V_{Pi} - \frac{C_{PD}}{C_{PT}} V_R \quad (3)$$

$$V_Y = -\frac{1}{2} V_{NK-1} + \sum_{i=0}^{K-2} \frac{C_{Ni}}{C_{NT}} \cdot (V_R - V_{Ni}) \quad (4)$$

where $C_{PT} = C_{PK-1} + \dots + C_{P0} + C_{PD}$ and $C_{NT} = C_{NK-1} + \dots + C_{N0} + C_{ND}$. By repeating the above mentioned mechanism, every voltage of the embedded piecewise linear stimulus can be generated and then quantified in the analog-to-digital conversion as shown in Fig. 2 for an 1-MHz 4-bit SAR ADC (sampling on bottom plates). The embedded stimulus and output digital code $Dout$ are shown as the solid line with square and dotted line with triangle, respectively. The piecewise linear ramp stimulus is composed by two local ramp

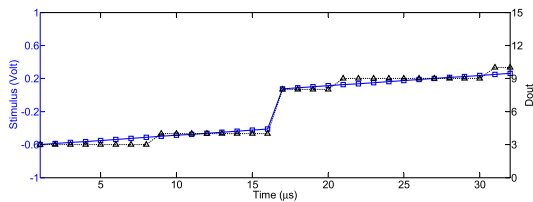


Fig. 2 The embedded stimulus and the digital output code.

stimuli. The minimum voltage of each local ramp stimulus is defined by the coarse pattern. The binary coarse patterns ($P_{C3} - P_{C0}$) for the first and second local ramp stimuli are $(1100)_2$ and $(0110)_2$, respectively. Based on the minimum voltage, the local ramp stimulus increases with the counting down binary sequence of the fine patterns ($P_{F3} - P_{F0}$) from $(1111)_2$ to $(0000)_2$. The interval for each local ramp stimulus is 16 clock cycles. Thus, the slope of each local ramp stimulus can be changed by regularly eliminating some fine patterns from the complete 4-bit counting sequence. The slope is also controlled by the supply ratios. The supply ratio α and β are 0.8 and 0.2, respectively. Thus, 10 hits can be collected for the digital output code 9. The relation between average number of hits per code and supply ratios are detailed in Sect. 2.3.

2.2 Modifications on Differential SAR ADCs (Sampling on Top Plates)

Many SAR ADCs (sampling on top plates) are proposed recently due to the simpler switch design, relaxed control logic design, and power-saving switching schemes [6], [7], [9], [10]. Thus, the proposed technique is also applied to a differential K -bit mono-switching SAR ADC (sampling on top plates) as a DFT for further verification. The differential SAR ADC (sampling on top plates) and the proposed DFT with the ORA and PG are shown in Figs. 3(a) and (b), respectively. By comparing Figs. 3(a) and (b), the proposed embedded stimulus only requires some additional switches and power sources as shown in Sect. 3.

In the normal mode as shown in Fig. 3(a), one conversion also contains three steps: sample, hold, and bit cycling. At first, the input signal is sampled on the top plates while the bottom plates are all connected to V_R . Then, the bit-cycling step starts without any operation in the hold step.

In the test mode as shown in Fig. 3(b), three steps are needed. At first, the top plates are connected to GND through SW_P and SW_N in the sample step. The bottom plates of the capacitors are connected to V_R , GND , or βV_R , according to the following equations

$$V_{Pi} = \overline{P_{Ci}} \cdot V_R + \overline{P_{Fi}} \cdot \beta V_R \quad i = 0, \dots, K-1 \quad (5)$$

$$V_{Ni} = P_{Ci} \cdot V_R + P_{Fi} \cdot \beta V_R \quad i = 0, \dots, K-1 \quad (6)$$

where P_{Ci} , P_{Fi} , and β are the same as defined in (2). The differences between (1), (2) and (5), (6) are caused by the two different reset voltages in two SAR ADC architectures in hold steps. By comparing Fig. 1(b) and Fig. 3(b), the input voltages in the sample steps are moved from $\frac{V_R}{2}$ to GND .

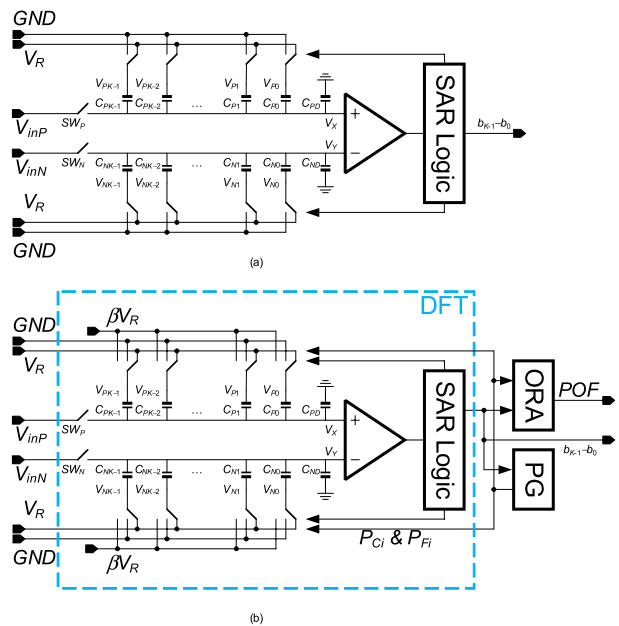


Fig. 3 (a) The differential SAR ADC (sampling on top plates). (b) The proposed DFT is contained in the BIST architecture.

On the other hand, all the bottom plates are set to V_R in the hold step. In contrast, some bottom plates are connected to GND and some are connected to V_R in the bottom-plate sampling SAR ADC in Fig. 1. After all the bottom plates are set according to (5) and (6) in the sample step, all the bottom plates are then connected to V_R in the hold step and the corresponding voltages on top plates are

$$V_X = \sum_{i=0}^{K-1} \frac{C_{Pi}}{C_{PT}} \cdot (V_R - V_{Pi}), \quad (7)$$

$$V_Y = \sum_{i=0}^{K-1} \frac{C_{Ni}}{C_{NT}} \cdot (V_R - V_{Ni}). \quad (8)$$

The voltage differences on the bottom plates are scaled by the capacitor ratios and transferred to the top plates. Next, the bit-cycling step starts until K output digits are evaluated.

With the proposed digitally-controlled embedded stimulus, the interface of the differential nonlinearity (DNL) measurement system can be simplified.

In the proposed mechanism, the embedded stimulus is generated and quantized with the same capacitor array. Thus, the input range of the SAR ADC is identical with the output range of the embedded stimulus. The linearity requirement for the static linearity test is discussed in Sect. 2.5. The implementation of the SAR ADC (sampling on top plates) and area cost are mentioned in Sect. 3.

2.3 Average Number of Hits Per Code

The selections of α and β in (1), (2) and (5), (6) are directly related to the average number of hits per code (H_{AVG}), which is the number of hits for a code to be observed in the conventional linear ramp histogram method [11]. In a rail-to-rail

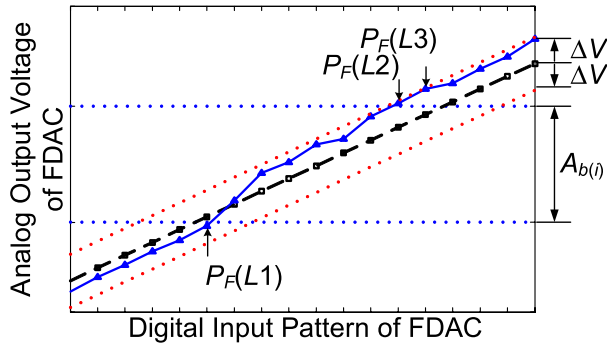


Fig. 4 The impacts of nonlinearity of FDAC on linearity Test in SAR ADCs.

differential K -bit SAR ADC, the minimal resolution is

$$\frac{2V_R}{2^K} = 2^{-(K-1)}V_R = 1LSB_{ADC} \quad (9)$$

In the FDAC, the fine patterns $P_F(i)$, $i = 0, \dots, 2^K - 1$, is proportional to the voltage range from 0 V to βV_R . Thus, the average resolution of FDAC is

$$\frac{\beta V_R}{2^K} = 2^{-K}\beta V_R = 1LSB_{FDAC}. \quad (10)$$

If the FDAC is controlled by a counter, the stimulus is increased by $1LSB_{FDAC}$ in one clock cycle and a linear ramp stimulus is generated. The generated linear ramp stimulus is quantified by the SAR ADC under test. From (9) and (10), the average number of hits per code is given as

$$H_{AVG} = \frac{1LSB_{ADC}}{1LSB_{FDAC}} = \frac{2}{\beta}. \quad (11)$$

Thus, the average number of hits per code is inversely proportional to the fine supply ratio of the FDAC. If the hit count for one code is defined, the values of β is also determined and so does α by the relation $\alpha + \beta = 1$.

2.4 Impact of FDAC Nonlinearity on Linearity Test in SAR ADCs

The integral nonlinearity (INL) of the FDAC may degrade the SAR ADC testing accuracy as one example shown in Fig. 4. The dashed line is the ideal transfer curve of the FDAC, and the solid line is the actual transfer curve. The boundaries of the INL and the input range of a certain SAR ADC output code are depicted with dotted lines. The partial analog output of the FDAC ($A_{b(i)}$) stimulates the SAR ADC to output a certain digital output code $b(i)$, where $b(i)$ in the decimal format is $b_{K-1} - b_0$ in the binary format in Fig. 1. Ideally, the fine patterns from $P_F(L_1)$ to $P_F(L_3)$ triggers the FDAC to generate the stimulus which fits the input range of the code $b(i)$. The actual transfer curve is limited by the boundaries $\pm\Delta V = \pm\gamma LSB_{FDAC}$ (γ is a constant). In this transfer curve, three deviated points ($P_F(L_1)$, $P_F(L_2)$, and $P_F(L_3)$) affect the hit count of the code $b(i)$. The ideal hit count for the code $b(i)$ is $H_{ideal}(b(i)) \cong H_{AVG}$. The measured

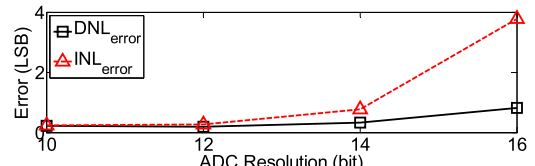


Fig. 5 The static linearity error for 10- to 16-bit SAR ADCs.

hit count should be above $(H_{AVG} - 2\gamma)$, and the measured DNL error of the SAR ADC is $|\frac{2\gamma}{H_{AVG}}|$, which is inversely proportional to H_{AVG} . Thus, the test accuracy can be improved by increasing the average number of hits per code H_{AVG} .

2.5 Discussion on Static Linearity Errors

The nonlinearity of the stimuli directly affects the static linearity test and causes some static linearity errors. Thus, the linearity of the proposed embedded stimulus is verified by the behavioral model in Matlab. The behavioral model is suitable for the two architectures in Sects. 2.1 and 2.2.

The capacitor mismatch error is the dominant factor for the static linearity in switch-capacitor SAR ADCs. The random mismatch errors limits the static linearity of SAR ADCs to 10 bits [12]. Thus, the capacitor mismatch error is introduced into the behavioral model as a Gaussian random variable. The standard deviation σ of the mismatch error is estimated by $\sqrt{2^{10}}\sigma = C_{min}$, where C_{min} is the minimum capacitance in the capacitor array in the 10-bit SAR ADC. The conversion rate and average number of hits per code are 1 MHz and 100, respectively. The DNL error is the difference between two measured DNLs by the ideal ramp histogram method and the proposed embedded stimulus. The INL error is evaluated with similar approach. One thousand SAR ADCs are simulated for every DNL error and INL error. As shown in Fig. 5, the average peak-to-peak DNL error and average peak-to-peak INL error in 10-bit SAR ADCs are 0.22 and 0.24 LSB, respectively. Thus, the linearity of the embedded stimulus is suitable for 10-bit SAR ADCs. Then, the 12- to 16-bit SAR ADCs are also simulated according to the same environment setup. In 12-bit SAR ADCs, the average peak-to-peak DNL error and INL error is 0.19 and 0.27 LSB, respectively. The linearity of the embedded stimulus is viable for the 12-bit SAR ADC with slightly increased INL error. In 14-bit SAR ADCs, the average peak-to-peak DNL error and INL error are 0.33 and 0.77 LSB, respectively. In 16-bit SAR ADCs, The average peak-to-peak DNL error and INL error are 0.82 and 3.77 LSB, respectively. The amount of missing codes arises with higher resolution and cause the increase of the DNL error and INL error. Thus, the proposed embedded stimulus is not suitable for 14- to 16-bit SAR ADCs.

3. Implementation of Building Blocks

To verify the feasibility of the proposed embedded stimulus in the SoC environment, the BIST in Fig. 3(b), including

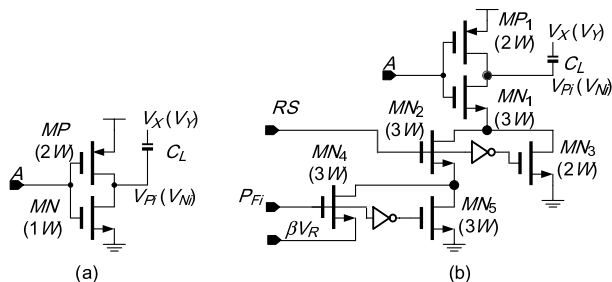


Fig. 6 (a) The switch used in [9] and (b) the modified switch in the proposed DFT.

the proposed embedded stimulus in the 10-bit SAR ADC (DFT), pattern generator (PG), and output response analyzer (ORA), are fabricated in a 0.18- μm CMOS process. The unit capacitor, bootstrapped switches, and SAR logic are implemented as those in [9]; other modified or designed components are described in this section.

3.1 Analog Components

The basic architecture of the comparator is the same with the dynamic two-stage comparator [13].

In this proposed DFT, only one additional supply (βV_R) is needed. Thus, a simple resistor string is qualified to be the supply of the FDAC.

Another modified component is the switch connected the bottom plates and power supplies. The switches are designed to be an inverter in [9] shown in Fig. 6(a). By contrast, in this proposed DFT, the switches should be connected to three different power supplies (V_R , GND , and βV_R) and controlled by two control signals (P_{Fi} and RS) as shown in Fig. 6(b). The P_{Fi} signal decides the lower voltage of the bottom plates (V_{Pi} or V_{Ni}) to be GND or βV_R . The RS signal is logic 1 in the test mode and logic 0 in the normal mode.

The size of every transistor in the modified switch is derived by evaluating the logic effort. The length of every transistor is set to be minimal length (L) in a CMOS process. For the discharging critical path through MN_1 , MN_2 , and MN_4 (MN_5), the width of every transistor is set to be $3W$, where W is the minimal width. If the gate delay of an inverter driving an identical inverter without parasitic capacitors is τ second, the gate delays in the the normal mode (t_{dN}) and test mode (t_{dT}) are

$$t_{dN} = \left(\frac{5}{3} \cdot \frac{C_L}{5WL} + \frac{25}{18} \right) \tau, \quad (12)$$

$$t_{dT} = \left(\frac{5}{3} \cdot \frac{C_L}{5WL} + \frac{5}{3} \right) \tau. \quad (13)$$

In general design, the effort delay ($\frac{5}{3} \cdot \frac{C_L}{5WL}$) τ is greater than the parasitic delay ($\frac{5}{3}$) τ or ($\frac{25}{18}$) τ . Thus, by ignoring the parasitic delay, the gate delay of the modified switch is the same as an inverter gate delay at the expense of the area overhead. The WL gates in the designed switch and inverter are summed up individually and compared. The area overhead

Table 1 Area comparison between SAR ADC and SAR DFT.

Components	SAR ADC (μm^2)	DFT (μm^2)
Bootstrapped Switch	$60 \times 38 \times 2$	$60 \times 38 \times 2$
Comparator	79×94	79×94
Capacitor Array	$224 \times 100 \times 2$	$224 \times 100 \times 2$
SAR Logic	223×55	233×55
Switches	$80 \times 20 \times 2$	$170 \times 20 \times 2$
Resistor String	0	82×24
ADC Core	326×293 (100%)	358×300 (112.4%)
PG	0	235×235
ORA	0	130×235
BIST	0	753×300 (236.5%)

of the modified switch is about 7.33 times as big as an inverter.

3.2 Digital Components

Some internal D flip flops (DFFs) in the SAR logic are modified to be scan flip flops to receive coarse patterns (P_{Ci}).

The pattern generator (PG) for coarse patterns (P_{Ci}) and fine patterns (P_{Fi}) is based on the selective code measurement [14], [15]. At first, the coarse and fine patterns are set for the embedded stimulus to test the least-significant bit (LSB), i.e. b_0 . Then, the output response analyzer (ORA) recodes the result and compares it with pre-defined upper and lower boundaries. After that, other bits ($b_1 \dots b_{K-1}$) are tested one by one. The coarse pattern generation is implemented by a 10-bit shift register, and the fine pattern generation is by a 10-bit counter.

The output response analyzer (ORA) circuit is designed to compare test results, generate test clock, and output pass-or-fail (POF) signal. The output comparison is achieved by 10 exclusive-OR gates (XORs). When one comparison is completed, the ORA circuit triggers the next comparison. When 10 comparison results are collected, the POF signal is activated.

3.3 Overhead

The area comparison between the SAR ADC (sampling on top plates) and the proposed DFT is shown in Table 1. The area of every component in the SAR ADC (sampling on top plates) is listed in the second column. The area of the components in the proposed DFT, PG, and ORA are listed in the third column. Three additional components (resistor string, PG, and ORA) are not required in the SAR ADC, thus the area is zero in the second column. The designed switch is much bigger than an inverter as mentioned in Sect. 3.1. However, the layout area is only about double and the associated layout cost is acceptable. This is due to the layout pitch (the minimal height for every digital component). In this work, the pitch is decided by the height of the D flip-flop layout. Thus, the area difference between the designed switch and the inverter shrinks. The resistor string doesn't consume much area in this proposed DFT design. The proposed DFT only consumes extra 12.4% area in comparison with the SAR ADC. The total BIST area is 2.36 times as much as the SAR ADC mainly due to the area consumed by the PG and ORA.

The total test time (t_{test}) can be divided into four parts, including tag time (t_{tag}), setup time (t_{setup}), sample time (t_{sample}), and output time (t_{output}) in a K -bit SAR ADC, i.e.

$$t_{test} = t_{tag} + t_{setup} + t_{sample} + t_{out} = (aK + bK + cK \cdot H_{AVG} + d)t_{CLK}. \quad (14)$$

where a, b, c , and d are constants to represent the number of clock cycles. The period of the conversion rate is t_{CLK} . In the selective code measurement, K test pattern sets are required for verifying a K -bit SAR ADC. The tag time is for the header of every test pattern set, e.g. a clock cycles for one test pattern set. The setup time is for adjusting the embedded stimulus to be less than the targeted output code by 1 LSBs, and every test pattern set requires at least b clock cycles. The sample time is for collecting the selective codes, and on average one certain code should repeat for H_{AVG} clock cycles. For one certain selective code, saying 15, the embedded stimulus should cover c LSBs around this output code. In this design the value of c is set to be 4, which means the generated piecewise linear ramp stimulus fulfills the small input range of the SAR ADC to output digital codes: 14, 15, 16, and 17. Finally, the pass-or-fail signal (POF) can be observed in d clock cycles due to the digital processing delay in the ORA. In the following experiment, the values of $a-d, K$, and H_{AVG} are 2, 10, 4, 2, 10, and 100, respectively. Thus, the total test time is 4.122 ms at clock rate of 1 MHz, which is shorter than that in the conventional ramp histogram method, i.e. 102.4 ms.

4. Measurement Results

The die photo of the fabricated chip is shown in Fig. 7. The occupied active area is $753 \times 300 \mu\text{m}^2$, and the detailed size of every components are listed in the third column in Table 1.

The test setup is shown in Fig. 8. The signal generator (Agilent 81150A) provides the clock signal and differential ramp/sinusoidal stimulus for the SAR ADC under test in the normal mode, but only clock signal in the test mode. The logic analyzer (Agilent 16822A) collects the output digital codes from the SAR ADC in both modes and POF signal from the ORA in the test mode. The collected data are passed to the PC for further signal processing and analysis. Other measurement results are demonstrated below.

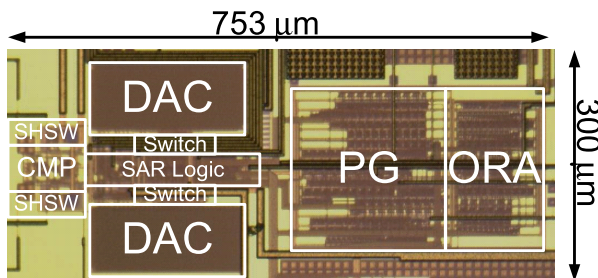


Fig. 7 The die photo of the BIST.

4.1 Dynamic Performance and Figure-of-Merit

The measured effective number of bits (ENOB) is 8.94 bits in the normal mode at Nyquist rate. The harmonic tones due to capacitor mismatch degrade the dynamic performance. The figure-of-merit (FOM) is 44.65 fJ/Conv.-step according to the formula in [9].

4.2 Static Performance

For the static performance, three capacitor configurations are demonstrated, including woMisCap, MisA, and MisB. In the woMisCap configuration, the capacitor arrays (C_{Pi} and $C_{Ni}, i = 9-0$) in the SAR ADC are binary-weighted. In the MisA configuration, the MSB capacitors (C_{P9} and C_{N9}) are increased by two-unit capacitance ($2C_{min}$), i.e. $C_{P9} = C_{N9} = 514C_{min}$, in comparison with $512C_{min}$ normally. In the MisB configuration, the third MSB capacitors are set to be two-unit capacitance bigger than the normal value, i.e. $C_{P7} = C_{N7} = 130C_{min}$, in comparison with $C_{P7} = C_{N7} = 128C_{min}$ normally.

The DNL and INL in the woMisCap configuration are shown in Fig. 9. Wide codes at code 511 and 512 can be ob-

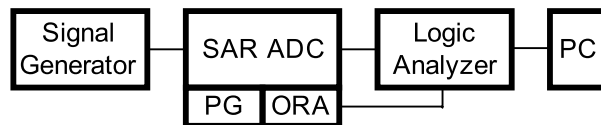


Fig. 8 The test setup in the normal mode and test mode.

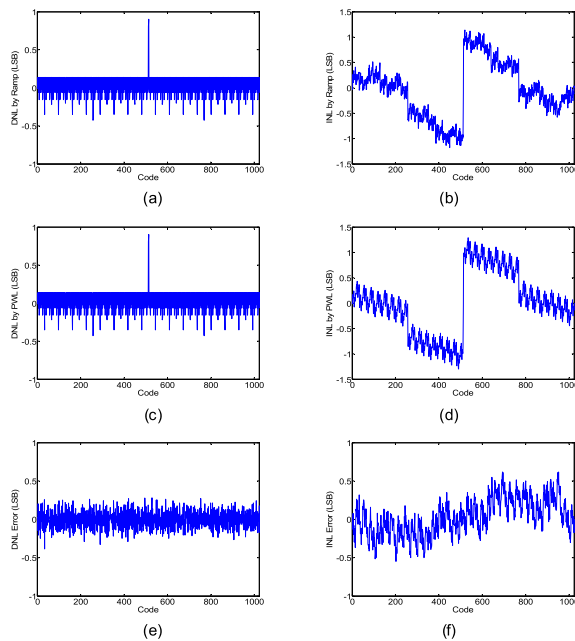


Fig. 9 The measured linearity results in the woMisCap configuration. (a) DNL by the ramp stimulus. (b) INL by the ramp stimulus. (c) DNL by the PWL stimulus. (d) INL by the PWL stimulus. (e) DNL error between two tests. (f) INL error between two tests in woMisCap configuration.

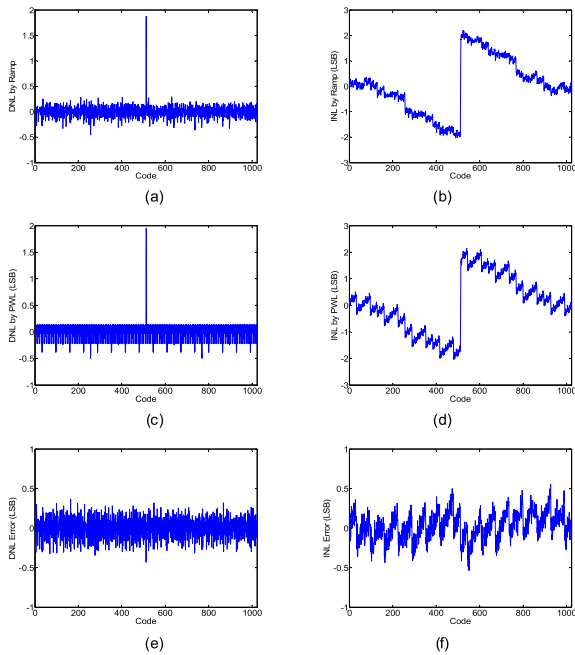


Fig. 10 The measured linearity results in the MisA configuration. (a) DNL by the ramp stimulus. (b) INL by the ramp stimulus. (c) DNL by the PWL stimulus. (d) INL by the PWL stimulus. (e) DNL error between two tests. (f) INL error between two tests in woMisCap configuration.

served in Fig. 9(a) and Fig. 9(c) by using the linear ramp histogram test method [11] (DNL by the ramp stimulus) and the selective code measurement (DNL by the piecewise linear stimulus, PWL), respectively. The wide-code phenomenon is due to the oversized MSB capacitance than expected. The corresponding INL are shown in Fig. 9(b) and Fig. 9(d). The DNL and INL errors between the two tests are shown in Fig. 9(e) and Fig. 9(f), respectively. The respective DNL error and INL error are $0.2814/-0.3861$ and $0.6189/-0.5471$ LSB.

In the MisA configuration, the more significant wide-code phenomena at code 511 and 512 are observed in Fig. 10(a) and Fig. 10(c) due to the additional mismatched capacitance on the MSB capacitors by roughly 1LSB in two test methods. The wide codes also generate abrupt INL gap at code 511 and 512 in Fig. 10(b) and Fig. 10(d). The DNL error and INL error in Fig. 10(e) and Fig. 10(f) are $0.3665/-0.4317$ and $0.5499/-0.5384$ LSB, respectively.

In the MisB configuration, the wide-code phenomena at code 511 and 512 are cancelled and some codes are almost missing (code 255, 256, 767, and 768) in Fig. 11(a) and Fig. 11(c). In Fig. 11(b) and Fig. 11(d), the INLs are separated into pieces and the abrupt gaps appear at the positions of wide/missing codes. The peak DNL error in Fig. 11(e) and INL error in Fig. 11(f) are $0.6216/-0.4049$ and $0.7869/-0.8422$ LSB, respectively. Four spikes at code 254, 257, 766, and 769 are shown in Fig. 11(e) because these codes are also affected by the additional mismatched capacitors (C_{P7} and C_{N7}). However, these codes are discarded by the selective code measurement. The error can be reduced

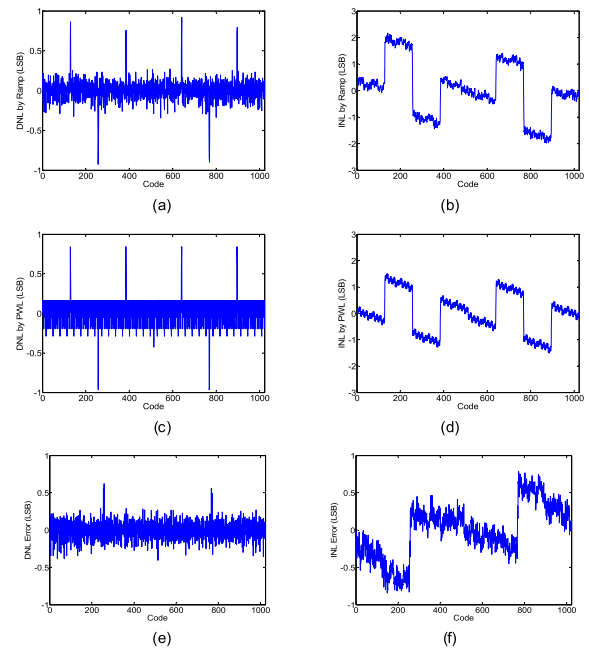


Fig. 11 The measured linearity results in the MisB configuration. (a) DNL by the ramp stimulus. (b) INL by the ramp stimulus. (c) DNL by the PWL stimulus. (d) INL by the PWL stimulus. (e) DNL error between two tests. (f) INL error between two tests in woMisCap configuration.

by introducing quick missing code test method [8] to filter out missing code samples or test more codes near the selective codes, saying code 254/257/766/769 with the expense of more test time.

5. Conclusion

The proposed embedded stimulus in a differential SAR ADC as a DFT enables a digital-in-digital-out test mechanism, which simplified the test interface design, for BIST applications in the SoC environment. The proposed DFT is implemented with 12.4-% area overhead, which is smaller than other previous work [4] in a 0.18- μm CMOS technology. The minimal measured DNL error ($0.2814/-0.3861$ LSB) verifies the feasibility of this proposed DFT.

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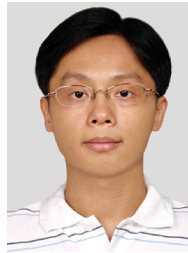
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