temperature variation, and clamp VDD close to a target level at runtime in spite of any given NBTI degradation and/or temperature variation within the specified ranges. As a result, active leakage power is reduced by 8%–10%, while dynamic power is reduced by 2.8%–3.7% for the given range of average die temperatures in early chip lifetime. Finally, we demonstrated that they maintain VDD close to a target level even in the presence of WID spatial process and temperature variations. VDD clamping helps to improve gate-oxide reliability. Oxide failure rate is reduced by 5% for the fast process corner and ~4% for the nominal and slow corners at \( t = 7.5 \) years.

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the input signal is sampled onto the sampling capacitors, capacitor array with a bridged capacitor. The reference DAC is a binary-weighted capacitor array which has better linearity than the C-2C capacitor array or the reference signal. The reference DAC is a binary-weighted capacitor array and the SAR ADC begins the conversion phase. The comparator control logic to control the reference switching of the DAC by the proposed switchback switching procedure.

The proposed capacitive DAC is split into two parts: a reference DAC and a sampling capacitor. The sampling capacitor controls the common-mode voltage to reference DAC, where

\[
V_{\text{ref}} = V_{\text{in}} \cdot \frac{1}{4} V_{\text{cm}} \]

and the comparator voltage supply to reference DAC, where

\[
E_{\text{avg, mono}} = \sum_{i=1}^{n-1} \left( \frac{n-1-i}{2} \right) CV_{\text{ref}}^2
\]

and

\[
E_{\text{avg, VCM}} = \sum_{i=1}^{n-1} \left( \frac{n-1-i}{2} \right) \left( V_{\text{ref}}^2 - C_{\text{ref}}^2 \right)
\]

where

\[
C_{\text{ref}} = \sum_{i=1}^{n} C_i
\]

and the common-mode voltage of the switchback switching procedure would be downward just for the first switching and then upward for the remainder. Hence, the maximum variation of the common-mode voltage is 1/4 \( V_{\text{ref}} \) and the common-mode voltage will gradually approach the common-mode voltage of the input signal \( V_{\text{cm}} \). It reduces the dynamic offset and the parasitic capacitance variation of the comparator.

As the monotonic switching procedure, the switchback switching procedure only switches a capacitor in each bit cycle, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. Moreover, the common-mode voltage of the switchback switching procedure is 1/4 \( V_{\text{ref}} \) and the common-mode voltage will gradually approach the common-mode voltage of the input signal \( V_{\text{cm}} \). It reduces the dynamic offset and the parasitic capacitance variation of the comparator.

Fig. 2 shows an example of the switchback switching method, where a 10-bit binary-weighted capacitive DAC is adopted and it is the same as the reference DAC adopted in Fig. 2. In order to simplify the illustration of the switchback switching method, the sampling capacitor of Fig. 2 is omitted in Fig. 3. The quantitative energy consumption of the three switching phases is shown. For the switchback switching method, the bottom plate of the MSB capacitor is connected to \( V_{\text{refp}} \) and the rest are connected to \( V_{\text{refn}} \) at the sampling phase. Then the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. After the MSB is determined, one MSB capacitor will switch to \( V_{\text{reff}} \). There is no energy consumption at this conversion step.

For an \( n \)-bit SAR ADC, if each digital output code is equiprobable, the average switching energy of the monotonic [2] and \( V_{\text{cm}} \)-based switching method [3] can be derived as

\[
E_{\text{avg, mono}} = \sum_{i=1}^{n-1} \left( \frac{n-1-i}{2} \right) CV_{\text{ref}}^2
\]

and

\[
E_{\text{avg, VCM}} = \sum_{i=1}^{n-1} \left( \frac{n-1-i}{2} \right) \left( V_{\text{ref}}^2 - C_{\text{ref}}^2 \right)
\]

where

\[
C_{\text{ref}} = \sum_{i=1}^{n} C_i
\]

and

\[
E_{\text{avg, switch}} = \sum_{i=1}^{n-2} \left( \frac{n-3-i}{2} \right) CV_{\text{ref}}^2
\]

For a 10-bit case, the monotonic and \( V_{\text{cm}} \)-based switching procedures consume 255.5 and 170.2 \( CV_{\text{ref}}^2 \), respectively, while the...
proposed switching procedure consumes only 127.5 \( CV_{\text{ref}}^2 \). The proposed technique thus requires 50% less switching energy than the monotonic one and 25% less than the \( V_{\text{cm}} \)-based one. Fig. 4 shows a comparison of switching energy for the four methods versus the output code.

Although the switchback switching method consumes less power than the monotonic and \( V_{\text{cm}} \)-based switching methods during the conversion phase. It must be pre-charged in the sampling phase. For a 10-bit case, if all of the switching methods sample the same input signal, the switchback switching method consumes 255.5 \( CV_{\text{ref}}^2 \). Fig. 4 also shows a comparison of switching energy for the four methods versus the output code when both sampling and conversion phase are calculated.

Accordingly, the switchback switching method may consume more power than the monotonic and \( V_{\text{cm}} \)-based switching methods if both sampling and conversion phases are taken into consideration. Nevertheless, it is worth to note that the switchback switching method reduces the design overhead of reference voltage circuit. The reason is for monotonic or \( V_{\text{cm}} \)-based switching methods, the MSB capacitor must settle to the reference voltage in a very short time during the conversion phase. The MSB capacitor of switchback switching method is pre-charged in the sampling phase which allows longer settling time than the conversion phase. Therefore, the switchback switching method does not require a fast-settling reference buffer to charge MSB capacitor in the conversion phase.

### III. Implementation of Key Building Blocks

#### A. S/H Circuit

The proposed SAR ADC samples input signal on the sampling capacitors, \( C_{sp} \) and \( C_{sn} \), via the bootstrapped switches, \( S_a \) and \( S_b \) [9].

The nonlinear variation of the parasitic capacitance during the conversion phase, induced by the sampling switch \( S_a \) and the comparator input pair, affects the linearity of the proposed SAR ADC. The top-plate parasitic capacitance of the sampling capacitor is a constant value, which does not affect the ADC performance. Fig. 5
shows the parasitic capacitance at the gate of the comparator input differential pair, $C_{gs} + C_{gd} + C_{gb}$. With the bootstrapped switch, a small-size sampling switch is adopted. During the conversion phase, the bootstrapped switch turns off and the parasitic capacitance of drain terminal, $C_{gd} + C_{ds}$, is smaller than 0.01 fF. Therefore, Fig. 5 just shows the simulated parasitic capacitance of the pre-amp input pair, which is the total capacitance of gate terminal. During the transition of the monotonic switching method, 0–0.5 $V_{ref}$, where $V_{ref}$ is $V_{refp} - V_{refn}$, the parasitic capacitance varies from 4.4 to 4.9 fF. Moreover, with the switchback switching method, the common-mode-voltage variation decreases from 0.5 to 0.25 $V_{ref}$. In this case, the parasitic capacitance varies from 4.74 to 4.9 fF.

The voltage of comparator input terminal, $V_{CMP}$, can be expressed as

$$V_{CMP} = V_{in} + \frac{C_{sp}}{C_{sp} + C_{p1}} V_{DAC}$$

$$= V_{in} + \left(1 - \frac{C_{p1}}{C_{total}} \frac{\Delta C_{p1}}{C_{total}}\right) V_{DAC} \quad (4)$$

where $C_{p1}$ is the parasitic capacitance at the comparator input terminal, including the top-plate parasitic capacitance of the sampling capacitor and the parasitic capacitance of the pre-amplifier. $C_{p1}'$ is the constant part of $C_{p1}$ and $\Delta C_{p1}$ is the variable part of $C_{p1}$. $V_{CMP}$ and $V_{DAC}$ are the voltages of the comparator input and reference DAC output, respectively. $V_{DAC}$ can be written as

$$V_{DAC} = \frac{9}{2^i - 1} \cdot C \cdot \frac{C_{sp} - C_{p1}}{C_{sp}} V_{ref} \quad (5)$$

If the parasitic capacitance $C_{p1}$ is a constant value ($\Delta C_{p1} = 0$), it can be regarded as a fixed gain error and does not affect the dynamic performance. However, $C_{p1}$ here is not a constant value. During the conversion process, $\Delta C_{p1}$ is 0.16 fF, which affects the ADC linearity. To achieve 10-bit linearity, assume the maximum error due to $\Delta C_{p1}$ must be smaller than 0.5 LSB. From (4), the minimum capacitance of the sampling capacitor $C_{sp}$ is 328 fF. According to (5), the minimum unit capacitance $C$ is 0.64 fF. If the monotonic switching method is adopted, the minimum capacitance of the sampling capacitor $C_{sp}$ is 1025 fF. With the proposed switching method, the minimum input capacitance decrease from 1025 to 328 fF. For routing parasitic capacitance, process variation and matching issues, the adopted values of $C_{sp}$ and $C$ are 400 and 5 fF, respectively. The sampling capacitors and reference DAC are metal-oxide-metal capacitors [2].

B. Dynamic Comparator

Fig. 6 shows the schematic of the comparator which consists of a pre-amplifier and a dynamic latched comparator. With a low sampling capacitance, the kickback noise originated from the latched comparator becomes more critical. Furthermore, the bottom plate of the sampling capacitors, $C_{sp}$ and $C_{sn}$, are floating and hence sampling capacitors are more sensitive to kickback noise than the conventional case. Therefore, the proposed comparator adopts a pre-amplifier to block the kickback noise and enhance the comparison speed.

C. SAR Control Logic

To avoid a high-frequency clock generator and a pulse-width modulator (PWM), the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals [5]. Fig. 7 shows a schematic and a timing diagram of the asynchronous phase generator. The conversion process starts once the system clock is switched to low. Sample is the sample signal which turns on the sampling switches. After ten comparisons, Sample will be set to high to sample the input signal until the system clock, Clk, switches to low. Therefore, the duty cycle of the system clock, Clk, is 50% and no PWM is needed for the integration application. The dynamic
TABLE II

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<td>8.18@39 MHz</td>
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IV. MEASUREMENT RESULTS

The ADC was fabricated in a 1P9M 90-nm CMOS technology. The micrograph of the ADC core is shown in Fig. 8. The ADC core only occupies an area of $525 \times 190 \mu m^2$. The ADC has a 1.2-V peak-to-peak differential input range. The measurement results of the prototype are presented below.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 9. The peak DNL and INL are $-0.66/0.88$ and $-1.27/1.32$ LSB, respectively.

Fig. 10 shows the measured fast Fourier transform spectrum with an input frequency close to 2 MHz at a 1-V supply and a 30-MS/s sampling rate. The measured signal-to-noise distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 52.25 and 68.15 dB, respectively.

Fig. 11 plots the measured SNDR and SFDR versus the input frequency at 30 MS/s. At a low input frequency, the measured SNDR and SFDR are 58.89 and 68.65 dB, respectively. The resultant ENOB is 9.16 bits. When the input frequency increases to 15 MHz, the measured SNDR and SFDR are 53.99 and 68.11 dB, respectively. The effective resolution bandwidth is higher than 15 MHz.

Fig. 12 shows the measured performance versus the sampling frequency with a 0.5-MHz sinusoidal stimulus. When the sampling rate was 10 MS/s, the SNDR and SFDR were 57.13 and 68.17 dB, respectively. When the sampling rate was over 30 MS/s, the performance rapidly degrades because the time for input signal sampling was insufficient.

At a 1.0-V supply and 30 MS/s, the analog part, including the S/H circuit and dynamic comparator, consumes 0.55 mW. The switching power of the DAC draws 0.08 mW and the digital control logic consumes 0.35 mW. The pre-amplifier depletes most of the analog power (76%) because it consumes static power consumption. The proposed switching sequence reduces the power consumption significantly; it just occupies 8.1% of the total power. Excluding analog power (76%) because it consumes static power consumption.

Table II compares the proposed ADC with other state-of-the-art SAR ADCs [2], [3], [6]–[8]. To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known figure-of-merit (FOM) equation is used

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min \{2 \times \text{ERBW}, f_s\}}.$$  

(6)

The FOM of the proposed ADC is 57 fJ/conversion-step at 30 MS/s and a 1.0-V supply. The pre-amplifier consumes 0.46 mW, which makes the FOM larger than the other works. Nevertheless, if the power consumption of the front-end buffer and reference buffer is considered, the FOM of the proposed ADC will be lower than the other works.

V. CONCLUSION

In this brief, a SAR ADC with a new switching method was presented. The proposed switching procedure reduces the parasitic capacitance variation and the comparator dynamic offset induced by input common-mode-voltage variation. The input capacitance of the proposed ADC is just 0.4 pF, which reduces the power consumption and design effort of the front-end buffer. The prototype occupies an active area of 0.1 mm², and achieves a 30-MS/s operation speed with power consumption less than 1 mW, resulting in an FOM of 57 fJ/conversion-step.

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