A 9-Bit 150-MS/s Subrange ADC Based on SAR Architecture in 90-nm CMOS

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***Abstract*—This paper presents a 9-bit subrange analog-to-digital converter (ADC) consisting of a 3.5-bit flash coarse ADC, a 6-bit successive-approximation-register (SAR) fine ADC, and a differential segmented capacitive digital-to-analog converter (DAC). The flash ADC controls the thermometer coarse capacitors of the DAC and the SAR ADC controls the binary fine ones. Both theoretical analysis and behavioral simulations show that the differential non-linearity (DNL) of a SAR ADC with a segmented DAC is better than that of a binary ADC. The merged switching of the coarse capacitors significantly enhances overall operation speed. At 150 MS/s, the ADC consumes 1.53 mW from a 1.2-V supply. The effective number of bits (ENOB) is 8.69 bits and the effective resolution bandwidth (ERBW) is 100 MHz. With a 1.3-V supply voltage, the sampling rate is 200 MS/s with 2.2-mW power consumption. The ENOB is 8.66 bits and the ERBW is 100 MHz. The FOMs at 1.3 V and 200 MS/s, 1.2 V and 150 MS/s and 1 V and 100 MS/s are 27.2, 24.7, and 17.7 fJ/conversion-step, respectively.**

***Index Terms*—Flash ADC, hybrid ADC, SAR ADC, subrange ADC, two-step ADC.**

I. Introduction

IN THE EARLY days of integrated circuits, high-accuracy amplifier design was difficult due to poor transistor characteristics. The successive-approximation-register (SAR) analog-to-digital converter (ADC), which does not require amplifiers, became a dominant architecture [1], [2]. Then, with progress in CMOS technologies, many other ADC architectures became popular and the SAR architecture became one of many possible options, often employed in low-speed applications. As the transistor feature size dramatically scales down, achieving high gain again becomes difficult. Short-channel transistors suffer from drain-induced barrier lowering which reduces the intrinsic gain.

Recently, the SAR ADCs have received renewed attention due to their excellent power efficiency and low-voltage potential compared to pipelined and cyclic ADCs. Various design techniques and structural modifications improve the SAR architecture [3]–[16]. These prototypes cover wide ranges of sampling speed, from 5 to 12 bits, and resolution, from several hundred kS/s to several hundred MS/s. Process technology affects the operation speed of SAR ADCs. For two identical designs, the one fabricated with better technology will achieve higher operation speed due to shorter gate delay. Breaking through the speed bottleneck is urgent to alleviate the need for expensive CMOS technologies.

This paper presents a subranged SAR ADC design that uses a coarse flash ADC to enhance the conversion speed of coarse bits. The proposed subrange ADC achieves a higher sampling rate than a conventional SAR ADC. The rest of this paper is organized as follows: Section II discusses the design considerations for a SAR ADC with the monotonic switching method. Section III presents the design concept of the subranged SAR ADC. Section IV describes the details of the flash-SAR ADC architecture and building blocks. Section V shows the experimental results of a 9-bit proof-of-concept prototype. Finally, we draw a conclusion in Section VI.

II. Design Considerations for SAR ADCs Using the Monotonic Switching Method

Fig. 1 shows a SAR ADC with the monotonic switching procedure which can be either upward or downward. For fast reference settling, i.e., discharging through n-type transistors, this work selects the downward switching. The ADC samples the input signal on the top plates and the comparator inputs are connected to the top plates of the capacitive digital-to-analog converter (DAC). At the same time, the bottom plates of the capacitors are reset to V_{refp}. After sampling, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor on the higher voltage potential side is switched to V_{refn} and the other one on the lower voltage potential side remains unchanged. The ADC repeats the procedure until the LSB is decided.

Fig. 2 shows the waveforms of the conventional and monotonic switching methods. In each bit cycle, there is only one capacitor switching which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. This ADC samples the signal on the top plates, allowing the comparator to perform the first comparison without any capacitor switching. For an n-bit ADC, the ADC performs n comparisons and n-1 DAC switchings, reducing the number of unit capacitors by half. Thus, the number of unit capacitors in a capacitor array is 2^{n-1}. A flow chart of the monotonic successive-approximation procedure is shown in Fig. 3.

Since a SAR ADC with the monotonic switching method only requires half the number of unit capacitors of a conventional ADC, there is 50% capacitor area reduction. The monotonic

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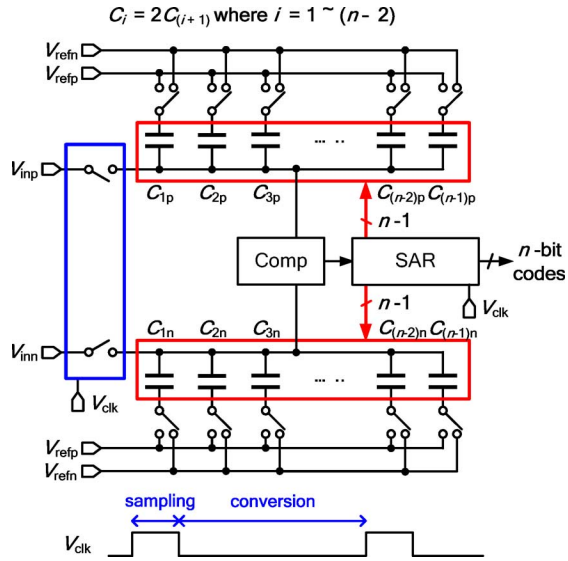


Fig. 1. A SAR ADC with monotonic switching method.

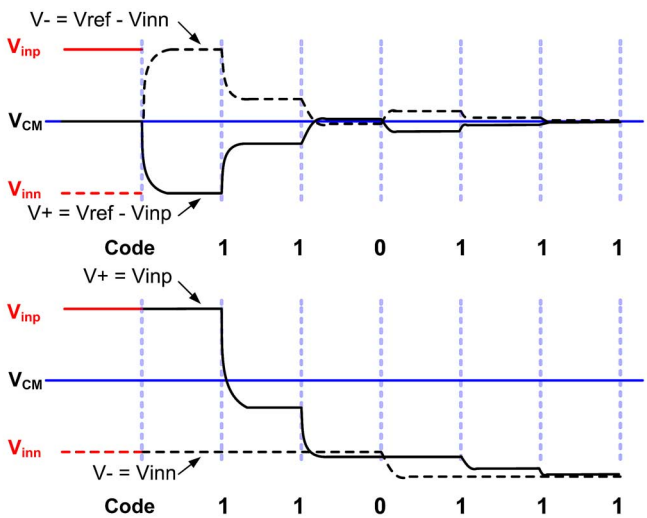


Fig. 2. Waveforms of (top) conventional and (bottom) monotonic switching methods.

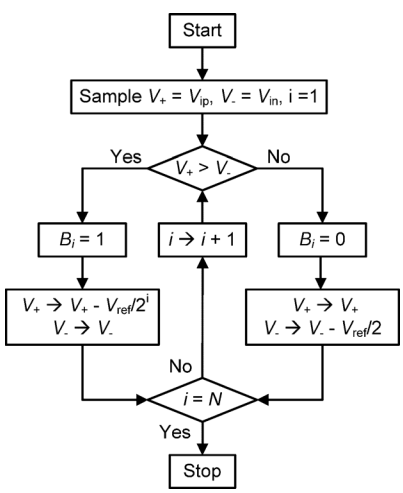


Fig. 3. Flow chart of the monotonic switching method.

switching method does not use the conventional trial-and-error switching procedures and only switches a capacitor for each bit cycle, resulting in a power reduction of up to 81% [3].

The basic building blocks of such a SAR ADC are a sampling switch, a comparator, a capacitive DAC, and digital control logic. The classic bootstrapped switch provides accurate sampling even under low-voltage conditions [17]. Compared to amplifier-based ADCs like pipelined and cyclic ADCs, the better power efficiency of the SAR ADC comes from the short operation time of the core block, the comparator. A latch-based comparator only turns on for a short period when its trigger arrives. The mismatches between paired devices generate an offset. The random offset voltage of a differential pair can be expressed as [18]

$$V_{\rm os} = \Delta V_{\rm TH1,2} + 0.5(V_{\rm GS} - V_{\rm TH})_{1,2}(\Delta S_{1,2}/S_{1,2} + \Delta R/R) \quad (1)$$

where $\Delta V_{\rm TH1,2}$ is the threshold voltage offset of the differential pair, $(V_{\rm GS} - V_{\rm TH})_{1,2}$ is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between the input transistors, and ΔR is the loading resistance mismatch of the loading transistors. The first term is a static value and the value of the second term is proportional to the effective voltage of the input pair. In flash, folding and binary-search ADCs, random offsets of comparators make reference intervals unequal. Averaging and calibration can overcome offsets in these ADCs [19], [20]. For non-multi-bit/step SAR ADCs, the comparator offset only causes the shift of the entire transfer curve. The second term varies with the gate-to-source voltage of the input pair transistor. For the monotonic switching method [3], the common-mode voltage changes during bit cycling. The resultant offset variation degrades the accuracy of SAR ADCs with this switching method.

The comparator design of the proposed ADC is described below. Because the common-mode voltage gradually approaches the negative reference, a p-type comparator, as shown in Fig. 4, is more suitable than an n-type one [3]. Generally, a tail current is not necessary for a comparator. Nonetheless, the following simulations show that the tail current plays a significant role in accuracy improvement. Fig. 5(a) shows the simulated gate-to-source voltages versus the input common-mode voltage where the case with a current source has a smaller voltage change. Fig. 5(b) shows the comparator offsets with respect to the input common-mode voltage where each node is the standard deviation of 50 Monte Carlo simulations based on the foundry mismatch model. The figure clearly shows that a comparator with a current source has smaller random offset variation.

The second non-ideality that originates from the comparator is the gate parasitic capacitance of the input pair. The gate nodes are connected to the top plates of the capacitive DAC. Some parasitic components such as the depletion and junction capacitances vary with the bias condition whereas the capacitance of metal-oxide-metal (MOM) capacitors or metal-insulator-metal (MIM) capacitors in the DAC has stronger immunity against environmental changes like temperature and voltage. During the conversion phases, the top plates of the DAC are floating. The parasitic capacitance variation affects the top-plate voltage owing to charge conservation. The right side of Fig. 4 depicts the linear comparator model for capacitance simulation.

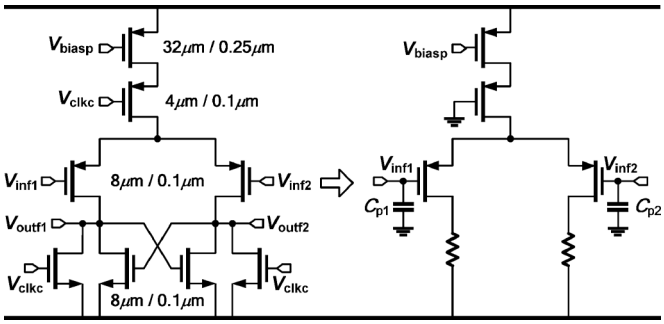
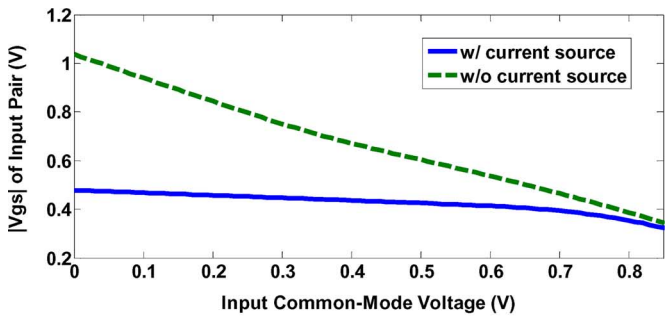
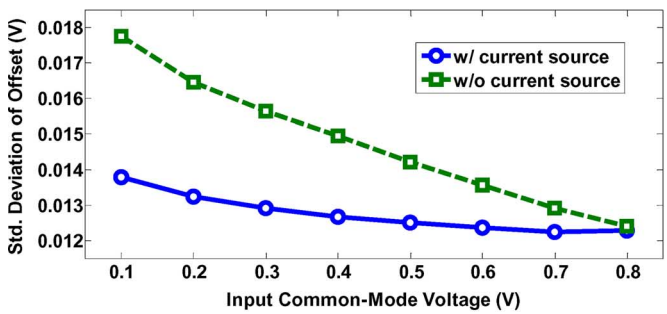


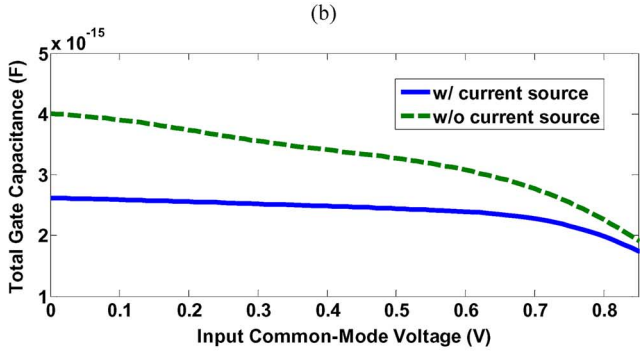
Fig. 4. Comparator of (left) the SAR ADC and (right) its equivalent linear model.



(a)



(b)



(c)

Fig. 5. Simulation results (blue solid) with and (green dashed) without a static current source: (a) gate-to-source voltage, (b) standard deviation of random offset, and (c) total gate capacitance.

Fig. 5(c) shows the change of the total gate capacitance with input common-mode voltage. The charge sharing between the gate capacitance and DAC capacitance affects the reserved voltage. For example, assume a small swing differential signal near the initial input common-mode voltage, 0.6 V, is sampled onto the top plates of the DAC where the parasitic capacitance is 3 fF, as shown in Fig. 5(c). After several conversion phases, the input common-mode voltage gradually approaches the negative reference voltage, reaching 0.1 V. The parasitic

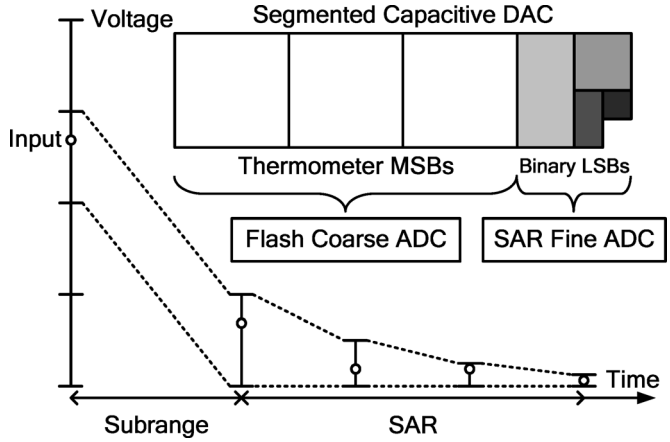


Fig. 6. Concept of proposed subranged SAR ADC.

capacitance approximates to 4 fF. The 1-fF difference slightly lowers the residue voltage in later stages of the DAC, and hence affects accuracy. To alleviate this effect, the DAC capacitance should be larger than the parasitic capacitance, so one must either enlarge the DAC capacitance or reduce the input pair size.

The accuracy of a SAR ADC also relies on the DAC matching. Recent state-of-the-art works adopt purely capacitive DACs to reduce power dissipation [8], [9]. In general, a binary-weighted DAC has better intrinsic matching than C-2C and split DACs, which usually require calibration or post-processing [10], [11]. However, the total capacitance of a binary-weighted DAC grows exponentially with resolution. For high-resolution cases, the ratio between the MSB and LSB capacitors is disproportionate. The MSB capacitors are too large to be driven and LSB capacitors are sensitive to parasitic effects. Due to this tradeoff, the selection of the unit capacitance is critical. The switching of large capacitors requires a long settling time, thus limiting operation speed. The mismatches between MSB and LSB capacitors degrade differential non-linearity (DNL) [21]. Due to parasitic effects and process variations, the DNL possibly shows large steps or spurs during the first few MSB transitions, e.g., at 128, 256, and 384 in the 9-bit case.

The aforementioned problems pose performance bottlenecks for a SAR ADC. Although the comparator with a tail current alleviates part of the accuracy problem, the speed issue still exists. The proposed subrange architecture provides accuracy improvement and speed enhancement with the assistance of a low-resolution flash coarse ADC (CADC).

III. Subrange ADC Composed of Flash and SAR ADCs

Flash and folding ADCs are high speed and power hungry whereas SAR ADCs are low speed and power efficient. A hybrid structure achieves a good compromise between speed and power consumption. If an ADC consists of two sub-ADCs, it is either subrange or two-step. A two-step ADC amplifies the residue of the CADC whereas a subrange ADC does not. A two-step ADC requires a closed-loop opamp or an open-loop amplifier for residue amplification. Accurate amplification requires a high-performance opamp, resulting in large power consumption. The open-loop approach usually requires calibration

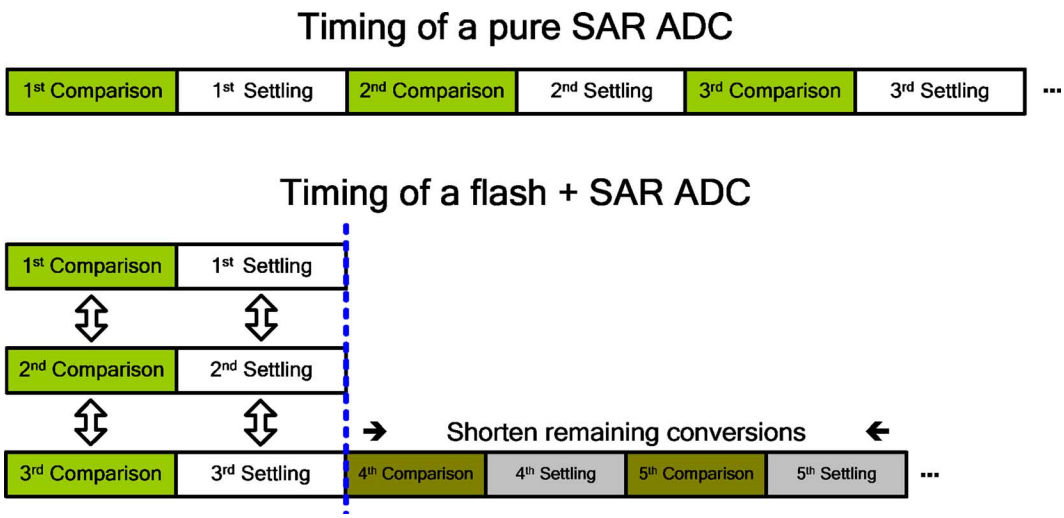


Fig. 7. Comparison of timing diagrams of a SAR ADC and a subranged ADC.

or post-processing to correct distortion or gain error, leading to a large core area and high complexity. The subrange architecture is used to avoid opamp and calibration.

Traditionally, a subrange ADC consists of a flash CADC and a flash fine ADC (FADC) [22]. The switching network for the FADC requires many analog switches for connecting the static references to the FADC input. Due to the complicated switching network, this ADC structure rarely achieves a high resolution. The present work uses a new combination: a flash CADC plus a SAR FADC. This hybrid structure exploits the high speed of a flash ADC and the low power of a SAR ADC. The CADC is designed with very relaxed accuracy due to redundancy. Consequently, this sampling speed of this ADC is higher than that of pure SAR ADCs with little additional power and hardware overhead.

When a DAC switches, a SAR ADC must wait until the DAC voltage settles to the required accuracy before the next comparison begins. For example, the second comparison must wait for the MSB to settle. The MSB capacitance of a binary DAC is equal to the sum of all the other LSBs. The settling of the first few large capacitors is a speed bottleneck. Although a binary DAC has simpler control circuit than a thermometer one, it exhibits large spurs during first few code transitions. On the other hand, a fully thermometer DAC requires a relatively complicated decoder. A good compromise is the so-called segmented DAC which consists of thermometer MSBs and binary LSBs. A segmented DAC has a simple control circuit and moderate linearity simultaneously. In this design, the flash-SAR hybrid ADC converts the capacitor DAC into a segmented one.

Fig. 6 depicts the concept of the proposed subranged SAR ADC. A flash ADC controls the thermometer capacitors, and a SAR ADC handles the binary ones. The flash ADC performs the first comparison to determine the subrange where the input signal is located. According to the output of the flash ADC, the ADC pulls down a number of thermometer coarse capacitors. Then, the input range of the subsequent SAR ADC becomes smaller. In the 2-bit CADC case, the input range reduces by a factor of 4. The hardware and power consumption of a flash ADC has an exponential relation with resolution. The overhead of 3- or 4-bit flash ADCs is small. Using a 5-bit or above flash ADC as a CADC is very expensive due to the large component count.

The proposed ADC has the advantages of a SAR ADC including good power efficiency and small area, while improving speed and accuracy. Fig. 7 shows a comparison of timing diagrams of a pure SAR ADC and the proposed one. A pure SAR ADC has to wait for the first capacitor switching to settle before the second comparison is made. Take a 9-bit SAR ADC as an example. The MSB capacitor is 256 times larger than the LSB capacitor. Assume the capacitor settling behavior is simple first-order RC settling. The driving capability of the digital buffer for the MSB capacitor must be 256 times larger than that of the LSB one for a given RC time constant. The driving buffer thus becomes extremely large. The proposed ADC overlaps the first few MSB settlings. Hence, there is only one critical capacitor settling. Moreover, the accuracy of the first comparison is relaxed because the ADC has redundancy. A SAR ADC must set a delay time to estimate the required DAC settling time. If the delay time is fixed for each conversion, its value is decided based on the worst case, usually the MSB switching. In this ADC, the settling of the FADC is less critical and hence the delay time can be further shortened.

Besides the comparator offset, the mismatch of the capacitor DAC is a main error source which deteriorates ADC linearity. The maximum DNL and integral non-linearity (INL) errors of a SAR ADC with the monotonic switching method are identical, and can be expressed as

$$\sigma_{\mathrm{maxDNL,binary}}(\mathrm{LSB}) = \frac{\sigma_0\sqrt{2^{b-1}}}{C_0} \tag{2}$$

where C_0 is the unit capacitance, σ_0 is the standard deviation of the random offset of a unit capacitor and b is the ADC resolution. A detailed derivation procedure is given in the Appendix.

The same derivation procedures are applied to the proposed flash-SAR structure to evaluate the maximum INL and DNL. For a flash-SAR ADC with redundancy, i.e., the flash CADC resolves non-integer bits, e.g., 1.5 bits, the INL error is the same as that of the monotonic case and the DNL error is calculated as

$$\sigma_{\mathrm{maxDNL,hybrid}}(\mathrm{LSB}) = \sqrt{\frac{3}{2^{T_c}}} \times \sigma_{\mathrm{maxDNL,binary}} \tag{3}$$

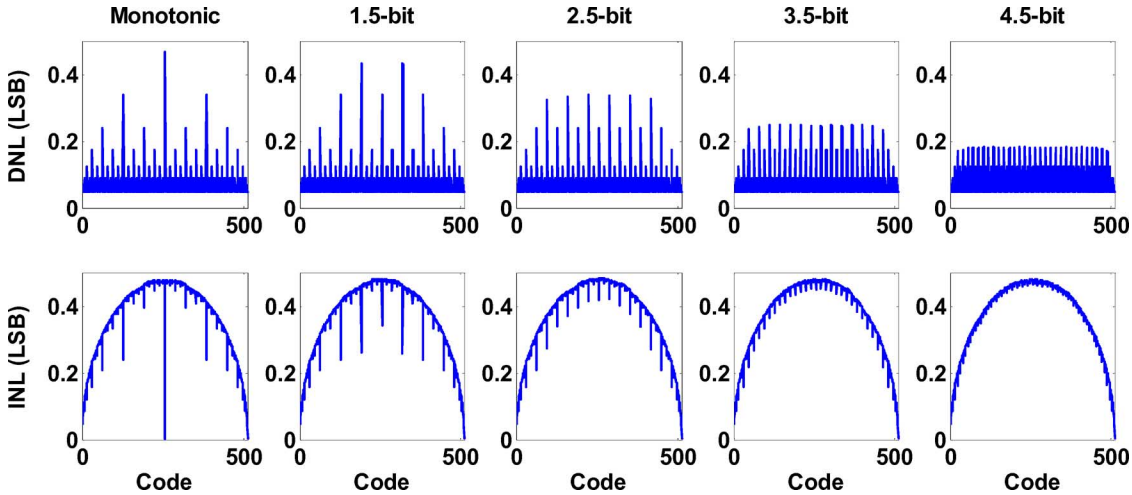


Fig. 8. Static performance of a SAR ADC using the monotonic switching method and proposed flash-SAR ADCs with different CADC resolutions.

where $T_c = \lceil T \rceil$ is the ceiling function value of T and T is the resolution of the coarse flash ADC.

Fig. 8 shows the behavioral simulations for the SAR ADC with the monotonic switching method (fully binary) and flash-SAR subrange ADCs for various CADC resolutions (1.5, 2.5, 3.5, and 4.5 bits). Because the two ends are fit to zero, the INL has a parabola shape. Each capacitor cell has a Gaussian random error with a standard deviation of 3%. Note the INL curves in Fig. 8 show spikes whose peak values decrease with the CADC resolution. The monotonic switching method performs the first comparison without any capacitor switching, i.e., the only error source in these simulations, so the sampled signals on DAC plates remain ideal. Since the comparator is also assumed to be ideal, it does not make any wrong decision. In other words, the MSB decision of the SAR ADC is errorless, so the middle of the INL curve in the monotonic case reaches 0. The DNL and INL curves are the root-mean-square (rms) values of 10 000 simulations. The simulations show the peak INL values of these cases are very close, as expected from the theoretical analysis. The peak DNL values decrease with increasing CADC resolution. Although a high-resolution CADC enhances DNL performance, the design complexity and overhead of the flash CADC should be considered.

IV. Prototype Design: ADC and Building Blocks

A. ADC Architecture

Fig. 9 depicts the block diagram of the prototype consisting of a 3.5-bit flash ADC, a 6-bit SAR ADC, and a differential segmented capacitive DAC. This architecture is very similar to a pipelined stage except for the non-amplified residue. The CADC serves as the sub-ADC, and the capacitor array behaves like a MDAC performing the subtraction of the input signal from a reference voltage according to the sub-ADC output. The total thermometer capacitance is 224C (14×16C) and the fine capacitance is 31C ($16\text{C} + 8\text{C} + 4\text{C} + 2\text{C} + 1\text{C}$), so the capacitance ratio between the thermometer and binary capacitors is around 7. After the first capacitor switching, only 12.5% of the total capacitance is left for the SAR FADC. In contrast, a pure SAR leaves 50% capacitance after the first comparison. Thus, the FADC does not suffer from the settling problem. The comparators determine 15 subranges. The top and bottom subranges are 1.5 times wider than the others. This architecture tolerates an offset of a coarse comparator of up to $\pm 1/32$ the full-scale input range. Hence, the accuracy requirement of the CADC is greatly relaxed. The flash CADC has a simple passive track-and-hold (T/H) circuit composed of a sampling switch and a capacitor on each side. The switching activities of the coarse comparators deteriorate the sampled input signal on the capacitor. Hence, preamplifiers are inserted between the sampling capacitors of the T/H circuit and the comparators to block the kickback noise of the coarse comparators.

Fig. 9 also shows the timing diagram of this ADC where $V_{\rm clks}$ is the sampling clock, $V_{\rm clkp}$ is the clock of the preamplifiers and $V_{\rm clkr}$ is the clock of the FADC. $V_{\rm clks}$ is the control signal of the sampling switches of the CADC and FADC. After $V_{\rm clks}$ falls, the ADC starts the coarse conversion. Since the preamplifiers turn on only before the coarse conversion and immediately turn off after the coarse conversion, a tail current switch is added for each preamplifier. After the coarse conversion, the ADC continues for 6 fine conversions. The time durations of these steps are also shown in Fig. 9. The coarse conversion only takes 15% of the total time, even though around 4 bits are resolved in this step. Each fine conversion on average takes 11% of the total time, a value close to the coarse conversion time.

The proposed ADC employs the switching scheme presented in [3], where the comparator input common-mode voltage gradually approaches the negative reference voltage ($V_{\rm refn}$) during conversions. The change of the input common-mode voltage is up to half of the input swing. In other words, the comparator offset at the first bit cycle and the last one are different. The dynamic offset degrades the linearity of a SAR with such a switching scheme. In this work, after the first DAC switching, the input range is pulled down to 1/8 the original value. The comparator offset becomes much smaller than the original value. The reduced input range of the FADC increases the accuracy of fine conversions. According to the data in Fig. 5(b), the change of offset standard deviation is only 0.6 mV in the case where the comparator has a current source.

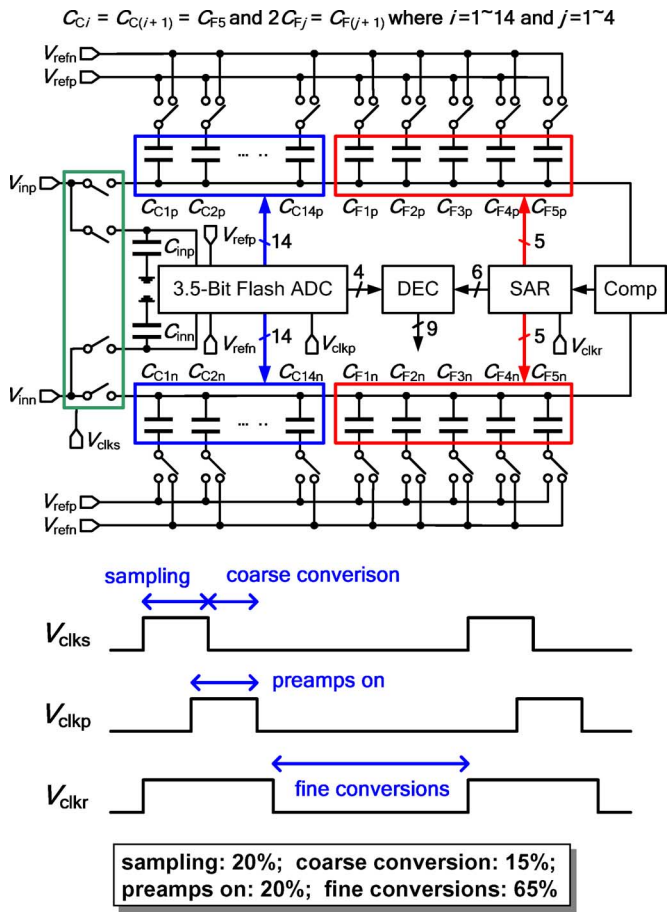


Fig. 9. Block diagram of the proposed ADC (top) and its timing diagram.

B. Asynchronous Clock Generator

As shown in Fig. 10, the work uses an asynchronous clock generator, similar to the one in [3], to produce internal control signals for SAR logic and capacitors. $V_{\rm valid}$ is the OR result of the two outputs of the fine comparator. In the comparator reset phase, its value is logic 0. $V_{\rm clkc}$ is the trigger signal for the p-type fine comparator which is the OR result of sampling signal $V_{\rm clkr}$, $V_{\rm valid}$ and $V_{\rm clk6}$. When $V_{\rm clkc}$ goes low, the fine comparison begins. After the comparator makes the decision and then a predefined delay, the fine comparator resets both output nodes. $V_{\rm clk1\sim6}$ are the control signals for capacitors.

C. Coarse ADC Design

The 3.5-bit flash ADC is composed of a T/H circuit, a reference ladder, 8 preamplifiers, 14 comparators, and an encoder as shown in Fig. 11. Note the T/H circuit and input signal path are not shown in this figure. To reduce the accuracy requirement of the CADC, a certain redundancy for the CADC is required. The whole ADC is capable of tolerating a wrong decision made by the CADC. This architecture uses an error correction method similar to that of the pipelined ADC [23]. The coarse stage of this ADC resolves non-integer bits. A comparator in a 3.5-bit CADC can tolerate an offset of $\pm 1/32$ the input range. For a 2-V peak-to-peak differential input swing, a coarse comparator has a tolerable offset range of ± 62.5 mV.

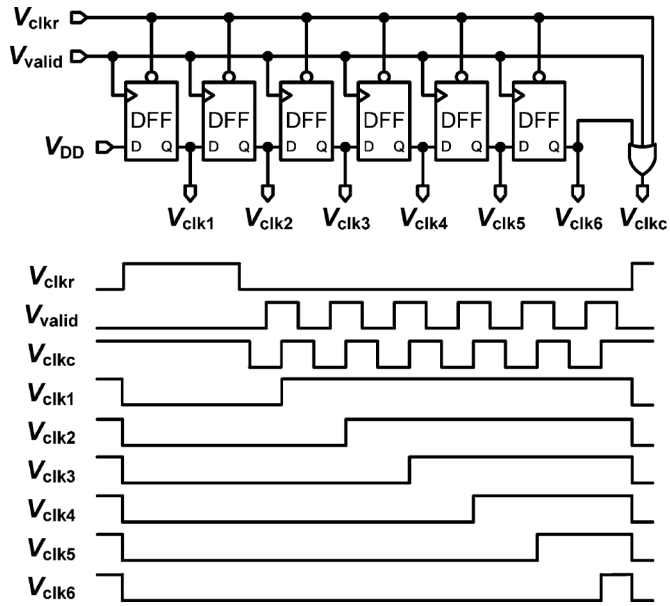


Fig. 10. Clock generator of the FADC (top) and its timing diagram.

D. Comparators of Coarse and Fine ADCs

To prevent the kickback noise of the coarse comparators from deteriorating the signal on the sampling capacitors, preamplifiers are placed between the capacitors and the comparators. Due to the interpolation technique, the CADC only needs 8 preamplifiers. Figs. 12 and 13 show the preamplifier and comparator of the flash ADC, respectively. The sizing of the preamplifier only has to satisfy the static offset constraint where the threshold voltage mismatch dominates. The threshold voltage mismatch is expressed as

$$\sigma V_{\rm TH} = \frac{A_{\rm VTH}}{\sqrt{WL}} \tag{4}$$

where W is the transistor width, L is the transistor length, and $A_{\rm VTH}$ is a process dependent parameter, which is usually less than 5 mV.μm in a 90-nm technology. Since the coarse comparator can tolerate around ± 62.5 mV for a 2-$V_{\rm pp}$ input swing, the input transistors can be small.

Unlike the cross-coupled inverters in the coarse comparator, there is only a pair of cross-coupled NMOS transistors in the fine comparator. When the input common-mode voltage of the p-type input pair gradually approaches the negative reference, the stacked NMOS and PMOS transistors slow down the comparison. Hence, the fine comparator uses a simpler structure. As stated previously, the input range of the FDAC is pulled down to 1/8 of the full range. In other words, the subrange architecture reduces the effective voltage variation of the fine comparator.

V. Experimental Results

Fig. 14 shows the proof-of-concept prototype fabricated in a 1P9M 90-nm CMOS process where the top two layers are thick metals [16]. This ADC occupies an active area of 0.028 mm^2. The capacitive DAC consists of 2.2-fF fingered sandwich metal-oxide-metal (MOM) unit capacitors. The top plates of all the unit capacitors are connected to the fine comparator inputs

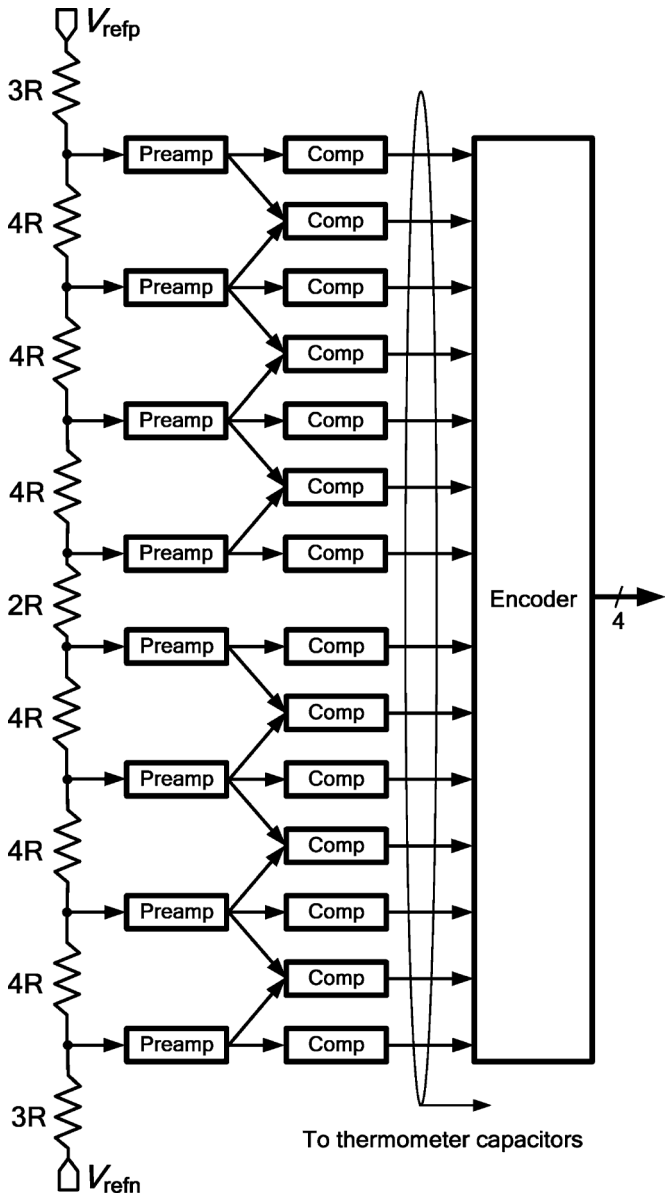


Fig. 11. Block diagram of the coarse ADC.

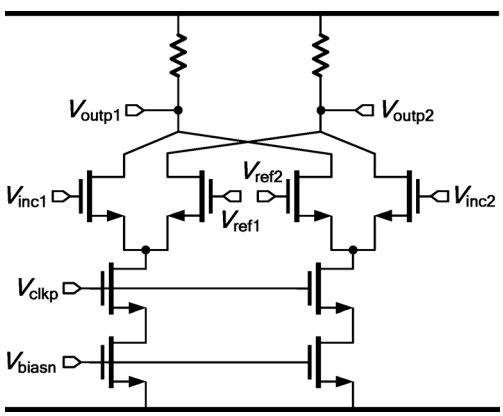


Fig. 12. Preamplifier of the coarse ADC.

and the bottom plates are connected to reference voltages, $V_{\rm refp}$ and $V_{\rm refn}$. The inputs of the fine comparator are directly connected to the top plates of the arrays. The parasitic capacitance

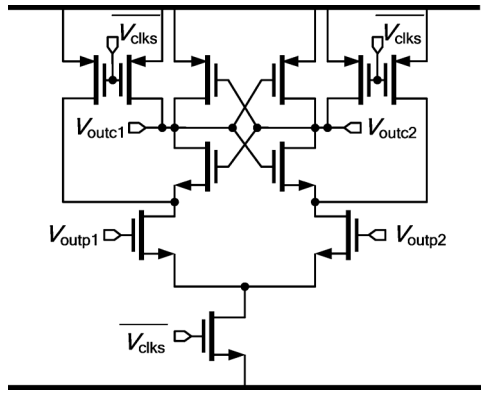


Fig. 13. Comparator of the coarse ADC.

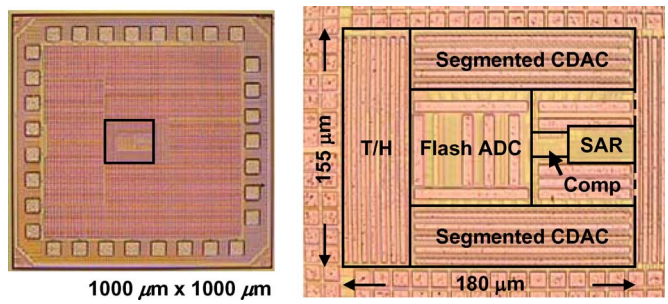


Fig. 14. Chip micrograph.

at the top nodes of the capacitor arrays contains the input capacitance of the comparator and the routing capacitance which are not switchable during bit cycling. Hence, the parasitic capacitance causes a gain error. Because the CADC and FADC of the proposed ADC should have the same input range, the parasitic capacitance should be minimized. The unit capacitor consists of three thin-metal layers to reduce metal-to-substrate parasitic capacitance. The top plate uses the 6th metal and the bottom plate consists of the 5th to 7th metals. The 6th metal is used to construct the finger structure. Except necessary top routing, the bottom plate encages the top plate to reduce the to-substrate parasitic capacitance of the top plate.

At 150-MS/s, the ADC consumes 1.53 mW from a 1.2-V supply voltage. The sampling circuits, CADC and the resistor ladder consume 0.7 mW. The FADC and other digital logic consume 0.67 mW. The digital buffers for capacitor switching dissipate 0.16 mW. The peak-to-peak differential input swing of this ADC is 2 V. Fig. 15 shows the peak values of DNL and INL are $-0.48/0.35$ and $-0.48/0.44$ LSB, respectively. For pure SAR ADCs, the static measurement results usually show large spurs during the MSB transitions. Due to the segmented DAC and sufficient unit capacitor matching, the DNL and INL charts do not show any large spur in MSB transitions. Fig. 16 shows the measured spectrum for a 1-MHz input, and Fig. 17 shows the spectrum for a 50-MHz input. Fig. 18 depicts the SNDR and SFDR plots versus input frequency for a 1.2-V supply. The peak SNDR is 54.07 dB and the peak SFDR is 72.75 dB. The high SFDR demonstrates the excellent linearity of the ADC. With a 1.3-V supply, as shown in Fig. 19, the sampling rate is 200 MS/s. The ENOB is 8.66 bits and the ERBW is 100 MHz. At 200 MS/s and 150-MS/s, the prototype has FOMs of 27.2 and 24.7 fJ/conversion-step, repectively. At 1-V 100-MS/s, the FOM is even lower, 17.7 fJ/conversion-step. Table I shows a

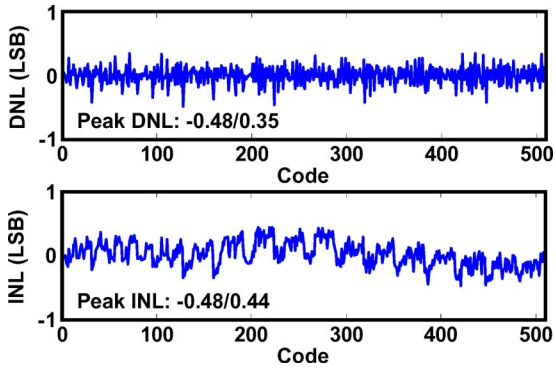


Fig. 15. Measured DNL and INL.

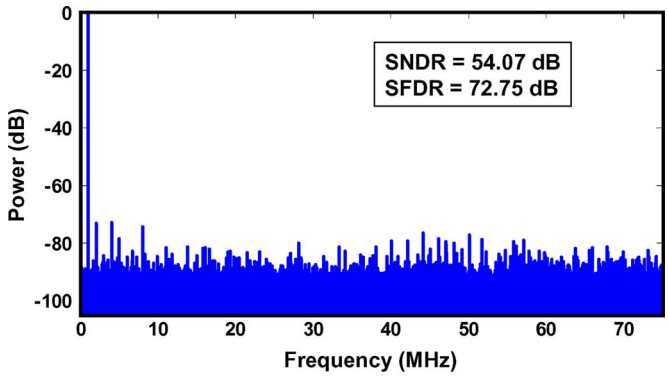


Fig. 16. Measured spectrum at 1-MHz input and 150 MS/s.

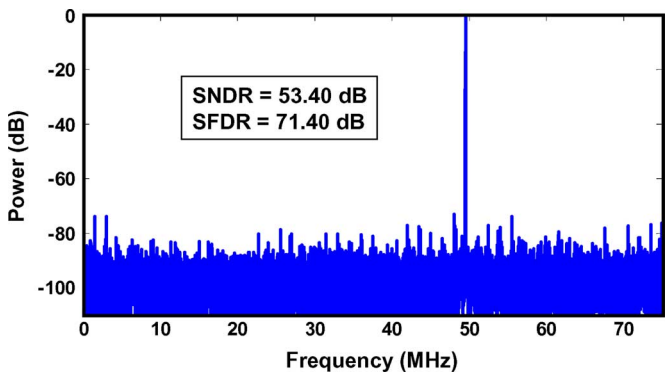


Fig. 17. Measured spectrum at 50-MHz input and 150 MS/s.

specification summary and a comparison to state-of-the-art 9-bit and 10-bit ADCs [3], [8], [11]–[13], [15]. The FOM is calculated based on the well-known equation

$$\mathrm{FOM}_{1,2} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}_{1,2}} \times \min(2 \times \mathrm{ERBW}, \mathrm{f_s})} \tag{5}$$

where ENOB_1 is the effective number of bits at low input frequency and ENOB_2 is the value at the ERBW or higher input frequency. FOM_1 and FOM_2 are figures of merit derived according to ENOB_1 and ENOB_2, respectively. Compared to other ADCs in Table I, the proposed ADC has the highest sampling rate while maintaining excellent power efficiency.

VI. Conclusion

A flash ADC is high speed and high power while a SAR ADC is opposite. The proposed 9-bit hybrid architecture exploits the high speed of a flash ADC and low power of a SAR ADC. The low-complexity, low-power flash ADC enhances the overall speed by merging the switching of the first three MSBs. The small input range and low resolution of the SAR ADC enables high-accuracy and high-speed operation. Without any calibration, the measurement results show this ADC achieves high accuracy, high operation speed and high power efficiency.

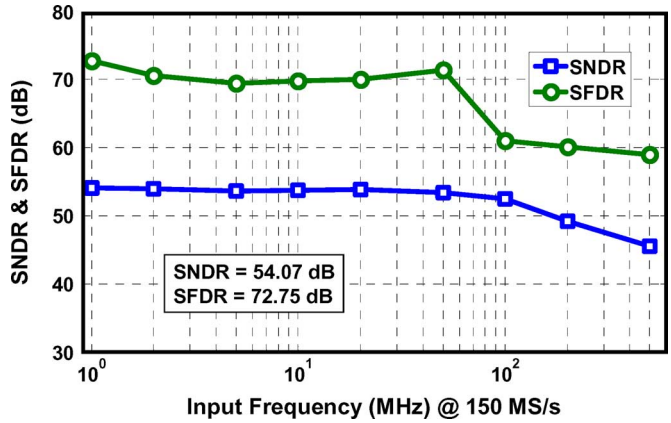


Fig. 18. Measured SNDR and SFDR vs. input frequency at 1.2-V supply.

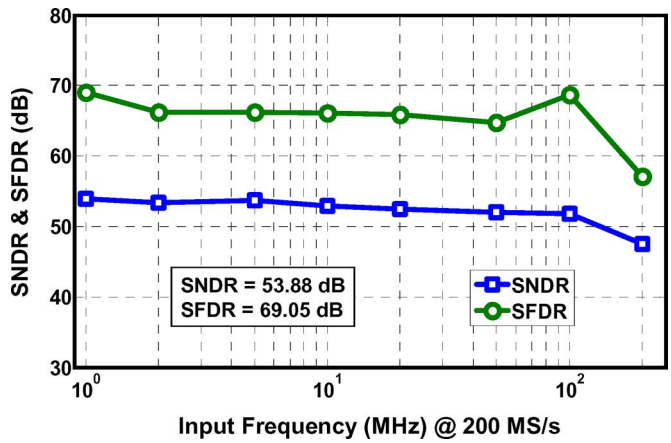


Fig. 19. Measured SNDR and SFDR vs. input frequency at 1.3-V supply.

Appendix

For matching concerns, a large capacitor in the DAC array consists of multiple identical unit capacitors. Owing to process variation, the practical capacitance of each unit capacitor deviates from the nominal value. For simplicity, assume that the error distributions of unit capacitors are independent and identically distributed (i.i.d.) Gaussian random variables. The capacitance of a capacitor can be expressed as [4]

$$C_n = 2^{n-1}C_0 + \delta_n \tag{6}$$

where n is an integer representing the bit position, C_0 is the unit capacitance and δ_n is the error term. The MSB is the bth bit for a b-bit ADC; the second MSB is the b-1th bit, and so on. For an ADC with the monotonic switching method, the capacitor of the nth bit consists of 2^{n-1} unit capacitors. Because the errors are i.i.d., the mean and variance of the error terms are

$$E[\delta_n] = 0, \quad E\left[\delta_n^2\right] = 2^{n-1}\sigma_0^2 \text{ and } E\left[\delta_0^2\right] = E\left[\delta_1^2\right] = \sigma_0^2 \tag{7}$$

TABLE I
COMPARISON TO STATE-OF-THE-ART WORKS AND SPECIFICATION SUMMARY

Specification (Unit)	ISSCC'07	ISSCC'08	ISSCC'08	VLSI'09	ISSCC'10	ISSCC'10	This Work		
Supply Voltage (V)	1	1	1.2	1.2	1	1.2	1	1.2	1.3
Sampling Rate (MS/s)	50	40	100	50	50	100	100	150	200
Power (mW)	0.7	0.82	4.5	0.92	0.82	1.13	0.75	1.53	2.20
$ENOB_1$ (bit) @ DC	7.8	8.56	9.5	8.48	9.16	9.51	8.72	8.69	8.66
$ENOB_2$ (bit) @ ERBW	7.4	8.23	9.3	8.01	9.11	9.01	8.44	8.42	8.31
ERBW (MHz)	10	32	200	100	100	50	50	100	100
FOM_1 (fJ/conv.-step)	65	54	62	52	29	15.5	17.7	24.7	27.2
FOM_2 (fJ/conv.-step)	86	68	69	72	30	21.9	21.5	29.8	34.7
Architecture	SAR	SAR	Pipelined	SAR	SAR	SAR	Flash + SAR		
Resolution (bit)	9	9	10	10	10	10	9		
Active Area (mm^2)	0.08	0.09	0.07	0.075	0.039	0.026	0.028		
Technology	90 nm	90 nm	65 nm	130 nm	65 nm	65 nm	90 nm		

As shown in Fig. 20, the differential input voltage of the comparator before it makes the last decision (i.e., all bits are decided except the LSB) can be expressed as

$$\begin{aligned}\Delta V_{\mathrm{x,binary}} &= V_{\mathrm{in}} + \frac{(-1)^{S_b}C_{b-1} + (-1)^{S_{b-1}}C_{b-2} \cdots + (-1)^{S_2}C_1}{C_{b-1} + C_{b-2} + \cdots + C_1 + C_0 + C_{\mathrm{p}}} V_{\mathrm{ref}} \\ &= V_{\mathrm{in}} + \frac{\sum_{n=2}^{b} (-1)^{S_n}(2^{n-2}C_0 + \delta_{n-1})}{2^{b-1}C_0 + \sum_{n=0}^{b-1}\delta_n + C_{\mathrm{p}}} V_{\mathrm{ref}} \end{aligned} \quad (8)$$

where S_n represents the comparator decision for the nth bit, V_{in} is the input signal difference, V_{ref} is the reference voltage and C_{p} is the parasitic capacitance. For simplification, the parasitic capacitance is ignored in the following derivations; V_{ref} and 0 replace V_{refp} and V_{refn}, respectively. If $\Delta V_{\mathrm{x,binary}}$ is 0, the input voltage is the transition level between two consecutive codes where all bits are equal except the LSB. Note that (8) is only valid for near half of the code transitions, i.e., 2^{b-1} for a b-bit ADC. The bold lines shown in Table II indicate when every code transition level is determined. From all 7 transition voltages, there are 4 where all bits are the same except the LSB ($0 \rightarrow 1, 2 \rightarrow 3, 4 \rightarrow 5$ and $6 \rightarrow 7$). The three code transition levels ($1 \rightarrow 2, 3 \rightarrow 4$ and $5 \rightarrow 6$) are determined without switching all capacitors. Assume y is the representation of the digital estimate, and the variance of the error term defined as differential comparator input minus the corresponding nominal value can be derived as

$$\begin{aligned} E\left[V^2_{\mathrm{err,binary}}(y)\right] &= E\left[(\Delta V_{\mathrm{x,binary}} - \Delta V_{\mathrm{x,nomial}})^2\right] \\ &= E\left[\frac{\sum_{n=2}^{b}\delta^2_{n-1}}{2^{2b-2}C_0^2}V^2_{\mathrm{ref}}\right] \cong \frac{2\sigma_0^2}{2^bC_0^2}V^2_{\mathrm{ref}} \end{aligned} \quad (9)$$

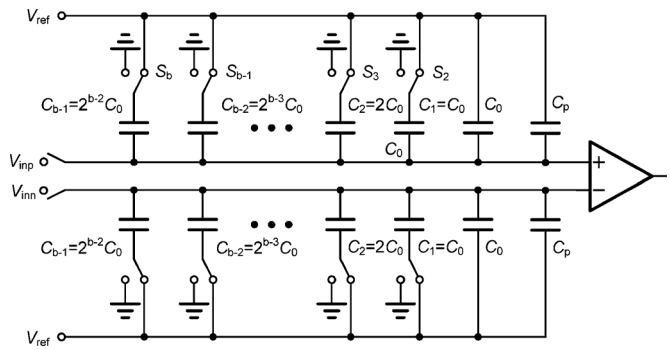


Fig. 20. A SAR ADC with a binary DAC.

Note the result in (9) is close to but not the accurate INL error since the error term and parasitic capacitance in the denominator of (8) are neglected in the derivation procedures. The peak INL value can be expressed as

$$\begin{aligned}\sigma_{\mathrm{maxINL,binary}}(\mathrm{LSB}) &\cong \frac{\sqrt{\frac{2\sigma_0^2}{2^bC_0^2}V^2_{\mathrm{ref}}}}{1\mathrm{LSB}} \\ &= \frac{\sqrt{\frac{2\sigma_0^2}{2^bC_0^2}V^2_{\mathrm{ref}}}}{\frac{1}{2^{b-1}}V_{\mathrm{ref}}} = \frac{\sigma_0\sqrt{2^{b-1}}}{C_0} \end{aligned} \quad (10)$$

The largest standard deviation of the INL happens for the code transition levels that are determined by switching all capacitors. For the other codes, their INL values are smaller because some capacitors do not switch. Take the 1/4 transition as an example, as shown in Table II, its value is determined after switching the MSB capacitors. Compared to the maximum case, only half the capacitance is switched, resulting in half the error variance according to (9). Thus, the INL value at the 1/4 transition is the maximum value divided by the square root of 2. For the most notable example, the half-scale transition is only determined by the first comparison without any capacitor switching. Therefore, it error variance is 0. Consequently, there are glitches in the plot of the standard deviation of the INL shown in Fig. 8.

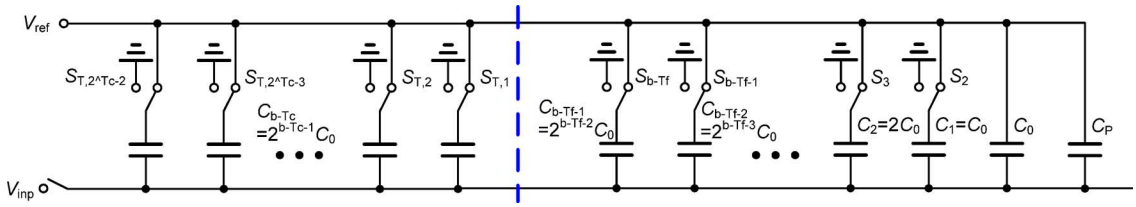


Fig. 21. Single-ended DAC of the flash-SAR ADC case.

TABLE II
INPUT LEVELS CAUSING CODE TRANSITIONS (BOLD) OF THE SAR ADC CASE

Code	*B3*	*B2*	*B1*
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The DNL is the difference of two adjacent codes expressed as

$$\mathrm{DNL}(y) = \frac{V_{\mathrm{err}}(y) - V_{\mathrm{err}}(y-1)}{1\mathrm{LSB}} \tag{11}$$

The maximum DNL of a binary DAC is the code distance between the middle code transition and its previous one. According to the aforementioned discussion, the middle transition is error free, so this error term is 0. The transition of the previous code switches all capacitor, so its error is the maximum value. The variance of the maximum DNL error is derived as

$$\begin{aligned} &E\left[(V_{\mathrm{err,binary}}(10\ldots00) - V_{\mathrm{err,binary}}(01\ldots11))^2\right] \\ &\quad = E\left[\left(0 - \frac{(-\delta_{b-1} + \delta_{b-2} + \cdots + \delta_1)}{2^{b-1}C_0}V_{\mathrm{ref}}\right)^2\right] \\ &\quad = \frac{E\left[\sum_{n=1}^{b-1}\delta_n^2\right]}{2^{2b-2}C_0^2}V_{\mathrm{ref}}^2 = \frac{(2^{b-1}-1)\sigma_0^2}{2^{2b-2}C_0^2}V_{\mathrm{ref}}^2 \cong \frac{2\sigma_0^2}{2^bC_0^2}V_{\mathrm{ref}}^2 \end{aligned} \tag{12}$$

Note that (9) and (12) yield the same final result. In other words, the maximum DNL value is the same as the maximum INL in (10).

Fig. 21 shows a flash-SAR ADC with a flash CADC resolving non-integer bits where T is the resolution of the CADC, $T_{\mathrm{f}} = \lfloor T \rfloor$ is the floor function result of T, and $T_{\mathrm{c}} = \lceil T \rceil$ is the ceiling function result of T. The proposed flash-SAR structure has the same INL as a binary SAR ADC shown in Fig. 20. For each digital code, the two ADCs eventually have the same unit capacitors switched, resulting in the same accumulated error. Unlike the monotonic case, the maximum DNL value happens during the reference levels of the comparators in the flash CADC. Take a flash-SAR ADC with a 1.5-bit CADC as an example. The maximum DNL values are at 3/8 and 5/8 full-scale range instead of 1/2. For a flash-SAR structure, original large capacitors

TABLE III
INPUT LEVELS CAUSING CODE TRANSITIONS (BOLD) OF THE FLASH-SAR ADC CASE

Code	*T2*	*T1*	B3	*B2*	*B1*
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	1	0	1	0
7	0	1	0	1	1
8	0	1	1	0	0
9	0	1	1	0	1
10	1	1	0	1	0
11	1	1	0	1	1
12	1	1	1	0	0
13	1	1	1	0	1
14	1	1	1	1	0
15	1	1	1	1	1

of the binary case are split into small identical ones. Equivalently, the mismatches of the large capacitors are redistributed, resulting in multiple small mismatch sources. Table III indicates the input signal levels (bold lines) causing code transitions of a 4-bit flash-SAR ADC with a 1.5-bit CADC where $T1$ and $T2$ represent the thermometer outputs of the CADC. In this example, $T1$, $T2$ and $B3$ control the same bit weight. The proposed flash-SAR ADC decides all thermometer codes after the first comparison. In other words, all thermometer capacitors are switched after the CADC comparison. Like in the binary case, the code transitions with the maximum error are those with all bits the same except the LSB. The minimum cases are the threshold voltages of the coarse comparators (3/8 and 5/8 transitions). A thermometer capacitor is switched in the transition between two adjacent thermometer codes. The minimum error is determined when one thermometer capacitor is not switched. The minimum error variance of a 1.5-bit CADC case is determined when 1/4 of the total capacitance is switched. To determine the 1/2 transition for a 1.5-bit CADC where $T2$ is 0 and $T1$ is 1, 1/2 of the total capacitance must be switched, the same quantity as the 1/4 transition of the binary case as shown in Fig. 8. The general form of the maximum DNL of the flash-SAR ADC in Fig. 21 can be expressed as

$$\begin{aligned} &\sigma_{\mathrm{maxDNL,hybrid}}(\mathrm{LSB}) \\ &\quad = \sqrt{1 - \left(\frac{(2^{T_{\mathrm{c}}} - 2) - 1}{2^{T_{\mathrm{c}}}}\right)} \times \sigma_{\mathrm{maxDNL,binary}} \end{aligned} \tag{13}$$

where the 2^{Tc} in the denominator means the total capacitance of the ADC, $2^{Tc}-2$ is the total capacitance of the thermometer capacitors. The equation derives the DNL of two adjacent codes where one has the maximum error and the other has the minimum error. Equation (13) is identical to (3)

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