A 6-bit Current-Steering DAC With Compound Current Cells for Both Communication and Rail-to-Rail Voltage-Source Applications

Ren-Li Chen, *Student Member, IEEE*, and Soon-Jyh Chang, *Member, IEEE*

***Abstract*—A compound current cell, with n-type, p-type, and bipolar properties, is proposed in this brief and utilized in a current-steering digital-to-analog converter (DAC) to satisfy the application of rail-to-rail voltage sources. In addition, the DAC with cells also has a high-speed fashion. Therefore, this brief presents a 6-bit CMOS current-steering DAC with cells for both communication and rail-to-rail voltage-source applications. Moreover, the effective output voltage step size is improved by appropriately switching these cells and connecting one of the gain control resisters, resulting in an about 6.4-mV step size in a 1.2-V supply. Furthermore, this DAC was implemented in a standard low-power 90-nm 1P9M CMOS technology with the active area of 0.045 mm^2. The measured spurious-free dynamic range is more than 36 dB over the Nyquist frequency at 3 GS/s and the DAC consumes 8.32 mW with a near-Nyquist sinusoidal output at the sampling rate of 3 GS/s.**

***Index Terms*—CMOS, current steering, digital-to-analog converter (DAC), rail-to-rail voltage sources.**

I. Introduction

IN MODERN wideband communication systems, low-resolution and high-speed data converters are increasingly required for signal processing [1]–[3]. For example, ultra-wideband technology needs a digital-to-analog converter (DAC) with accuracy above 4 bits (preferably 6 bits for the design margin) and operating speed beyond 1 GS/s. Therefore, the current-steering DAC is a good candidate to meet this application. It is intrinsically faster than resistor-string and switched-capacitor DACs and has the capability to drive a typical 50-Ω load without a voltage buffer, which will limit the overall performance of the DACs. Moreover, the evolution of IC fabrication technology has led to considerable growth in the integration of more components to include more functionality in a system-on-a-chip (SoC). However, some other circuits in the SoC may be out of order due to an inappropriate bias voltage originating from aging, process corner, and other variations. Designers can employ a resistor-string DAC as a voltage source to generate an appropriate bias voltage for the circuits to make them work in order. However, this will cause additional integration challenges and cost. If a DAC is idle in other channels, we can utilize it to generate an appropriate bias voltage without integrating other circuits. If the DAC provides rail-to-rail voltage sources, the appropriate voltage near any dc levels can be supplied. This could imply the reduction of the integration challenges and cost. Hence, in this brief, we want to propose a low-cost solution to make the DAC generate the appropriate bias voltage because other circuits failed due to the inappropriate bias voltage from various variations when the DAC in a SoC is idle in that moment. The remainder of this brief is organized as follows. Three conventional current cells and the proposed compound cell are introduced in Sections II and III, respectively. Section IV details the architecture, whereas the design considerations are presented in Section V. The measurement results and conclusion are given in Sections VI and VII, respectively.

Manuscript received February 19, 2012; revised April 29, 2012; accepted September 20, 2012. Date of publication October 26, 2012; date of current version January 4, 2013. This work was supported by the National Science Council of Taiwan under Grant NSC-98-2221-E-006-156-MY3. This brief was recommended by Associate Editor T.-C. Lee.

The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan (e-mail: chicboy@sscas.ee.ncku.edu.tw; soon@sscas.ee.ncku.edu.tw).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2012.2220696

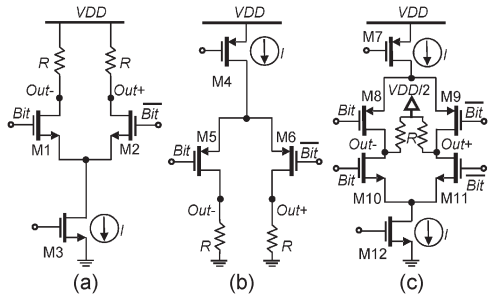

Fig. 1. Conventional current cells. (a) N-type. (b) P-type. (c) Bipolar.

II. Conventional Current Cells

A. N-Type Current Cell

Fig. 1(a) depicts an n-type current cell. The voltage of Out+ is either VDD or VDD $- IR$; therefore, this cell provides the output voltage range near VDD. In addition, the single-ended swing is IR and the peak to peak differential swing is $2IR$.

B. P-Type Current Cell

Fig. 1(b) shows a p-type current cell, and the voltage of Out+ is either GND or IR. The output swing conditions are equal to those of the n-type, but the output range is near GND.

C. Bipolar Current Cell

The bipolar current cell proposed in [4] is illustrated in Fig. 1(c). The output voltage of Out+ is either VDD$/2 + IR$ or VDD$/2 - IR$ and, consequently, the output range is near VDD$/2$. Additionally, the single-ended and peak-to-peak differential swings are $2IR$ and $4IR$, respectively. The power

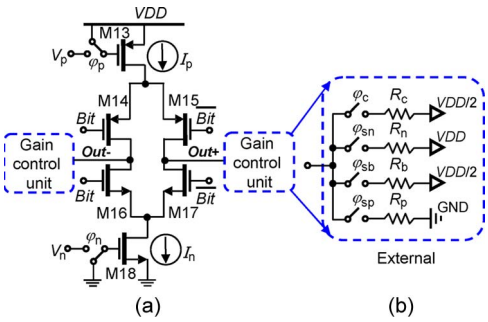

Fig. 2. (a) Compound current cell. (b) Gain control unit.

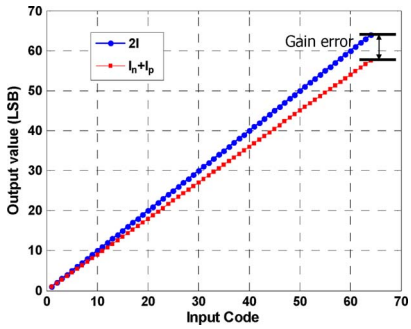

Fig. 3. Input–output transfer curves of the two DACs.

consumption of the three cells is VDD $\times I$, and the bipolar cell with the same output swing as the n- or p-type cell only consumes half the power.

III. Compound Current Cell

In order to meet the two applications, we propose a compound current cell, as shown in Fig. 2. The n- and p-type current sources, i.e., I_n and I_p, respectively, are turned on or off by connecting switches φ_n and φ_p to V_n and V_p or GND and VDD. In addition, the gain control unit consists of four resistors. R_c is designed for the communication application and the value is determined by communication systems for impedance matching to transfer the maximum power, and it is almost equal to 50 Ω. Other resistors, namely, R_n, R_b, and R_p, are utilized for the rail-to-rail voltage-source application and the main idea to realize rail-to-rail voltage sources is turning on the n-type, p-type, or both current sources in the compound current cells to supply a voltage range near VDD, GND, or VDD$/2$ and adjusting the output resistor values to make the three voltage ranges cover the rail-to-rail voltage. If any two resistor values of the four resistors are the same, we can only use either of the resistors to reduce the cost and parasitic capacitances at output nodes Out$+$ and Out$-$. The operating principles of communication and rail-to-rail voltage-source applications are introduced in the following sections.

A. Communication Application

On communication applications, both current sources I_n and I_p are turned on by connecting switches φ_n and φ_p to V_n and V_p, and R_c is connected by switch φ_c. In addition, this connection type is similar to the bipolar current cell, but both current sources in the bipolar one have the same I. Consequently, one may be afraid that the offset of I_n and I_p will result in nonlinearity. Nonetheless, this offset does not cause nonlinearity. For a DAC with cells, we assume $I = I_n > I_p$ and $R_c = R$. If there is no mismatch between the n-type current sources or between the p-type ones, the value of least significant bit (LSB) will be $(I_n + I_p) \times R_c$ and different from that of a DAC with the bipolar ones, which is $2IR$. Fig. 3 shows the two DACs' input–output transfer curves: the output value is linearly increased with input codes and only a gain error is caused. The subsequent variable gain amplifier can compensate for this error. Moreover, we can switch on one of the two current sources and connect R_c to VDD or GND for providing a voltage range near VDD or GND to conform with the input common mode of subsequent circuits. However, only the voltage swing of I_nR_c or I_pR_c is supplied. In addition, more switches are needed, and the extra parasitic capacitance from the switches will result in bad dynamic performance. With the aim of power efficiency and good dynamic performance at high frequencies, we turn on both I_n and I_p and only connect R_c to VDD$/2$ on this application.

B. Rail-to-Rail Voltage-Source Application

The output voltage is defined by Ohm's law as

$$V = IR. \tag{1}$$

The output voltage is changed by adjusting the value of the output current or load. In a current-steering DAC, enlarging the output current increases the die size and power dissipation due to widening of the width of the output lines and connection lines of each current source to obey electromigration reliability rules. Therefore, the output swing is changed by adjusting the output load value to maintain the same power and cost. Moreover, it is important not to exceed the maximum voltage range on the output current pins to ensure that the current cells are operating within the specified operating conditions.

We give an example of an N-bit DAC with cells to describe how to fulfill this application. The individual and total currents of the n-type current sources are assumed as I_n and I_N, respectively, with the relation of $I_N = (2^N - 1)I_n$. I_p and I_P also have the same relation and meaning of the p-type ones. The properties of the three voltage ranges are presented next, and these three are defined as Ranges A, B, and C for easy identification.

1) *Range A:* In this range, only n-type current sources are turned on by closing switches φ_n and φ_p to V_n and VDD, and the output load is R_n by closing switch φ_{sn}. Moreover, the DAC provides the output voltage from VDD to VDD $- I_NR_n$, the output voltage swing is I_NR_n, and the step size is I_nR_n.
2) *Range B:* The output voltage of the DAC from VDD$/2 + I_PR_b$ to VDD$/2 - I_NR_b$ is supplied, both current sources are switched on by connecting switches φ_n and φ_p to V_n and V_p, and switch φ_{sb} is connected to R_b. Additionally, the voltage swing and step size are $R_b(I_N + I_P)$ and $R_b(I_n + I_p)$, respectively.
3) *Range C:* Only p-type current sources are turned on by connecting switches φ_n and φ_p to GND and V_p. Switch φ_{sp} is closed to R_p, the output voltage is from GND to I_PR_p, and the output swing and step size are I_PR_p and I_pR_p, respectively.

To ensure that the three voltage ranges cover the rail-to-rail voltage, some design criteria, which are defined in the following

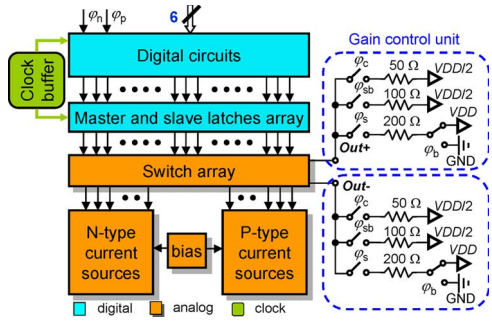

Fig. 4. Block diagram of the proposed 6-bit DAC.

equations, must be satisfied. The criteria are that the sum of the three ranges is larger than or equal to VDD, as presented in (2), and that the minimum value of Rang A $(\text{VDD} - I_N R_n)$ and the maximum value of Rang C $(I_P R_p)$ are both within Range B to make Ranges A and C overlap Range B, as expressed in (3) and (4). That is

$$I_N R_n + (I_N + I_P) R_b + I_P R_p \geq \text{VDD} \tag{2}$$

$$\text{VDD}/2 + I_P R_p \geq \text{VDD} - I_N R_n \geq \text{VDD}/2 - I_N R_n \tag{3}$$

$$\text{VDD}/2 + I_P R_p \geq I_P R_p \geq \text{VDD}/2 - I_N R_p. \tag{4}$$

IV. Architecture

Fig. 4 shows the block diagram of the proposed 6-bit DAC. Two control signals, namely, φ_n and φ_p, are designed to turn on or off the n- and p-type current sources for the communication and rail-to-rail voltage-source applications. In addition, one can turn off both current sources to save power consumption when the DAC is not in use. The operating principles of the two applications are presented next.

A. Communication Application

A 50-Ω resistor is connected for impedance matching and both current sources are turned on for better power efficiency. In addition, both current sources I_n and I_p can be designed as different values with no decrease in linearity, as introduced in Section III. However, if there is no mismatch between I_n and I_p, the power dissipation of the supply $\text{VDD}/2$ will be zero. In practice, there might be some mismatches between I_n and I_p [4]. Consequently, we design $I_n = I_p$ to ensure that the power dissipation of the supply is negligible. In this design, the total output currents of both current sources, i.e., I_N and I_P, are chosen to be 2 mA to reach a compromise between the system requirement and the DAC's performance, and thus, both LSB currents are 31.7 μA. The single-ended and peak-to-peak differential swings are 200 and 400 mV, respectively.

B. Rail-to-Rail Voltage-Source Application

In this design, the supply voltage is 1.2 V. If we want to design each range with equal value, each range would be 400 mV. Therefore, the appropriate resistor value should be chosen to make the three ranges cover the rail-to-rail voltage and satisfy the design criteria presented in (2)–(4). Moreover, we present the properties of the three voltage ranges.

1) *Range A:* Only the n-type current sources with a 2-mA total current are turned on, and the load value is designed as 200 Ω to obtain a 400-mV output range. In addition, switch φ_s is closed and switch φ_b is connected to VDD. Consequently, the output range is from 1.2 to 0.8 V.
2) *Range B:* Both current sources with total currents of 2 mA are turned on. If we want to design the output swing as 400 mV, the load value would be half the load value in Range A. Accordingly, the load value is designed as 100 Ω, not 200 Ω. Moreover, switch φ_{sb} is closed to $\text{VDD}/2$ and the DAC provides the voltage range from 0.8 to 0.4 V in this range.
3) *Range C:* Only the p-type current sources with the total value of 2 mA are turned on. The load value is designed as 200 Ω for a 400-mV output swing. The load value is the same as that in Range A; therefore, we only utilize one resistor and share it when the DAC is operated in Range A or C to reduce the extra resistors and parasitic capacitances at the output nodes of Out+ and Out−, which is introduced in Section III. Additionally, switch φ_s is closed and switch φ_b is connected to GND. Moreover, the output range is supplied from 0.4 V to GND.

V. Design Considerations

The digital circuits shown in Fig. 4 are the same as those in [5]. The proposed DAC employs a 3-bit pseudothermometer decoder proposed in [5] to improve the dynamic performance and relax the matching requirements of the current cells more than that of a binary DAC for a given differential nonlinearity (DNL) specification.

The current cell transistors should be properly designed to fulfill static matching and to provide sufficient output impedance over the Nyquist frequency for alleviating nonlinearity distortion induced by frequency-dependent output impedance according to [1], [5]:

$$(WL)_{\min} = \frac{1}{2}\left[A_\beta^2 + \frac{4 \cdot A_{VT}^2}{(V_{GS} - V_T)^2}\right] \Bigg/ \left(\frac{\sigma(I)}{I}\right)^2 \tag{5}$$

$$\text{IMD3} = \frac{14 g_{\text{imp}}^2 N^2 + 16 g_l^2 + 16 g_l g_{\text{imp}} N}{3 g_{\text{imp}}^2 N^2} \tag{6}$$

with A_β and A_{VT} as the process parameters; $\sigma(I)/I$ as the relative LSB current source standard deviation; g_l and g_{imp} as the reciprocals of the load resistance and the required frequency-dependent impedance, respectively; and N as the number of current source cells. As a consequence, the W/L ratios of unit nMOS and pMOS current cell transistors are designed as 3.5 μm/1.2 μm and 5.2 μm/0.4 μm. In addition, the difference between the output impedance of the n- and p-type current sources will result in different integral nonlinearity (INL) and DNL when n- or p-type current cells are operated in Range A, B, or C. Therefore, we design the two output impedances to be the same as much as possible.

The switch transistors are designed with the minimum length; the W/L ratios of unit nMOS and pMOS switch transistors are designed as 0.3 μm/0.1 μm and 0.9 μm/0.1 μm, respectively; and rail-to-rail switch control signals are employed for easy realizing from the supply voltage. In addition, we cascade the compact latch proposed in [5] to form the master and slave latches shown in Fig. 5 to increase the processing time for the digital circuits from half a clock period to a complete clock period. Consequently, employing the latches reduces the timing error and secures enough timing margin for the digital circuits.

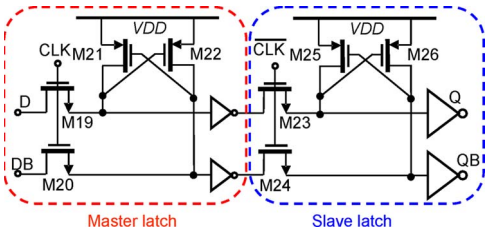

Fig. 5. Master and slave latches.

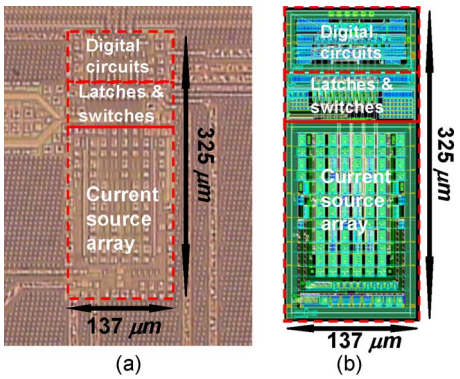

Fig. 6. (a) Chip microphotograph. (b) Layout view.

Under layout considerations, the LSB current is implemented only with a unit transistor. The binary-weighted current source cell is realized with the same binary-weighted number of unit transistors connected in parallel with a finger structure to reduce the source/drain junction capacitance and silicon area. A simple centroid switching scheme as in [5] is employed to compensate for systematic errors with less parasitic capacitances. Moreover, the dummy cells are placed around the active current cells to make all the current cells have the same surroundings as each other. The treelike connections for both the clock net and the output nets are employed to reduce timing errors [1].

The digital circuits are realized with power-efficient CMOS logic. Moreover, in order to reduce power bouncing and interference, we design the analog and digital parts of the DAC powered separately with individual metal-to-metal and MOS decoupling capacitors extensively used for power supply filtering.

Only higher speed signals pass through switch φ_c, and thus, the printed circuit board trace through it should be designed as shortly as possible to reduce parasitic capacitances.

VI. Measurement Results

A. Communication Application

Fig. 6 shows the chip microphotograph and corresponding layout view with the active area of 137 μm $\times$ 325 μm. The measurement of this application is performed on a differential output. The measured DNL and INL are less than 0.05 and 0.07 LSB, respectively.

The dynamic performance of this DAC has been measured at the conversion rates of 1, 2, and 3 GS/s. Fig. 7 summarizes the measured spurious-free dynamic range (SFDR) results as a function of the normalized input frequency at the different sampling rates. On the horizontal axis, the normalized frequency is defined as the single tone's fundamental frequency f_s divided by the sampling frequency f_c. The measured SFDR results are

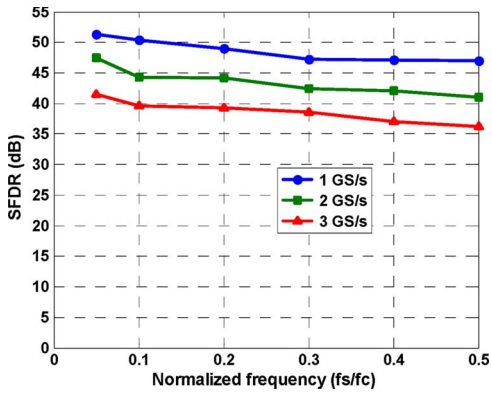

Fig. 7. Measured SFDR results at 1, 2, and 3 GS/s.

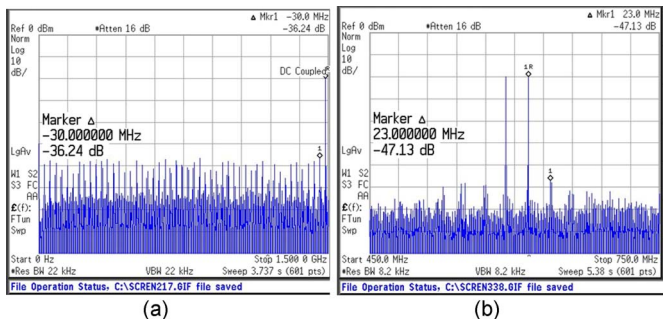

Fig. 8. (a) Output spectrum with a near-Nyquist signal at 3 GS/s. (b) Two-tone test spectrum.

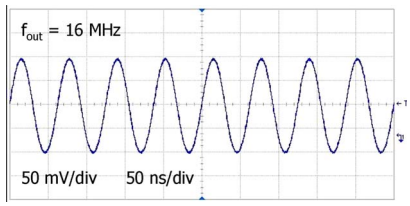

Fig. 9. Measured sinusoidal output waveforms.

more than 40 and 36 dB over the Nyquist frequency at 2 and 3 GS/s, respectively. The SFDR of the DAC at 3 GS/s decreases because of nonlinear switching transients in a shorter clock cycle, and the DAC sampling rate is limited by the settling time of nonlinear switching transients. Fig. 8(a) shows that the measured SFDR with a near-Nyquist output signal at 3 GS/s is 36.24 dB, the power consumption with a near-Nyquist output signal at 3 GS/s is 8.32 mW, and the digital and analog power levels are 4.3 and 4.02 mW, respectively. Fig. 8(b) shows a two-tone test spectrum with frequencies of 591 and 614 MHz at 3 GS/s and a third-order intermodulation distortion of less than -47 dB. Fig. 9 depicts the measured single-ended sinusoidal output waveforms for the output frequency of 16 MHz.

In order to compare this work with other previous ones, we list the published arts [1], [5]–[7] with similar specifications in Table I. In addition, the measurement results of this DAC are also included in the table for comparison purposes. The figure-of-merit (FOM) in [8] is used to assess the performance of the DACs as

$$\text{FOM} = \frac{2^{\text{ENOB}_{\text{LF}}} \times 2^{\text{ENOB}^2_{fcl}} \times f_s}{P_{\text{Total}} - P_{\text{Load}}} \tag{7}$$

TABLE I
COMPARISON WITH OTHER PUBLISHED ARTS

Reference	[1]	[5]	[6]	[7]	This work
Resolution (bit)	6	6	6	6	6
Technology (nm)	130	130	130	65	90
Update rate (GS/s)	3	2.7	1.25	2.4	3
DNL (LSB)	NA	0.09	0.06	0.02	0.05
INL (LSB)	0.02	0.11	0.05	0.02	0.07
$SFDR_{LF}$ (dB)	47	39.62	47.7	48	41.54
$SFDR_{fs/2}$ (dB)	36	36.07	23	36	36.24
Active area (mm^2)	0.2	0.059	0.08	0.023	0.045
Power (mW)	29	5.4	8	14	8.32
FOM ($10^3 \times$ GHz/mW)	1	2.07	0.39	1.99	1.91

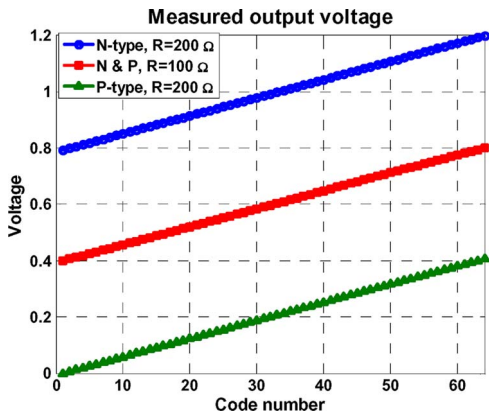

Fig. 10. Measured output voltages.

TABLE II
OUTPUT VOLTAGE SPECIFICATION TABLE

Range	A	B	C
Current type	N-type On	N & P On	P-type On
V_{min} (mV)	793.7	400	0
V_{MAX} (mV)	1200	800	407.2
Swing (mV)	406.3	400	407.2
Output load (Ω)	200	100	200
Step size (mV)	6.45	6.35	6.46
DNL (LSB)	0.064	0.074	0.033
INL (LSB)	0.193	0.264	0.112
Monotonicity	√	√	√

where $\text{ENOB}_{\text{LF}} = (\text{SFDR}_{\text{LF}} - 1.76)/6.02$ and $\text{ENOB}_{fc/2} = (\text{SFDR}_{fc/2} - 1.76)/6.02$. The FOM and active area of this DAC are comparable with those of other published arts.

B. Rail-to-Rail Voltage-Source Application

The measurement of this application is performed on a single-ended output. We choose the correct resistance value by measuring it in advance to ensure that the resistor values do not influence the output voltage swings in Ranges A, B, and C and the rail-to-rail voltage-source application. Fig. 10 shows the measured output voltage versus input code numbers with different ranges. In addition, Table II indicates the output voltage specifications of the three ranges. Moreover, monotonicity is guaranteed in each range.

In this design, our design target is to make sure the three voltage ranges cover the rail-to-rail voltage without any larger voltage gaps. Therefore, if we ensure the swing of Range B is equal to 400 mV, the swings of Ranges A and C will be larger than 400 mV due to the finite output impedance effect, and the target will be achieved without any trimming. One can make the three ranges all have a 400-mV swing by altering the output load value. However, two resistors are necessary for Ranges A and C because the finite output impedance effects in the n- and p-type current sources are different. Consequently, the additional resistors are needed to increase the cost and parasitic capacitance at the output nodes Out+ and Out− and thus cause bad dynamic performance at high frequencies. Therefore, one resistor is utilized and shared between Ranges A and C. Additionally, if a 6-bit resistor-string DAC is employed to realize this application, the step size will be 19 mV from the expression of 1200 mV$/(2^6 - 1)$. Consequently, the step size in this design is improved by this design methodology, and it is about 6.4 mV in a 1.2-V supply. If designers want the resistor-string DAC to provide the same step size, the resolution of the DAC should be increased and, thus, the number of components and the size of components should be also increased to keep relative accuracy. This will increase the considerable cost.

VII. CONCLUSION

This brief has demonstrated a 6-bit current-steering DAC with compound current cells to fulfill communication and rail-to-rail voltage-source applications. Moreover, this DAC was implemented in a 90-nm CMOS technology with the measured SFDR more than 36 dB over the Nyquist frequency at 3 GS/s and the power consumption of 8.32 mW with a near-Nyquist sinusoidal output. Furthermore, the output voltage step size is improved by appropriately switching the cells and connecting one of the gain control resisters, resulting in the step size of about 6.4 mV in a 1.2-V supply. Finally, this DAC can be integrated into a SoC for the two applications well at different timing to reduce the integration challenges.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center, Taiwan, for fabrication and measurement support.

REFERENCES

[1] X. Wu, P. Palmeras, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit full Nyquist 3 GS/s DAC," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2396–2403, Nov. 2008.

[2] Y. M. Greshishchev, D. Pollex, S.-C. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, and P. Schvan, "A 56 GS/s 6b DAC in 65 nm CMOS with 256 × 6b memory," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 194–196.

[3] M. Nagatani, H. Nosaka, K. Sano, K. Murata, K. Kurishima, and M. Ida, "A 60-GS/s 6-bit DAC in 0.5- μm InP HBT technology for optical communications systems," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, Oct. 2011, pp. 1–4.

[4] K. Farzan and D. A. Johns, "A CMOS 10-Gb/s power-efficient 4-PAM transmitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 529–532, Mar. 2004.

[5] R. L. Chen, H. W. Ting, and S. J. Chang, "Six-bit 2.7-GS/s 5.4-mW Nyquist complementary metal–oxide semiconductor digital-to-analogue converter for ultra-wideband transceivers," *IET Circuits Devices Syst.*, vol. 6, no. 2, pp. 95–102, Mar. 2012.

[6] S. M. Lin, D. U. Li, and W. T. Chen, "1 V 1.25 GS/s 8 mW D/A converters for MB-OFDM UWB transceivers," in *Proc. IEEE Int. Conf. Ultra-Wideband*, Sep. 2007, pp. 453–456.

[7] B. C. Kim, M. H. Cho, Y. G. Kim, and J. K. Kwon, "A 1 V 6-bit 2.4 GS/s Nyquist CMOS DAC for UWB systems," in *Proc. IEEE Int. Microw. Symp.*, May 2010, pp. 912–915.

[8] M. Clara, W. Klatzer, B. Seger, A. Di Giandomenico, and L. Gori, "A 1.5 V 200 MS/s 13b 25 mW DAC with randomized nested background calibration in 0.13 μm CMOS," in *Proc. ISSCC Dig. Papers*, Feb. 2007, pp. 250–600.