A 1-μW 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications

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***Abstract*—This paper presents an energy efficient successive-approximation-register (SAR) analog-to-digital converter (ADC) for biomedical applications. To reduce energy consumption, a bypass window technique is used to select switching sequences to skip several conversion steps when the signal is within a predefined small window. The power consumptions of the capacitive digital-to-analog converter (DAC), latch comparator, and digital control circuit of the proposed ADC are lower than those of a conventional SAR ADC. The proposed bypass window tolerates the DAC settling error and comparator voltage offset in the first four phases and suppresses the peak DNL and INL values. A proof-of-concept prototype was fabricated in 0.18-μm 1P6M CMOS technology. At a 0.6-V supply voltage and a 200-kS/s sampling rate, the ADC achieves a signal-to-noise and distortion ratio of 57.97 dB and consumes 1.04 μW, resulting in a figure of merit of 8.03 fJ/conversion-step. The ADC core occupies an active area of only 0.082 mm^2.**

***Index Terms*—Bypass window SAR ADC, incomplete settling tolerance, low power ADC, SAR ADC, successive approximation analog-to-digital converter.**

I. Introduction

In the last few years, there has been a growing interest in the design of wireless sensing device for portable, wearable or implantable biomedical applications. These sensing devices are generally used for detecting and monitoring biomedical signals such as electrocardiographic (ECG), electroencephalography (EEG), and electromyography (EMG), to name a few. Most biomedical signals are often very slow and exhibit limited dynamic range [1]. A typical biomedical sensor interface consists of a band-pass filter, a low-noise amplifier and an analog-to-digital converter (ADC). The digitalization of the sensed biomedical signals is usually performed by ADCs with moderate resolution (8–12 bits) and sampling rate (1–1000 kS/s) [2], [3]. In such devices, energy efficiency and long battery life are paramount design goals. Particularly, ADCs for implanted medical devices need microwatt operation to run on a small battery for decades [4]. Therefore, energy efficiency is a critical challenge for ADCs design.

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Successive approximation register (SAR) ADC has the advantage of power efficiency compared with other ADC architectures (e.g., pipelined ADC). Furthermore, SAR ADC benefits from technology downscaling because of two major reasons: (1) SAR ADC mainly consists of digital circuits which get faster in deep sub-micron technologies; and (2) SAR ADC is an opamp-free architecture. In other words, SAR ADC does not require high gain and high bandwidth opamps to guarantee the linearity. A high-performance opamp consumes large power, and suffers from short channel effect and low supply voltage in advanced process nodes [5]. These reasons arouse the interest of designers which is reflected in the number of recent publications [6]–[22].

SAR ADCs are commonly used in biomedical acquisition systems due to their low power consumption and simplicity, particularly for simple analog sub-circuits [10]–[15]. The comparator and sampling switches are the only two analog components. No static power is consumed if preamplifiers are not used. Several power-efficient switching sequences for capacitive digital-to-analog converters (DACs) have been proposed [8]–[11] to reduce the dynamic power consumption. Compared to the conventional switching sequence, the energy-saving [8], monotonic [9], $V_{\rm cm}$-based [10], and, partial floating [11] switching sequences reduce switching energy by 69%, 81%, 90%, and 94%, respectively. However, the DAC switching accounts for only about 30% of the power consumption of a modern SAR ADC. The digital control logic and comparator account for the rest. Although the $V_{\rm cm}$-based and partial floating switching sequences reduce the switching energy by over 90%, they require complex digital control logic.

Many biomedical signals exhibit small variations in magnitude for a large portion of time, as shown in Fig. 1. To reduce the power consumption of the SAR ADC for biomedical signal acquisition, this work proposes a bypass window technique to refer to input signal range to determine the switching sequences of the capacitive DAC. The basic idea of the proposed technique is to skip the conversion steps for several significant bits when the signal is within a predefined small window. The power consumptions of the capacitive DAC, latch comparator, and digital control logics of the proposed ADC are lower than those of a conventional SAR ADC. Moreover, the skip operation reduces the error accumulation to improve the static performance.

In addition to power consumption, incomplete DAC settling is a critical issue as it affects the linearity of a SAR ADC. Several methods have been proposed to overcome this problem [16], [17]. However, extra comparison cycles, and thus extra power, are required to compensate for the settling error. The

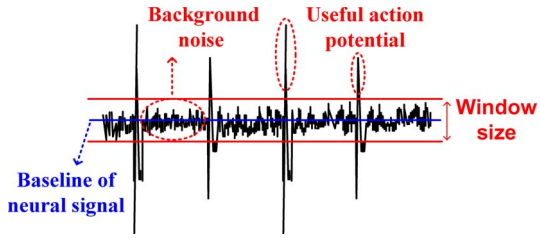


Fig. 1. Neural signal.

proposed bypass window technique does not need extra power or comparison cycles.

The remainder of this paper is organized as follows: Section II describes the architecture and basic design concept of the proposed bypass window SAR ADC. Section III shows the advantages of the bypass window SAR ADC. Section IV presents the details of the implementation for all key building blocks. Section V shows the measurement results to demonstrate the effectiveness of this proposed technique. Finally, conclusions are drawn in Section VI.

II. Architecture and Design Concept of the Proposed SAR ADC

A. Bypass Window Concept

For an N-bit SAR ADC, N times comparisons and capacitor switches are required during the conversion procedure. The capacitor array is switched from the most significant bit (MSB) to the least significant bits (LSB) according to the comparator outputs. During conversion process, $V_{\rm DACP}$ and $V_{\rm DACN}$ are added or subtracted a binary-weighted voltage, $V_{ref,i}$, i.e., $V_{ref,1} = 1/2V_{ref}$ and $V_{ref,2} = 1/4V_{ref}$, according to the comparator output. Fig. 2(a) shows an example of the conventional conversion process where $V_{\rm DACP}$ and $V_{\rm DACN}$ are the voltages at the comparator input terminals. The voltage difference between $V_{\rm DACP}$ and $V_{\rm DACN}$ in phase 2, $V_{\rm diff,2}$, is very small. However, the two signals diverge in phase 3, which is power inefficient. In [19], a variable voltage window, $V_{{\rm win},i}$, is used to detect whether $V_{{\rm diff},i}$ is smaller than $V_{ref,i}$, where the adopted window voltage, $V_{{\rm win},i}$, is the same as $V_{ref,i}$ and active in the first four phases. Where $V_{{\rm diff},i}$ and $V_{{\rm win},i}$ are $V_{\rm DACP} - V_{\rm DACN}$ and the window voltage at ith phase, respectively. If $V_{{\rm diff},i} < V_{{\rm win},i}$, the DAC switching is neglected.

Suppose the constant voltage window (bypass window), $V_{\rm win}$, is adopted and which is the same as $V_{ref,2}$ (128 LSBs). If $V_{\rm diff,1} < V_{\rm win}$ (128 LSBs) in phase 1, it means no DAC switching is needed in phase 1 and 2. Therefore, SAR ADCs can avoid two DAC switchings and comparison in phase 2. For the bypassed phase, the power consumptions of DAC switching, comparator and digital control logic (including the DAC switching buffers) are saved. The smaller window size is chosen, the more redundant phase can be bypassed. However, the less probability of input signal is within the bypass window.

Fig. 2(b) shows an example of the bypass window, which uses a 32-LSB window size, $V_{\rm win}$. The bypass window adopts in the first four phases. If $V_{{\rm diff},i} < V_{\rm win}$, the digital controller logic triggers the bypass window and skips to phase 5, as shown in Fig. 2(b). There is no DAC switching and comparison in phases 3 and 4.

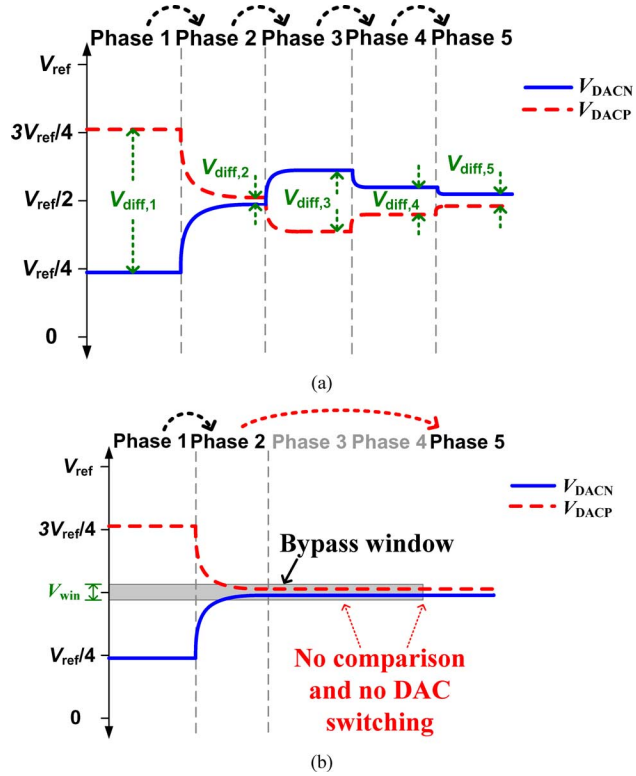


Fig. 2. Conversion processes of (a) conventional and (b) proposed bypass window SAR ADC.

B. Power Reduction of Different Window Size

The power consumption of SAR ADCs consists of three parts: comparator, digital control logic and DAC switching. For a 10-bit SAR ADC, a complete data conversion requires 10 comparisons. The total power consumption of the comparator is $10P_{\rm CMP,avg}$, where $P_{\rm CMP,avg}$ is the average power consumption of one comparison. The proposed bypass window architecture needs two coarse comparators for the window prediction, however, the size of the coarse comparator is half of the fine one. The detail design concepts of the architecture are introduced in Section III-A. Here, we assume the power consumption of each comparison is the same.

The power consumption of the digital control logic contains two parts: successive approximation control logic (SA) and DAC switch buffers. The SA is regular control logic and the power consumption is proportional to the required phases. The bypass window needs extra control logic to detect whether the bypass window is triggered. However, the additional control logic is relatively simple. The details of the extra control logic are discussed in Section III-C. The size of each switch and switch buffer are binary-weighted as the capacitor array. The power consumption of switch buffers is proportional to the switch sizes. For a conventional 10-bit SAR ADC, the average power consumption of the total control logic and switch buffers are $10P_{\rm SA,avg}$ and $511P_{\rm Switch,avg}$, respectively, where $P_{\rm SA,avg}$ and $P_{\rm Switch,avg}$ are the average power consumption of the control logic and unit size switch buffer in each phase.

The power consumption of the DAC switching is determined by the switching sequence and the capacitance of the capacitor array. Assume the capacitance of the capacitor array is binary-weighted. For a conventional 10-bit SAR ADC, the average power consumption of the DAC switching is $\sum_{i=1}^{9} P_{DAC,i}$, where $P_{DAC,i}$ is the average power consumption of the DAC switching in phase i.

Suppose each digital output code is equiprobable. For a 10-bit SAR ADC using different size bypass window, the average power consumption of the comparator, SA, switch buffers, and DAC switching can be derived as

$$P_{\mathrm{CMP.total}} = \left(10 - \sum_{i=0}^{8-M} i \cdot 2^{-(i+1)}\right) P_{\mathrm{CMP.avg}} \quad (1)$$

$$P_{\mathrm{SA.total}} = \left(10 - \sum_{i=0}^{8-M} i \cdot 2^{-(i+1)}\right) P_{\mathrm{SA.avg}} \quad (2)$$

$$P_{\mathrm{Switch.total}} = \left(511 - \sum_{i=0}^{8-M} 2^{M} \cdot (1 - 2^{-(i+1)})\right) P_{\mathrm{Switch.avg}} \quad (3)$$

$$P_{DAC.\mathrm{total}} = \sum_{i=1}^{9} P_{DAC,i} - \sum_{i=0}^{8-M} (2^{i+1} - 1) \cdot 2^{-(i+1)} P_{DAC,i+1} \quad (4)$$

where $P_{\mathrm{CMP,total}}$, $P_{\mathrm{SA,total}}$, $P_{\mathrm{Switch,total}}$, and $P_{DAC,\mathrm{total}}$ are the average power consumption of comparator, SA, switch buffers, and DAC switching for a complete conversion process, respectively, and M is the window size factor (i.e., the window size is 2^M LSBs).

Form the simulation results, $P_{\mathrm{CMP,total}}$, $P_{\mathrm{SA,total}}$, $P_{\mathrm{Switch,total}}$, and $P_{DAC,\mathrm{total}}$ occupy about 15.4%, 44.3%, 11.1%, and 29.2% of the total power consumption, respectively. Fig. 3 shows the total power consumption of the different window size in SAR ADCs. For uniformly distributed input signals, the 128-LSB window size reduces the most power consumption. However, for different input signal, such as normal distributed signal, ECG signal, or neural signal, most of their signal levels are in the proximity of the V_{cm}, as shown in Fig. 1. In this case, we can use a narrower bypass window for power reduction. For example, if a proper instrument amplifier (IA) is adopted to amplify the input signal and most of the input signal are within -24 dBFS, a 32-LSB bypass window is more suitable than 128-LSB for the power reduction. Therefore, in this work, a 32-LSB bypass window is adopted for biomedical applications.

C. ADC Architecture

Fig. 4 shows the architecture of the proposed SAR ADC. It consists of two coarse comparators, a fine comparator, two capacitor arrays and SAR control logic. Compared to the conventional SAR ADCs, the bypass window SAR ADC needs two comparators and a window reference voltage, V_{r}, to complete the bypass window function, where V_{r} is a constant voltage and it decides the bypass window size. In the sampling phase, the capacitor array samples the input signal via the bootstrapped switches [23], while the bottom plates of capacitors $C_{9\mathrm{b}} \sim C_{6\mathrm{b}}$

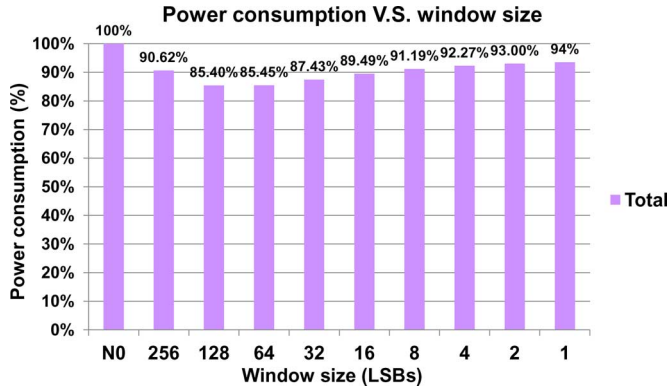


Fig. 3. Power consumption of different window size with uniformly distributed output code.

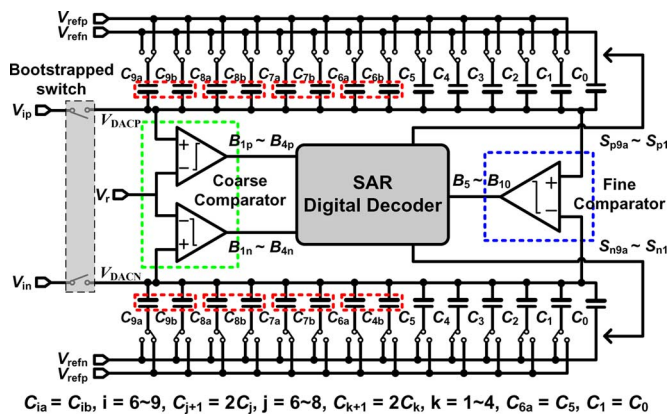


Fig. 4. Architecture of proposed SAR ADC.

and $C_5 \sim C_1$ switch to V_{refn} and the bottom plates of capacitors $C_{9\mathrm{a}} \sim C_{6\mathrm{a}}$ switch to V_{refp}. In the conversion phase, the proposed SAR ADC adopts a 32-LSB bypass window, which determines whether $V_{\mathrm{diff},i}$ is less than V_{win} in the first four comparisons.

In phase 1, the coarse comparators compare the top plate voltages of the capacitor array, V_{DACP} and V_{DACN}, with the window reference voltage V_{r} to generate $B_{1\mathrm{p}}$ and B_{1n}, respectively. If both $B_{1\mathrm{p}}$ and B_{1n} are "1" ($V_{\mathrm{diff},i} < V_{\mathrm{win}}$), the digital control logic triggers the bypass window and shifts to phase 5 in the next comparison. If $B_{1\mathrm{p}}$ and B_{1n} are "10" or "01" ($V_{\mathrm{diff},i} > V_{\mathrm{win}}$), the bypass window is not triggered. Suppose that $B_{1\mathrm{p}}$ and B_{1n} are "10"; then, the bottom plate voltage of $C_{9\mathrm{a}}$ of the P side DAC switches from V_{refp} to V_{refn}. Simultaneously, the voltage of $C_{9\mathrm{b}}$ of the N side switches from V_{refn} to V_{refp}. The voltage difference of the DAC output terminals ($V_{\mathrm{diff},i}$) change from V_{input} to $V_{\mathrm{input}} - 1/2V_{ref}$, where V_{input} is $V_{\mathrm{ip}} - V_{\mathrm{in}}$ and V_{ref} is $V_{\mathrm{refp}} - V_{\mathrm{refn}}$. Then, the digital control logic shifts to phase 2 and the bypass window operates as in phase 1.

The proposed SAR ADC uses the monotonic switching sequence from phase 5 to phase 10, where the fine comparator generates $B_5 \sim B_{10}$. The monotonic switching sequence has the least switches and it reduces the power consumption of switch controller [10]. The digital decoder converts $B_{1\mathrm{p}} \sim B_{4\mathrm{p}}$, $B_{1n} \sim B_{4n}$ and $B_5 \sim B_{10}$ to $D_1 \sim D_{10}$ [19]. The digital decoder only requires four full adders.

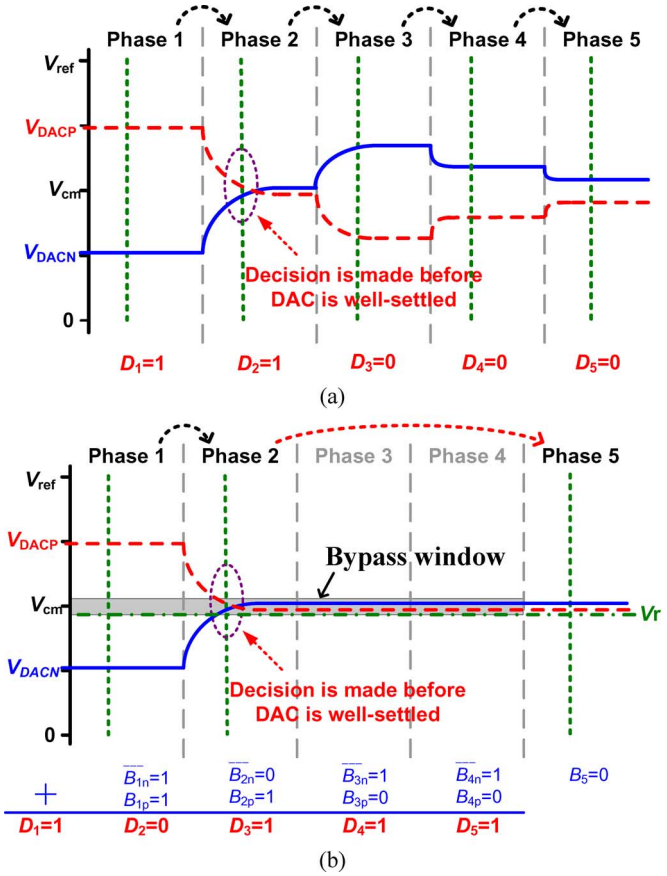


Fig. 5. Incomplete settling in (a) conventional SAR ADC and (b) bypass window SAR ADC.

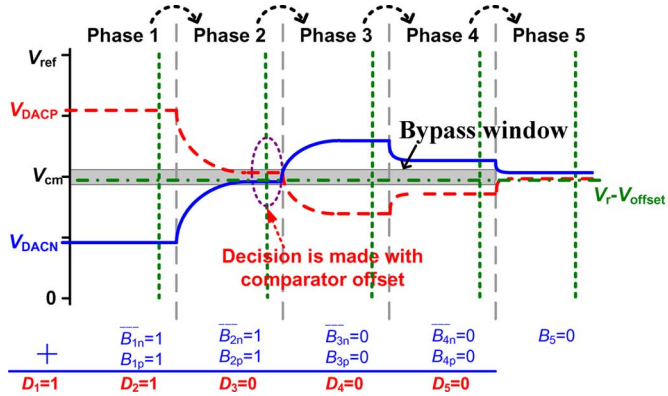


Fig. 6. Conversion process of bypass window SAR ADC with comparator offset.

III. Advantages of the Bypass Window

A. Incomplete Settling Tolerance

Fig. 5(a) shows an example of incomplete settling of the conventional SAR ADC. $V_{\rm DACP}$ and $V_{\rm DACN}$ are the voltages of the comparator input terminals and the dotted lines indicate the regeneration phases of the comparator. In phase 2, the comparator makes a decision before the DAC is well-settled, and the output code D_2 is "1", resulting in a wrong switching sequence. If no compensation method is adopted, the final output code will be incorrect.

The window function of the SAR ADCs is a tri-state comparison. The comparison results of the window are "1" when $V_{\rm DACP} > V_{\rm r}$ and $V_{\rm DACN} < V_{\rm r}$; "0" when $V_{\rm DACP} < V_{\rm r}$ and $V_{\rm DACN} > V_{\rm r}$; and "*BW*" when $V_{\rm DACP} > V_{\rm r}$ and $V_{\rm DACN} > V_{\rm r}$. "*BW*" means $V_{{\rm diff},i} < V_{\rm win}$. For a 32-LSB bypass window, when the window selects the "*BW*" state, the ADC keeps the DAC state and shifts to phase 5 to determine whether $V_{\rm DACP}$ is higher than $V_{\rm DACN}$. Therefore, when $V_{\rm DACP}$ and $V_{\rm DACN}$ are close to each other, the bypass window selects the "*BW*" state regardless of which one is higher. The proposed ADC makes an accurate decision in phase 5 with sufficient time for DAC settling.

Fig. 5(b) shows an example of incomplete settling of the bypass window SAR ADC. $V_{\rm DACP}$ and $V_{\rm DACN}$ sample the input signals from the previous example. In phase 2, the comparator makes a decision before the DAC is well-settled. The bypass window selects the "*BW*" state. Consequently, there is no DAC switching and the phase state of the ADC shifts to phase 5. In phase 5, the comparator determines that $V_{\rm DACN}$ is higher than $V_{\rm DACP}$ and the output code, B_5, is "0". The digital decoder converts $B_{1\rm p} \sim B_{4\rm p}$, $B_{1n} \sim B_{4n}$, and B_5 to $D_1 \sim D_5$; the final output code is "10111". Although incomplete settling occurs in phase 2, the bypass window method tolerates the settling error and provides accurate results. The highest number of comparisons in the proposed 10-bit ADC is 10, which is the same as the conventional SAR ADCs.

For the conventional SAR ADC with top-plate sampling, the required settling time of each comparison phase, the settling error is less than 1/2 LSB, can be derived as:

$$t_{{\rm conv},i} = (11-i)\tau_i \ln 2, \quad i = 2 \sim 10 \tag{5}$$

where $t_{{\rm conv},i}$ is the required settling time of $i_{\rm th}$ phase and τ_i is the RC time constant of the capacitive DAC in the $i_{\rm th}$ phase. For a 2^M-LSB bypass window SAR ADC, the required settling time can be derived as:

$$\begin{aligned} t_{BW,i} &= (10-M-i)\tau_i \ln 2, \quad i = 2 \sim 9-M \\ t_{BW,i} &= (11-i)\tau_i \ln 2, \quad i = 10-M \sim 10 \end{aligned} \tag{6}$$

where $t_{BW,i}$ is the required settling time of the bypass window SAR ADC in the $i_{\rm th}$ phase.

For a 32 LSBs bypass window, it tolerates settling error in the first four phases, which are the most critical for DAC settling.

B. Coarse Comparator Offset Tolerance

Fig. 2(b) shows the normal conversion process of a 32-LSB bypass window SAR ADC. In phase 2, the bypass window is triggered. Then, the proposed SAR ADC shifts to phase 5 to determine B_5 and the output codes are "11000".

If the coarse comparator has a voltage offset, $V_{\rm offset}$, the threshold voltage of the bypass window will change from $V_{\rm r}$ to $V_{\rm r} - V_{\rm offset}$. Suppose that coarse comparator has a negative offset voltage, $V_{\rm offset} < 0$, which makes the bypass window idle in phase 2, as shown in Fig. 6. Then, the proposed SAR ADC switches the DAC voltage and the coarse comparator compares $V_{\rm DACP}$ and $V_{\rm DACN}$ with $V_{\rm r}$-$V_{\rm offset}$ to determine whether bypass window is triggered in phases 3 and 4. Although the bypass window is not triggered in phase 2 due to the

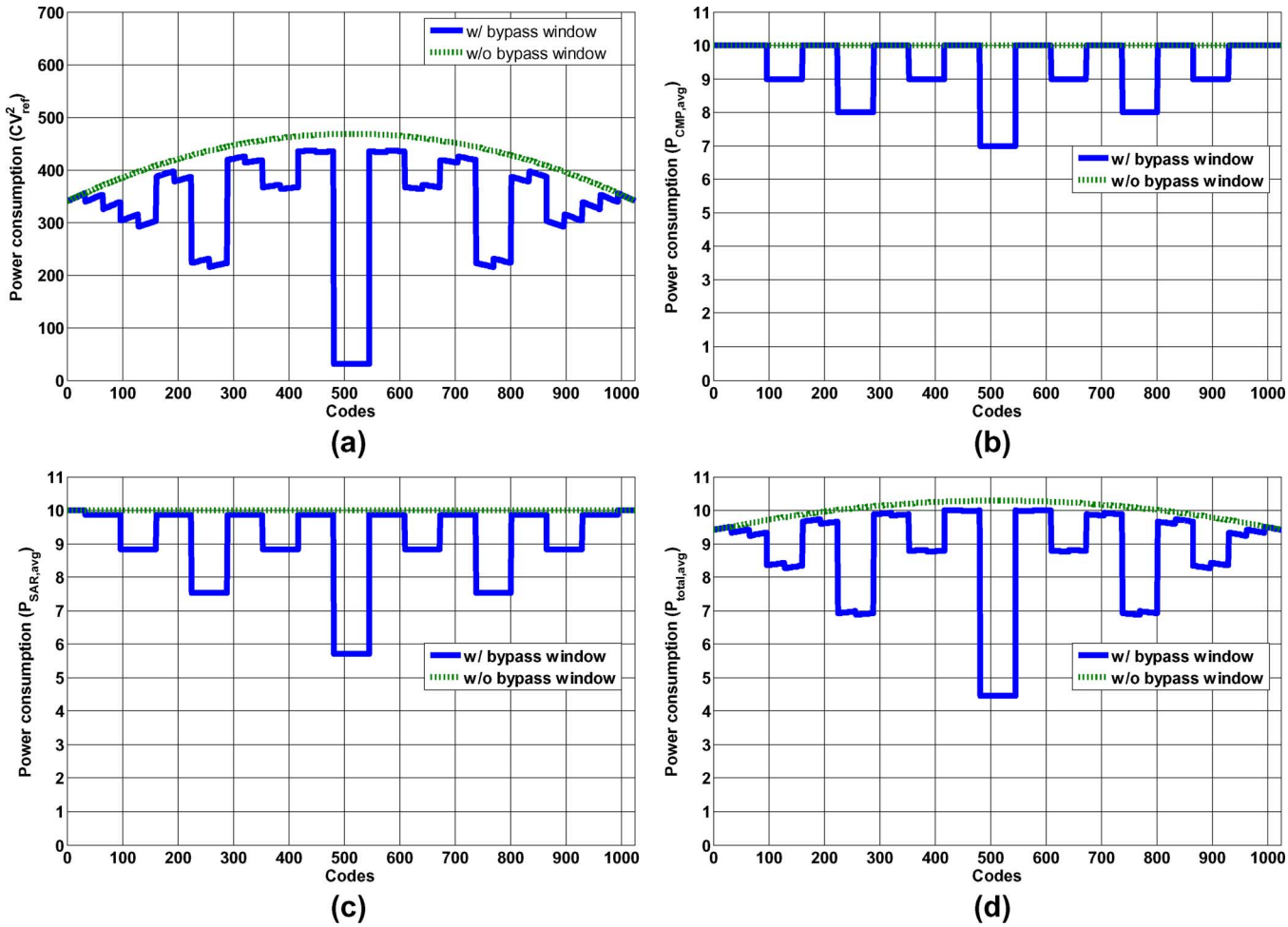


Fig. 7. Power consumption of (a) DAC switching, (b) comparator, (c) SAR, and (d) total block with 32-LSB bypass window.

comparator voltage offset, the conversion process continues as in the conventional SAR ADC. The output codes are "11000", which are the same as those shown in Fig. 2(b). For a 2^M-LSB bypass window SAR ADC, the offset tolerance range of the comparator can be derived as:

$$V_{offse,+} + |V_{offse,-}| = 2^{-(10-M)}V_{ref}, \quad M = 0 \sim 8 \quad (7)$$

where $V_{\text{offset},+}$ and $V_{\text{offset},-}$ are the positive and negative offset voltages of the coarse comparators, respectively.

C. Power Reduction of the 32 LSBS Bypass Window

Section II-B discusses the power reduction of different window sizes with a uniformly distributed input. In this work, a 32-LSB bypass window is adopted and the power reduction of each output code in each block is shown as below.

For an N-bit SAR ADC, if each digital output code is equiprobable, the average switching energy of the proposed SAR ADC without adopting a bypass window:

$$E_{\text{avg}} = \sum_{i=1}^{4}(2^{n-2-2i})(2^i - 1)CV_{ref}^2 + \sum_{i=5}^{N-1}(2^{n-2-i})CV_{ref}^2. \quad (8)$$

For the 10-bit case, the proposed SAR ADC consumes $171.5CV_{ref}^2$. However, it consumes $254.5CV_{ref}^2$ to pre-charge the capacitive DAC at the reset phase. The pre-charge energy of the proposed SAR ADC can be derived as:

$$E_{\text{pre}} = \sum_{i=1}^{4}(2^{n-2-i})CV_{ref}^2 + \sum_{i=5}^{N-1}\frac{15}{16}(2^{n-2-i})CV_{ref}^2. \quad (9)$$

The total switching energy is the sum of E_{avg} and E_{pre}. A comparison of switching energy for an ADC with and without the bypass window is shown in Fig. 7(a). Fig. 7(b) and (c) show the power consumption of comparator and SAR control logic (including the SA and switch buffers) versus the output codes, respectively. Moreover, a comparison of total power consumption for an ADC with and without the bypass window is shown in Fig. 7(d). When the output codes are between 480~543, the bypass window is triggered at phase 1. The power consumption of ADC is reduced by 53%. If the output codes trigger the bypass window in phases 2, 3, and 4, power consumption is reduced by 30%, 16%, and 6%, respectively. For a neural signal, which has small variations in magnitude for a large portion of time as shown in Fig. 1, assume 85%, 2%, 3%, and 5% of the time triggers the 32-LSB bypass window in phase 1, 2, 3, and 4, respectively. The overall power reduction is about 46%.

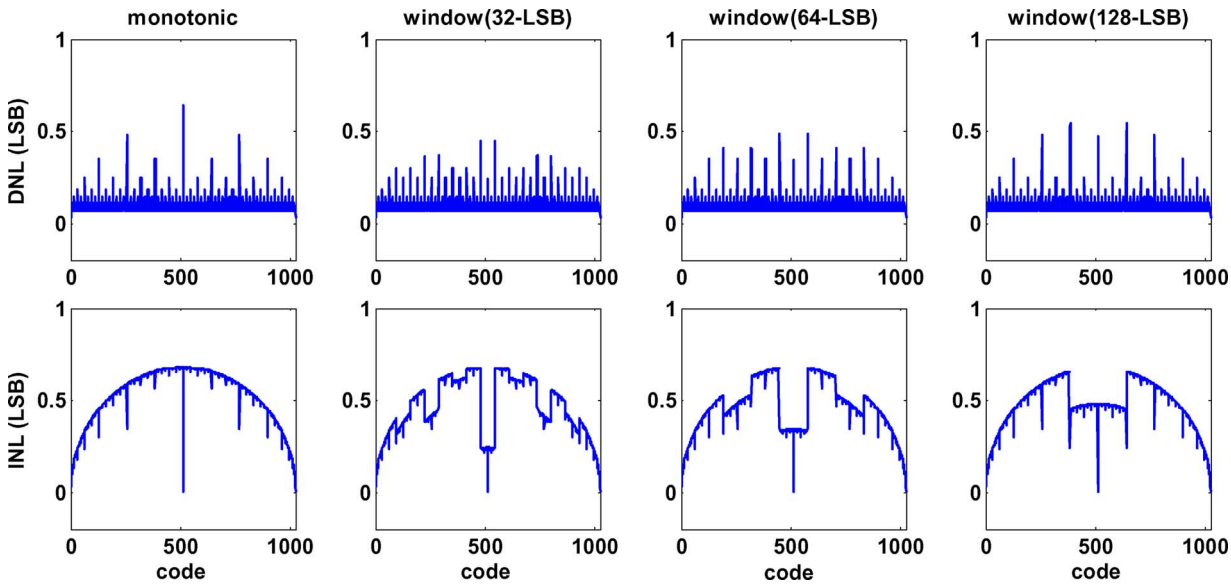


Fig. 8. Static performance with a SAR ADC using the monotonic switching method and bypass window with different window sizes.

D. Linearity Improvement of the Bypass Window

Besides the comparator offset and incomplete settling, the mismatch of the capacitor DAC is a main error source which deteriorates SAR ADC linearity. Assume a SAR ADC uses the monotonic switching method with a binary-weighted capacitor array and the error distribution of unit capacitors are independent and identically distribution (i.i.d). The maximum differential non-linearity (DNL) and integral non-linearity (INL) errors, which occurs at $FS/2$ and $FS/2-1$, respectively, where FS means the full scale signal, are identical and can be expressed as

$$\sigma_{INL,mono}\left(\frac{FS}{2}-1\right)=\frac{\sigma_0\sqrt{2^{n-1}}}{C_0}$$
$$\sigma_{DNL,mono}\left(\frac{FS}{2}\right)=\frac{\sigma_0\sqrt{2^{n-1}}}{C_0} \quad (10)$$

where C_0 is the unit capacitance, σ_0 is the standard deviation of the random offset of a unit capacitor and n is the ADC resolution. The detailed derivation procedures is given in the Appendix.

The same derivation procedures are applied to the proposed bypass window structure to evaluate the INL and DNL. For a bypass window SAR ADC with different window sizes, the INL and DNL errors at $FS/2-1$ and $FS/2$, respectively, are calculated as

$$\sigma_{INL,BW}\left(\frac{FS}{2}-1\right)=\frac{\sigma_0\sqrt{2^{M+1}}}{C_0}$$
$$\sigma_{DNL,BW}\left(\frac{FS}{2}\right)=\frac{\sigma_0\sqrt{2^{M+1}}}{C_0} \quad (11)$$

where 2^M is the bypass window size.

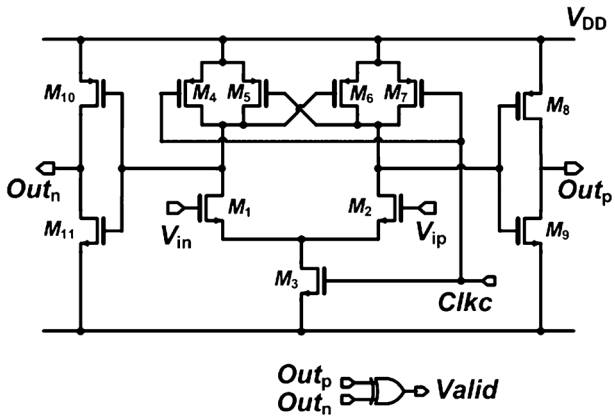
Fig. 8 shows the behavioral simulations for the SAR ADC using the monotonic switching method and bypass window for different window sizes (32, 64, and 128 LSBs). The only error source is the capacitor mismatch and comparator offset and incomplete settling error are excluded in these simulations. The DNL and INL curves are the root-mean-square (rms) values of 10,000 simulations and each capacitor cell has a Gaussian random error with a standard deviation of 3%. Because the two ends are fit to zero, the INL has a parabola shape.

SAR ADCs adopt binary-search algorithm to complete the data conversion. The INL values of each code are determined depend on binary-search algorithm, i.e., the INL error of $FS/2$ or $FS/4$ is generated at the MSB or MSB-1 decision, respectively. For top-plate sampling SAR ADCs, the MSB is generated without any capacitor switching, so the sampled signals on DAC plates remain ideal. The MSB decision of top-plate sampling SAR ADCs is errorless, so the middle of the INL curve in each case reaches 0. Hence, there are glitches in the INL curve as shown in Fig. 8. For some specific codes, which trigger the bypass window during the conversion phase, the bypass window reduces the unnecessary capacitor switching to suppress the DNL and INL errors. Although a small size bypass window enhances DNL performance, the small power reduction, comparator offset and incomplete settling tolerance should be considered.

IV. Implementation of Key Building Blocks

A. Dynamic Latch Comparator

Fig. 9 shows a schematic of the coarse and fine comparators. Although three comparators are used in this ADC, the bypass window can tolerate the coarse comparator voltage offset, as described in Section III-B. This work does not use comparator offset calibration technique and the transistor sizes of the coarse comparator are half that of the fine one. The transistor sizes of the fine comparator are shown is Fig. 9. Although two latch comparators are needed for phases 1~4, the average power consumption of each comparison phase is the same. Therefore, this work assumes that average power consumption of the latch comparator for each phase is $P_{\mathrm{CMP,avg}}$.



	Coarse	Fine
M_1	16μ / 0.18μ	8μ / 0.18μ
M_2	16μ / 0.18μ	8μ / 0.18μ
M_3	2μ / 0.18μ	1μ / 0.18μ
M_4	2μ / 0.18μ	1μ / 0.18μ
M_5	4μ / 0.18μ	2μ / 0.18μ
M_6	4μ / 0.18μ	2μ / 0.18μ
M_7	2μ / 0.18μ	1μ / 0.18μ
M_8	2μ / 0.18μ	2μ / 0.18μ
M_9	1μ / 0.18μ	1μ / 0.18μ
M_{10}	2μ / 0.18μ	2μ / 0.18μ
M_{11}	1μ / 0.18μ	1μ / 0.18μ

Fig. 9. Schematic of dynamic latch comparator.

The dynamic latch comparator adopts an N-type input pair. For low-supply-voltage operation, the number of cascaded transistors should be as low as possible. When $Clkc$ is low, the comparator is in the reset state; $Outp$ and $Outn$ are reset to $V_{\rm DD}$. Then, when $Clkc$ changes to high, the comparator is in the regenerate state to determine which terminal has the higher voltage. After the comparison is completed, a XOR gate is adopted to generate *Valid*, which is used for the asynchronous timing controller to trigger the next phase. Then, the asynchronous timing controller changes $Clkc$ to low and the comparator resets immediately.

The kickback noise is a critical issue for the comparator, which causes the voltage at the input terminals to rise or fall immediately and affect the comparison result. When the comparator has different capacitive or resistive loads at two input terminals, the rise/fall voltage is different, which can be taken as a comparator offset. However, for a fully differential SAR ADC, two binary-weighted capacitor arrays are used at the comparator input terminals, which have the same capacitance. When the voltage of the comparator input terminal are close to each other, the kickback noise for each terminal is the same. Therefore, it has no influence on the comparison results. Although the coarse comparators have different loading at the input terminals, the bypass window can tolerance the comparator offset as shown in Section III-B. The kickback noise does not affect the proposed SAR ADC performance.

B. Capacitive DAC

In the first comparison, the MSB is determined directly by comparing the top-plate voltages without any switching of the DAC. Therefore, a 9-bit DAC is needed in the SAR ADC. Fig. 4 shows the 9-bit binary-weighted capacitor array. The first four MSB capacitors are split into two equal parts, $C_{i\rm a}$ and $C_{i\rm b}$, where only one capacitor is switched to keep the common-mode voltage constant during phases 1~4. $S_{\rm p9a}$ to $S_{\rm p1}$ and S_{n9a} to S_{n1} are the control signals generated by the SAR control logic.

The DACs use metal-oxide-metal capacitors. The capacitance of a unit cell is about 4.5 fF. The input capacitance of the proposed SAR ADC is about 2.3 pF. To reduce the parasitic capacitance of the routing, the binary-weighted capacitor array is laid out based on a one-dimensional matching placement.

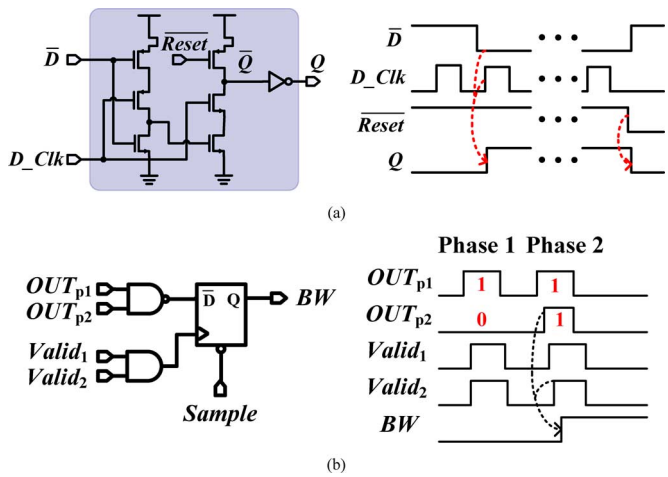


Fig. 10. Schematic and timing diagram of (a) proposed once-triggered DFF and (b) *BW* signal generator.

C. Digital Control Logics of Bypass Window SAR ADC

The phase generator of SAR ADCs is consisted of serial DFFs, which is triggered one by one and resets at the end of the conversion. Generally, the master-slave DFF is used to realize the phase generator. Fig. 10(a) shows the schematic and timing diagram of the proposed once-triggered DFF. When D is high and D_Clk rises to high, Q is triggered from low to high. Then, the once-triggered DFF is locked at high until *Reset* rises to high to reset it. Compared with master-slave DFF, the proposed DFF just requires eight MOS transistors, which reduces the power consumption, gate delay and active area.

When $V_{\rm DACP} > V_{\rm r}$ and $V_{\rm DACN} > V_{\rm r}$, the bypass window is triggered to generate *BW* signal. Fig. 10(b) shows the schematic and timing diagram of the *BW* signal generator consisting of a NAND, a AND, and a once-triggered DFF. $OUT_{\rm p1}$ and $OUT_{\rm p2}$ are the comparison results of the coarse comparator and $Valid_1$ and $Valid_2$ are triggered at the end of the coarse comparator. When $OUT_{\rm p1}$ and $OUT_{\rm p2}$ are high, the once-triggered DFF is triggered to generate *BW* and keeps the output until the ADC completes this data conversion.

The proposed SAR ADC uses asynchronous timing controller [7] to avoid the requirement of a high-speed clock generator. Fig. 11 shows a schematic and waveforms of the bypass window

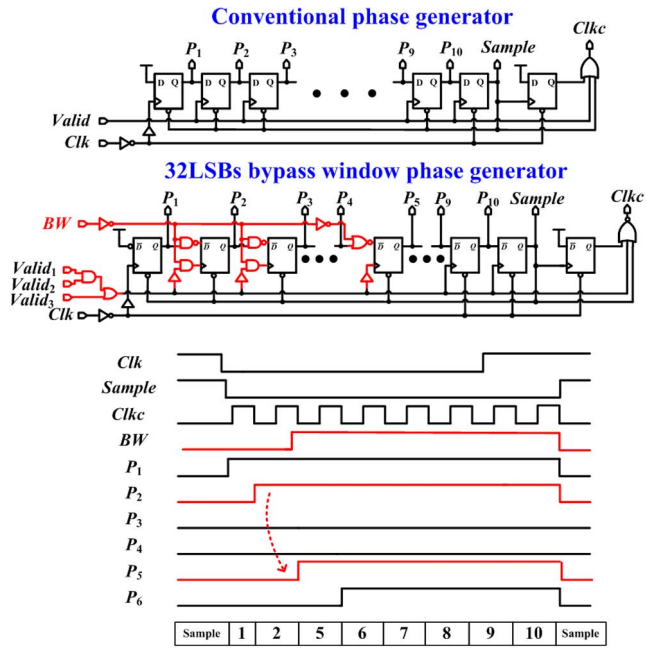


Fig. 11. Schematic and timing diagram of the conventional and proposed bypass window phase generator.

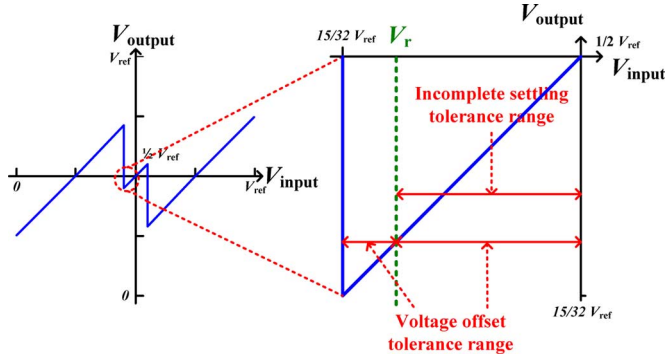


Fig. 12. Transfer curve of bypass window SAR ADC.

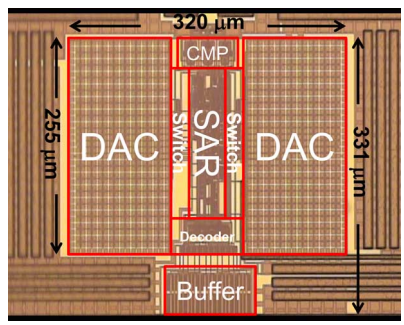


Fig. 13. Die micrograph.

phase generator. Clk is the system clock; $Valid_{1\sim3}$, for asynchronous timing control, is generated by the comparator output; *BW* is the trigger signal of the bypass window. Compared to conventional phase generator without bypass window, it requires 15 extra logic gates as shown in Fig. 11. Fig. 10 shows an example where the bypass window is triggered in phase 2 and *BW* is switched to high. Therefore, phases 3 and 4 are skipped and it just needs eight phases to complete the data conversion.

The bypass window SAR ADC requires some extra logic gates to achieve *BW* signal and phase skip function. From the post-simulation results, the power consumption of digital control logic of the bypass window SAR ADC and conventional SAR ADC are 0.536 and 0.478 μW, respectively. In this case, the bypass window does not be triggered from phase 1 to 4.

D. Reference Voltage of Bypass Window

The proposed SAR ADC requires a reference voltage, $V_{\rm r}$, and two coarse comparators to achieve the bypass window function. In this work, the window reference voltage, $V_{\rm r}$, is a constant value and it determines the transfer curve and window size. Theoretically, for a 32-LSB bypass window, $V_{\rm r}$ is $V_{\rm cm} - 16V_{\rm LSB}$, where $V_{\rm cm}$ is the common-mode voltage of the input signal and $V_{\rm LSB}$ is the voltage of a LSB.

Fig. 12 shows the transfer curve of a 32-LSB bypass window SAR ADC. $V_{\rm input}$ and $V_{\rm output}$ are the voltages of $V_{\rm DACP}(V_{\rm DACN})$ in phase i and $i+1$, respectively. The tolerance range of incomplete settling and the comparator offset can be derived as:

$$t_{BW,\rm tol} = \tau_i \ln\left(\frac{\frac{1}{2}V_{ref} - V_{\rm r}}{\frac{1}{2048}V_{ref}}\right), \quad i = 2 \sim 4$$
$$V_{\rm r} - \frac{1}{2}V_{ref} \le V_{\rm offset,tol} \le V_{\rm r} - \frac{15}{32}V_{ref} \qquad (12)$$

where $t_{BW,\rm tol}$ is the tolerance time of the incomplete settling and $V_{\rm offset,tol}$ is the tolerance offset voltage of the coarse comparator. Theoretically, if no incomplete settling and comparator offset occurs in the bypass window SAR ADC, the window reference voltage, $V_{\rm r}$, can be adjusted from 1/2 to 15/32 V_{ref} without affecting the ADC performance. It merely affects the power reduction of the bypass window. However, if the bypass window has comparator offset and incomplete settling problem, we can adjust $V_{\rm r}$ to tolerate it. For example, if the coarse comparator has a positive offset voltage, $V_{\rm r}$ can adjust higher than 15/32 V_{ref} to tolerate it. However, if the $V_{\rm r}$ is made higher than 15/32 V_{ref}, the tolerance range of the DAC incomplete settling, the reduction of power consumption and the linearity improvement will be reduced.

V. Measurement Results

The ADC was fabricated in 1P6M 0.18-μm CMOS technology. The micrograph of the ADC core is shown in Fig. 13. The active area (excluding output buffers) of the ADC is 0.082 $\rm mm^2$. In order to reduce power consumption, the proposed SAR ADC is designed for a low supply voltage (0.6 V). In this work, the supply voltage (0.6 V) is adopted as the reference voltage of the DAC switching, therefore, no reference buffer is used in the chip. With a 0.6-V reference voltage, the input signal swing of this ADC is rail-to-rail (1.2 $\rm V_{pp}$). However, there is a gain error for the capacitive DAC, which induces from the parasitic capacitance of the capacitor array and comparator input pair, the real input signal range is 1.13 $\rm V_{pp}$.

The window reference voltage, $V_{\rm r}$, is generated from the external power supply. Theoretically, $V_{\rm r}$ can adjust from 0.28125

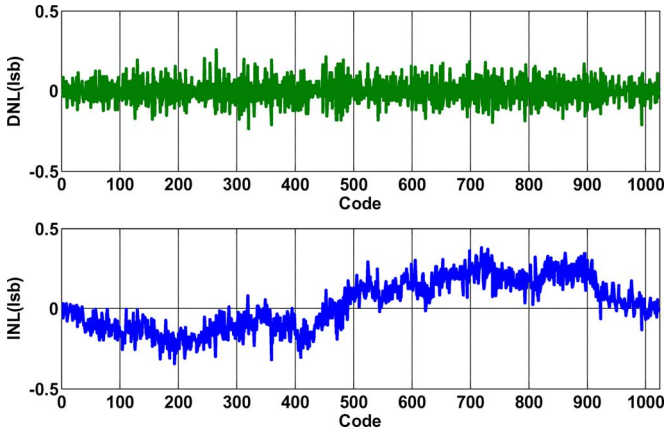


Fig. 14. DNL and INL at 200 kS/s.

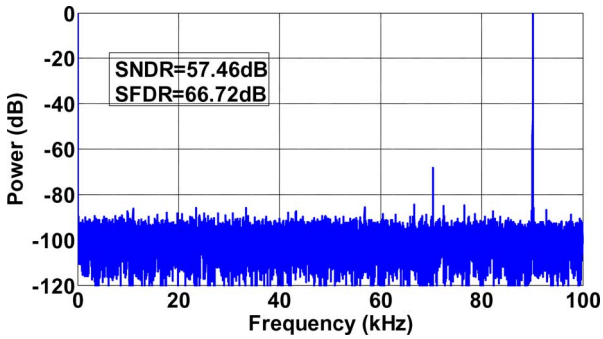


Fig. 15. Measured power spectrum at 200 kS/s and 90-kHz input.

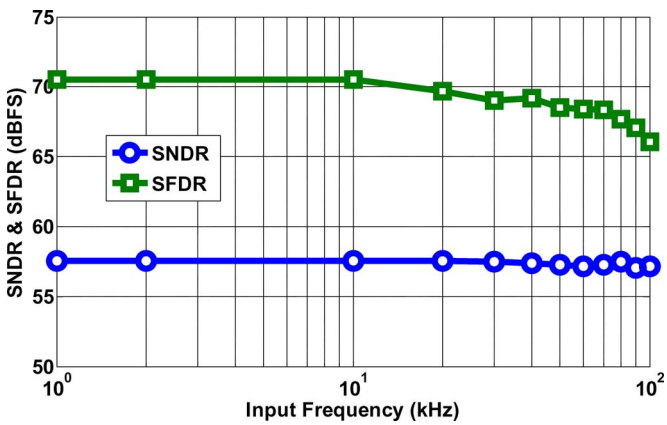


Fig. 16. Dynamic performance versus input frequency at 200 kS/s.

to 0.3 V. Actually, if the ADC demands to maintain the performance, V_r can adjust merely from 0.285 to 0.296 V. This is due to the gain, incomplete settling error, and positive offset voltage of the coarse comparator. For the maximum power reduction and maintain the ADC performance, V_r adjusts to 0.285 V for the measurement. The measurement results of the prototype are presented below.

The measured DNL and INL of the proposed ADC are shown in Fig. 14. The conversion rate is 200 kS/s with a 0.6-V supply. The peak DNL and INL are $-0.23/0.25$ LSB and $-0.34/0.38$ LSB, respectively.

Fig. 15 shows the measured FFT spectrum with an input frequency close to 90 kHz with a 0.6-V supply and a 200-kS/s sampling rate. The measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 57.46 dB and 66.72 dB, respectively.

Fig. 16 plots the measured SNDR and SFDR versus the input frequency at 200 kS/s with a 0.6-V supply. At a low input frequency, the measured SNDR and SFDR are 57.97 dB and 70.5 dB, respectively. The resultant efficient number of bits (ENOB) is 9.34. When the input frequency increases to 100 kHz, the

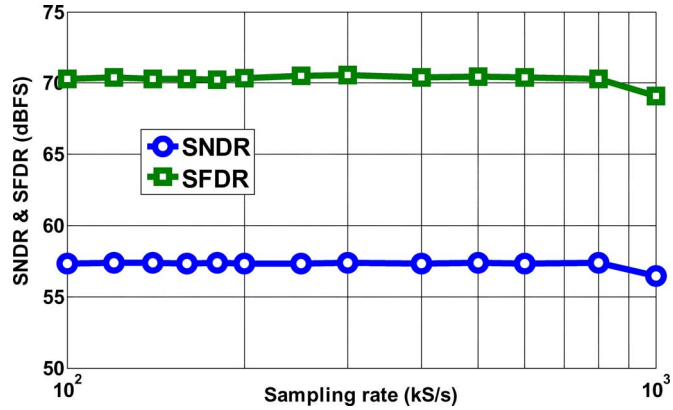


Fig. 17. Dynamic performance versus sampling frequency with 2-kHz input.

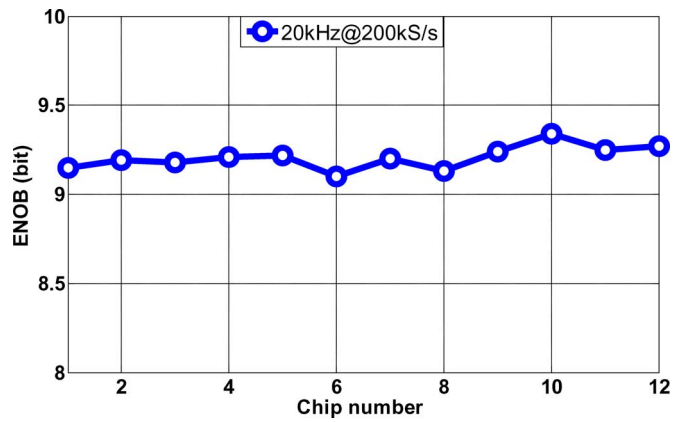


Fig. 18. ENOB of different chips with 20-kHz input and 200-kS/s sampling rate.

TABLE I
SPECIFICATION SUMMARY

Specification	Experimental result
Resolution (bits)	10
Supply Voltage (V)	0.6
Input Common-Mode Voltage (V)	0.3
Input Range (V_{pp})	1.13
Core Area (mm^2)	0.082
Peak DNL / INL (LSB)	-0.23~0.25 / -0.34~0.38
Sampling Frequency (kS/s)	200
SNDR / SFDR (dB)	57.98 / 70.4 (2 kHz)
	57.46 / 66.7 (90 kHz)
ENOB (bits)	9.34
Power (μW)	1.041 / 0.493 (BW)
FOM (fJ/con.step)	8.03 / 3.80 (BW)

TABLE II
COMPARISON TO STATE-OF-THE-ART WORKS

Specification	ESSCIRC'11 [12]	CICC'11 [16]	ISSCC'11 [20]	JSSC'11 [21]	JSSC'10 [22]	This work	This work
Architecture	SAR	SAR	SAR	SAR	SAR	SAR	SAR
Technology	180 nm	180 nm	65 nm	180 nm	65 nm	180 nm	180 nm
Supply Voltage (V)	0.9	0.5	0.55	0.6	1	0.6	0.6
Sampling Rate (kS/s)	1000	1	20	100	1000	200	1000
Resolution (bits)	10	10	10	10	10	10	10
ENOB (bits)	8.38	8.52	8.84	9.3	8.75	9.34	9.18
Power (μW)	7.16	0.0025	0.206	1.3	1.9	1.04	5.253
FOM (fJ/Conv.-step)	21.56	6.8	22.4	21	4.4	8.03	9.11
Active Area (mm^2)	0.48	0.05	0.212	0.125	0.026	0.082	0.082

measured SNDR and SFDR are 57.60 dB and 66.09 dB, respectively. The effective resolution bandwidth (ERBW) is over 100 kHz.

Fig. 17 shows the measured performance versus the sampling frequency with a 2-kHz sinusoidal stimulus. At a 0.6-V supply voltage, the ADC achieves a maximum sampling rate of 1 MS/s with an SNDR of 57.02 dB.

Fig. 18 shows the measured ENOB of 12 different chips with a 20-kHz sinusoidal stimulus and 200-kS/s sampling rate. The measured results show the ENOB are above 9.15.

At a 0.6-V supply and 200 kS/s, the power consumption excluding the output buffers is 1.04 μW. The comparator, SAR control logic, and DAC account for 17%, 53%, and 30%, respectively, of power consumption for the normal conversion process, where the input signal is a rail-to-rail sinusoidal stimulus. If the swing of the input signal is -24 dBFS, the bypass window is triggered in phase 1. In this case, the comparator, DAC, and digital control logic power consumptions are reduced by 30%, 93%, and 47%, respectively.

A specification summary of the ADC is given in Table I. With a 0.6-V supply voltage, the proposed ADC achieves an ENOB of 9.34 and an SNDR of 57.97 dB for a 2-kHz input frequency and a 200-kS/s sampling frequency. If the bypass window is triggered in phase 1, the total power consumption is 0.493 μW and the resultant FOM is 3.8 fJ/conversion-step (excluding the power consumed by the $V_{\rm r}$ generator). The total power consumption is reduced by about 53%.

To compare the proposed ADC with other state-of-the-art SAR ADCs, the figure-of-merit (FOM) is used.

$$FOM = \frac{Power}{2^{ENOB} \times \min\{2 \times ERBW, f_{\rm s}\}} \tag{13}$$

where $f_{\rm s}$ is the sampling frequency, and *ENOB* is the effective number of bits at *ERBW*.

Table II compares the proposed ADC with other state-of-the-art SAR ADCs [12], [16], [20]–[22]. Although the proposed ADC was fabricated in the 0.18-μm CMOS process, its FOM is comparable with those of other works implemented in the 65-nm CMOS process [20], [22].

VI. CONCLUSION

A SAR ADC with a 32-LSB bypass window, which is manipulated to reduce the power consumption of DAC switching, the latch comparator, and digital control logic, was presented. For small-variation-in-amplitude biomedical signals, the bypass window reduces power consumption by about half, and consequently extends battery life for biomedical electronic systems. Moreover, the proposed bypass window SAR ADC can suppress the maximum DNL and INL error and tolerate incomplete settling error and comparator offset voltage, which improves its dynamic and static performance.

APPENDIX

The capacitor array of SAR ADCs consists of multiple identical unit capacitors. Owing to process variation, the capacitance of unit capacitor deviates from the nominal value. Suppose the error distributions of unit capacitors are independent and identically distributed (i.i.d.) Gaussian random variables. The capacitance of a capacitor can be expressed as [24]

$$C_i = 2^{i-1}C_0 + \delta_i \tag{14}$$

where i is an integer representing the bit position, C_0 the unit capacitance and δ_i the error term. The MSB is the n-th bit for an n-bit ADC; the second MSB is the $(n-1)$-th bit, and so on. For an ADC with the monotonic switching method [10], the capacitor of the n-th bit consists of 2^{n-1} unit capacitors. Because the errors are i.i.d., the mean and variance of the error terms are

$$E[\delta_i] = 0,\ E\left[\delta_i^2\right] = 2^{i-1}\sigma_0^2 \text{ and } E\left[\delta_0^2\right] = E\left[\delta_1^2\right] = \sigma_0^2. \tag{15}$$

The final voltage difference of two top-plate nodes of the DACs after analog-to-digital conversion can be expressed as

$$V_{mono}(y) = V_{\rm inp} - V_{\rm inn} + V_{ref} - \frac{2S_nC_{n-1} + 2S_{n-1}C_{n-2} + \cdots + 2S_2C_1 + C_0}{\sum_{i=0}^{n-1} C_i} V_{ref} \tag{16}$$

where S_n represents the comparator decision for the n-th bit, $V_{\rm inp}$ and $V_{\rm inn}$ the input signal difference, V_{ref} the reference voltage. Subtracting the nominal value yields the error term shown in (17) at the bottom of the page, with variance

$$\begin{aligned} &E\left[V_{err,mono}^2(y)\right] \\ &= E\left[\frac{2\sum_{i=1}^{n-1} S_{i+1}\delta_i^2}{2^{2n-2}}V_{ref}^2\right], \quad y < 2^{n-1} \\ &= E\left[\frac{2\sum_{i=1}^{n-1} (1-S_{i+1})\delta_i^2}{2^{2n-2}}V_{ref}^2\right], \quad y \geq 2^{n-1} \end{aligned} \tag{18}$$

where y is the digital output. Note (17) and (18) must separates into two parts because the mean of $\sum_{i=0}^{n-1}\delta_i$ is 0. This error is also directly related to the INL of the ADC. Therefore, the maximum INL error of monotonic switching method is

$$\begin{aligned} \sigma_{INL,mono}\left(\frac{FS}{2}-1\right) &= \frac{\sqrt{E\left[V_{err,mono}^2(2^{n-1}-1)\right]}}{1LSB} \\ &\cong \frac{\sqrt{\frac{\sigma_0^2}{2^{n-1}C_0}V_{ref}^2}}{\frac{1}{2^{n-1}}V_{ref}} = \frac{\sigma_0\sqrt{2^{n-1}}}{C_0}. \end{aligned} \tag{19}$$

The DNL is the difference of two adjacent codes expressed as

$$DNL(y) = \frac{V_{err}(y) - V_{err}(y-1)}{1LSB}. \tag{20}$$

The maximum DNL of a binary DAC happens during $FS/2$ transition when the MSB capacitor is 1 and the other capacitors are 0 to the condition the MSB capacitor switches to 0 and the others to 1. The error term of $FS/2$ is generated at the MSB decision and it is error free of $FS/2$ with the top-plate sampling. Therefore, the variance of the maximum DNL error is derived as

$$\begin{aligned} &E\left[(V_{err}^2(2^{n-1}) - V_{err}^2(2^{n-1}-1))\right] \\ &= E\left[\left(0 - \left[\frac{2\sum_{i=1}^{n-1} S_{i+1}\delta_i^2}{2^{2n-2}}V_{ref}^2\right]\right)\right] \cong \frac{\sigma_0^2}{2^{n-1}C_0}V_{ref}^2. \end{aligned} \tag{21}$$

Therefore, the maximum DNL error of monotonic switching method is

$$\sigma_{DNL,mono}\left(\frac{FS}{2}\right) = \frac{\sigma_0\sqrt{2^{n-1}}}{C_0}. \tag{22}$$

Note (22) yield the same result as (19). The maximum DNL value is the same as the maximum INL.

For the bypass window SAR ADC, it can bypass several unnecessary switching, which reduces the accumulated error. For the codes nearby $FS/2$, the bypass window is triggered in phase 1 and the error term is shown in (23) at the bottom of the page. Therefore, the INL of $FS/2-1$ transition and DNL of FS/2 transition can be derived as

$$\begin{aligned} \sigma_{INL,BW}\left(\frac{FS}{2}-1\right) &= \frac{\sqrt{E\left[V_{err,BW}^2(2^{n-1}-1)\right]}}{1LSB} \\ &= \frac{\sigma_0\sqrt{2^{M+1}}}{C_0} \\ \sigma_{DNL,BW}\left(\frac{FS}{2}\right) &= \frac{\sqrt{E\left[0 - V_{err,BW}^2(2^{n-1}-1)\right]}}{1LSB} \\ &= \frac{\sigma_0\sqrt{2^{M+1}}}{C_0}. \end{aligned} \tag{24}$$

$$\begin{aligned} V_{err,mono}(y) &= \frac{2S_n\delta_{n-1} + 2S_{n-1}\delta_{n-2} + \cdots + 2S_2\delta_1 + \delta_0}{\sum_{i=0}^{n-1} C_i}V_{ref}, \quad y < 2^{n-1} \\ &= \frac{2(1-S_n)\delta_{n-1} + 2(1-S_{n-1})\delta_{n-2} + \cdots + 2(1-S_2)\delta_1 + \delta_0}{\sum_{i=0}^{n-1} C_i}V_{ref}, \quad y \geq 2^{n-1} \end{aligned} \tag{17}$$

$$\begin{aligned} V_{err,BW}(y) &= \frac{2S_{M+1}\delta_M + 2S_M\delta_{M-1} + \cdots + 2S_2\delta_1 + \delta_0}{\sum_{i=0}^{n-1} C_i}V_{ref}, \quad 2^{n-1} - 2^M < y < 2^{n-1} \\ &= \frac{2(1-S_{M+1})\delta_M + 2(1-S_M)\delta_{M-1} + \cdots + 2(1-S_2)\delta_1 + \delta_0}{\sum_{i=0}^{n-1} C_i}V_{ref}, \quad 2^{n-1} + 2^M \geq y \geq 2^{n-1}. \end{aligned} \tag{23}$$

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