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Six-bit 2.7-GS/s 5.4-mW Nyquist complementary metal-oxide semiconductor digital-to-analogue converter for ultra-wideband transceivers

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Abstract: This study presents a 6-bit 2.7 GS/s low-power digital-to-analogue converter (DAC) for ultra-wideband transceivers. A '2(thermometer) + 4(binary)' segmented architecture is chosen to reach a compromise between the current source cell's area and the operating speed of the thermometer decoder. In addition, the proposed pseudo-thermometer structure improves the DAC's dynamic performance. The bipolar current source cell and latch clock delay technique are employed to reduce the power consumption in the analogue and digital parts, respectively. Moreover, the compact de-glitch latch presented in this study simplifies the conventional latch design and layout. This DAC was implemented in a standard 0.13 μm 1P8M complementary metal-oxide semiconductor technology with the active area of 0.0585 mm^2. The measured differential non-linearity and integral non-linearity are less than 0.09 and 0.11 least significant bit, respectively. The measured spurious-free dynamic range is more than 36 dB over the Nyquist frequency at the sampling frequency of 2.7 GHz. The DAC consumes 5.4 mW with a near-Nyquist sinusoidal output at 2.7 GS/s, resulting in a better figure of merit of 31 fJ/conversion-step than other published arts.

1 Introduction

In modern wideband wireless communication systems, low-resolution and high-speed data converters are increasingly required for signal processing [1]. Moreover, the evolution of integrated circuit (IC) fabrication technology has led to considerable growth in the integration of more components to include more functionality. Power consumption is one of the most important issues in hand-held or portable electronic devices, and thus integrating more power-efficient components has become critically important in power-limited applications.

Current-steering digital-to-analogue converters (DACs) are widely used for high-speed applications [2]. In multimode communication systems, DACs need to be operated at various sampling rates that conform to the system requirements for different operations. For example, in ultra-wideband (UWB) applications, multiband orthogonal frequency-division multiplexing (MB-OFDM) UWB and direct spectrum code division multiple access (DS-CDMA) UWB are the two major technologies currently in use [3]. In MB-OFDM UWB technology, the spectrum from 3.1 to 10.6 GHz is divided into 14 channels, each with a 528 MHz channel bandwidth. Consequently, a DAC with a clock rate higher than 1.056 GS/s is required. In contrast, the highest data rate is 1.35 Gbps with DS-CDMA UWB technology, so a system with two times oversampling of the data signal needs the DAC to be operated at 2.7 GS/s [4].

In MB-OFDM UWB systems, it is easy to realise the required DAC with power-efficient static complementary metal-oxide semiconductor (CMOS) logic for digital circuits, but this DAC may not be able to reach 2.7 GS/s for DS-CDMA UWB systems. In [4], a DAC is presented with more pipeline stages in the thermometer decoder to reach 2.7 GS/s. Nevertheless, this DAC inevitably requires more sequencing elements, namely latches or flip-flops, and consequently increases both clock loading and power consumption. In [5], current mode logics (CMLs) are adopted to implement the digital parts of the DAC for achieving faster logic switching. Nonetheless, CMLs consume the same power at different operating frequencies, and dissipate considerable power at low operating frequencies. Accordingly, with the aim of increasing power efficiency, two DACs are necessary for the two applications. One with less power consumption and a lower operating speed is integrated into MB-OFDM UWB systems, and the other with more power dissipation and a higher operating speed is designed for DS-CDMA ones.

In this paper, we propose a power-efficient 6-bit DAC with the operating rate ranging from 1 to 2.7 GS/s for full integration into MB-OFDM and DS-CDMA UWB systems. In this DAC, a '2(thermometer) + 4(binary)' segmented architecture is chosen in a detailed analysis, and latch clock delay technique [6] is also employed to take on the challenges of high-speed decoder design. Therefore the decoder in this DAC is realised with power-efficient static CMOS logic without inserting more pipeline stages. In addition, the segmented architecture combined with the proposed pseudo-thermometer structure and the compact de-glitch latch design presented in this work are

manipulated to improve DAC's dynamic performance and to reduce the design complexity of digital circuitries, therefore cutting power consumption. Furthermore, the bipolar current source cell [7] is also adopted to reduce the power consumption in current source cells. Consequently, the figure of merit (FOM) of this DAC at 2.7 GS/s is 31 fJ/conversion-step, less than that achieved in several recent publications on wireless personal area network (WPAN) applications [1, 4, 7–10]. The remainder of this paper is organised as follows: the DAC architecture is presented in Section 2, whereas Section 3 introduces the low-power building blocks of this DAC. Section 4 presents the layout considerations, while the measurement results are given in Section 5. Finally, we conclude this work in Section 6.

2 Architecture

Binary, thermometer and segmented architectures are available to implement a current-steering DAC. The segmented one strikes a balance between the strengths and weaknesses of the binary and thermometer ones, and therefore is preferred. However, the different thermometer-coded bits in different segmented architectures with the same resolution result in different static and dynamic performances and operating speeds [2], so the number of the thermometer-coded bits should be carefully chosen.

Generally, some static performance parameters of a DAC, such as integral non-linearity (INL) and differential non-linearity (DNL), must be small enough (e.g. 0.5 least significant bit (LSB)) to ensure monotonicity and the linearity of the DAC. Additionally, in this work, we aim both INL and DNL to be less than 0.5 LSB with a 99.7% yield.

In statistical analysis, in an N-bit DAC, if the error of a unit current source is normally distributed with zero mean and a standard deviation $\sigma(I)$, and each output level is uncorrelated with each other, the maximum standard deviation of INL and DNL will be written as

$$\sigma\mathrm{INL}_{\max} = 0.5\sqrt{2^N - 1}\,\frac{\sigma(I)}{I}(\mathrm{LSB}) \tag{1}$$

$$\sigma\mathrm{DNL}_{\max} = \sqrt{2^{B+1} - 1}\,\frac{\sigma(I)}{I}(\mathrm{LSB}) \tag{2}$$

with $\sigma\mathrm{INL}_{\max}$ the maximum standard deviation of INL, N the resolution of the DAC, $\sigma(I)/I$ the relative standard deviation of a unit current source, $\sigma\mathrm{DNL}_{\max}$ the maximum standard deviation of DNL and B the number of the binary-weighted bits of the DAC. Equation (2) is valid for the binary ($B = N - 1$) and thermometer ($B = 0$) implementation [2, 11]. According to (1) and (2), if $\sigma\mathrm{DNL}_{\max}$ is less than $\sigma\mathrm{INL}_{\max}$, B should be less than or equal to $N - 3$. This means that the INL error will become a limiting factor of static performance design specifications without considering the DNL error if the thermometer-coded bits in the segmented DAC are larger than or equal to 3.

In reality, there are strong correlations between output levels. Additionally, different thermometer-coded bits in different segmented architectures with the same resolution result in different INL and DNL behaviours [12]. Consequently, in this work, Monte-Carlo simulations are performed to obtain the accurate standard deviation of the unit current source cell to estimate the area of the current source cell. Fig. 1 shows the results of the INL and DNL yields of a 6-bit DAC with three different architectures including binary, '2(thermometer) + 4(binary)' and '3(thermometer) + 3(binary)' ones. These simulations are carried out under the prerequisite that all the basic current sources in these architectures have the same physical dimensions to eliminate systematic errors [13]. The results are in agreement with those obtained from statistical analysis. The matching requirements of current sources for a 99.7% INL yield in the three architectures are almost the same. In addition, in the '3(T) + 3(B)' architecture, the 99.7% INL yield specification is one of the limiting factors in determining the area constraint of the unit current source cell. However, the relative current source standard deviations in these architectures for a 99.7% DNL yield are different, and the binary one has the most demanding matching requirement. Moreover, in the binary and '2(T) + 4(B)' architectures, the 99.7% DNL yield requirement becomes one of the strict specifications to determine the current source cell's area. If we choose the '3(T) + 3(B)' architecture, a small area in unit current source cells can be designed so as to have a low-cost DAC. However, the thermometer decoder in this architecture is composed of three input NAND and NOR gates, and consequently it is not easy to reach 2.7 GS/s with power-efficient CMOS logic. Inserting more pipeline stages in the thermometer decoder solves this problem [4], but consumes more power due to the extra sequencing elements and heavier clock loading. Finally, we choose the '2(T) + 4(B)' architecture to make a compromise between the current source cell's area and the operating speed of the thermometer decoder.

Adopting more thermometer-coded bits in a DAC can improve its dynamic performance. However, a decoder with more thermometer-coded bits has a noticeable decrease in

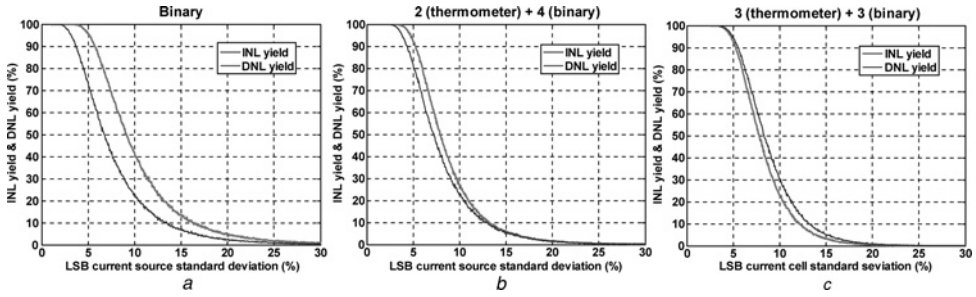

Fig. 1 *Monte-Carlo simulations of the INL and DNL yields of a 6-bit DAC with three different architectures against relative LSB current source standard deviation*

a Binary
b '2(thermometer) + 4(binary)'
c '3(thermometer) + 3(binary)'

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its operating speed. An alternative method, called pseudo-segmentation [13], has been shown to improve dynamic performance without a thermometer decoder. Its basic concept is to arrange the digital outputs of the binary architecture just the same as those of the thermometer or segmented one. The performance of a DAC is limited by amplitude and timing errors. Employing this skill balances the delay difference between different binary-weighted bits, so it can reduce the glitch error and thus enhance dynamic performance. However, a DAC built with this method still has the property of a binary architecture, and suffers from significant mismatch errors that result in larger DNL. According to the previous Monte-Carlo simulations, a larger transistor area needs to be designed to meet the DNL specification. To tackle this issue, we propose a method called pseudo-thermometer to obtain the same dynamic performance as the thermometer architecture and to relax the matching requirement of the binary one. Figs. 2 and 3 show 3-bit pseudo-segmentation and pseudo-thermometer decoders, respectively. The 3-bit thermometer, pseudo-segmentation and pseudo-thermometer decoders all have the same digital inputs and outputs connected to the subsequent latches and switches. Therefore the DAC with the pseudo-segmentation or pseudo-thermometer decoder can balance the delay difference between different binary-weighted bits and control the switching behaviour as effectively as a DAC with the thermometer decoder. Additionally, a 6-bit DAC with the 3-bit pseudo-thermometer decoder has the property of the '2 + 4' segmented architecture, and

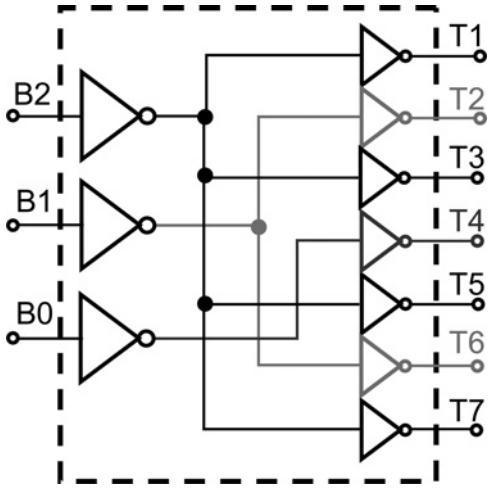

Fig. 2 *3-bit pseudo-segmentation decoder*

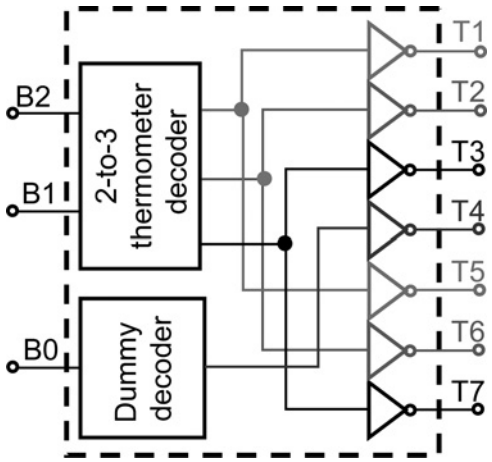

Fig. 3 *3-bit pseudo-thermometer decoder*

therefore a smaller transistor area in this work than in the binary architecture is designed to meet the same DNL specification. Fig. 4 shows the simulated 2.7 GS/s fast Fourier transform (FFT) spectra of a 6-bit DAC with three different implementations, including the '2(T) + 4(B)' architecture, the '2(T) + 4(B)' architecture with the 3-bit pseudo-thermometer decoder and the binary architecture with the 3-bit pseudo-segmentation decoder. The spurious free dynamic range (SFDR) of the 6-bit DAC with the 3-bit pseudo-thermometer decoder is better than that of the '2(T) + 4(B)' architecture about almost 3 dB through simulation. Additionally, the simulated SFDR of the 6-bit DAC with the 3-bit pseudo-segmentation decoder is equal to that with the 3-bit pseudo-thermometer decoder.

From the perspective of static performance, in the 3-bit pseudo-segmentation decoder, when inputs transit from 011 to 100, the outputs {T2, T4 and T6} are pulled down, and all the other outputs {T1, T3, T5 and T7} are pushed higher. This behaviour is the same as a 3-bit binary decoder. During the same input transition, in the 3-bit pseudo-thermometer decoder, the outputs {T3 and T7} remain high, only the output {T4} is pulled down, and the outputs {T2 and T6} are pushed higher. This behaviour is similar to a '2(T) + 1(B)' decoder, and such an arrangement exhibits a better DNL. In other words, for a given DNL requirement, the DAC with the pseudo-thermometer decoder relaxes the matching requirements of the current source cells more than the binary one or a DAC with the pseudo-segmentation decoder.

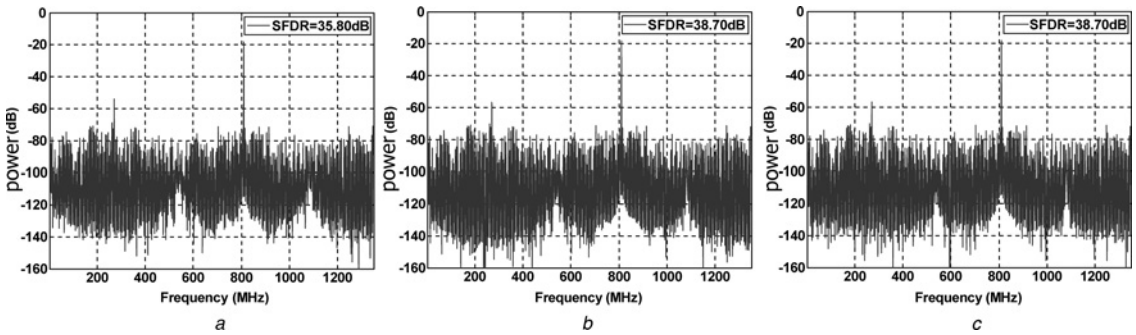

Fig. 4 *Simulated FFT spectra of a 6-bit DAC with three different implementations*

a '2(T) + 4(B)' architecture
b '2(T) + 4(B)' architecture with 3-bit pseudo-segmentation decoder
c Binary architecture with 3-bit pseudo-thermometer decoder

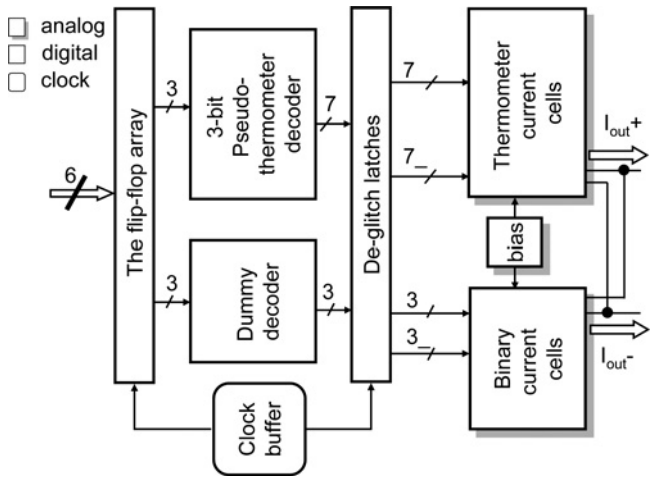

Fig. 5 *Block diagram of the proposed 6-bit DAC*

In this design, the minimum required area of the unit current source transistor is 62% less than that of the binary architecture, and the current source array occupies 54% of the active area. Therefore the binary architecture with the pseudo-segmentation skill has an extra 33% total area more than this design. The pseudo-thermometer decoder has an additional 2-to-3 decoder than the pseudo-segmentation one, but the extra decoder only occupies 1.5% of the total area. The increase in area compared with the reduction in area is thus negligible. Additionally, the 3-bit pseudo-thermometer decoder matches the timing margin at 2.7 GS/s due to only having a 2-to-3 decoder. Consequently, the DAC illustrated in Fig. 5 is proposed to improve dynamic performance and to balance the DAC's operating speed against the current source cell's area.

3 Low-power building blocks

3.1 Current source cell

Fig. 6 shows two different current source cells: unipolar and bipolar. In the unipolar current source cell, if the tail current is I, the single-ended output voltage will be either VDD or VDD − RI. Therefore the single-ended swing is RI, and the peak to peak differential swing is 2RI. In the bipolar one, the single-ended output voltage is either VDD/2 + RI or VDD/2 − RI, so the single-ended swing is 2RI, and the peak-to-peak differential swing is 4RI. The power consumption in both architectures is $VDD \times I$, and the swing of the bipolar current source cell is two times the swing of the unipolar one. From the standpoint of power consumption, the bipolar one with the same output swing as the unipolar one only consumes half the power [7]. Therefore the DAC presented in this work uses a bipolar current source cell to reduce the power consumption, and more design considerations in this paper related to this cell than in [7] are introduced below.

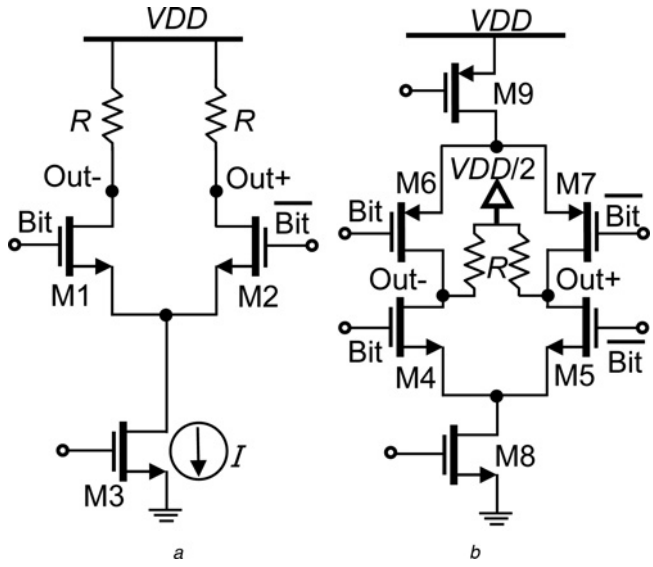

Fig. 6 *Current source cells*

a Unipolar
b Bipolar [7]

The transistor mismatch in the current source cells causes the non-linearity in a DAC. Appropriate sizing of the transistor in the current source cells must be undertaken to fulfil the matching requirement [14]. The signal-dependent output impedance at the output of the DAC also induces non-linearity distortion. The current source cell should provide sufficient output impedance over the Nyquist frequency to alleviate this problem [15]. The requirements of the transistor's area and output impedance are summarised as

$$(\mathrm{WL})_{\min} = \frac{1}{2}\left[A_\beta^2 + \frac{4A_{\mathrm{VT}}^2}{(V_{\mathrm{GS}} - V_T)^2}\right] \Big/ \left(\frac{\sigma(I)}{I}\right)^2 \quad (3)$$

$$\mathrm{IMD3} = \frac{14g_{\mathrm{imp}}^2 N^2 + 16g_l^2 + 16g_l g_{\mathrm{imp}} N}{3g_{\mathrm{imp}}^2 N^2} \quad (4)$$

with $\mathrm{WL}_{\min}$ the minimum required transistor's area of a unit cell, A_β and A_{VT} the process parameters, $V_{\mathrm{GS}} - V_T$ the gate overdrive voltage of a unit transistor, $\sigma(I)/I$ the relative LSB current source standard deviation, IMD3 the desired third-order inter-modulation distortion, g_l and g_{imp} the reciprocals of the load resistance and required frequency-dependent impedance, and N the number of current source cells.

The unit current source transistor is carefully designed to satisfy the above requirements. Moreover, the appropriate layout skills described in Section 4 are utilised to alleviate the global gradient variation error and ensure the current source cells have the same environment as each other.

3.2 Latch clock delay technique

In this DAC, the digital circuits are designed to perform the decoding and distribution in half the clock period, that is, 185 ps. Consequently, it is difficult to only employ power-efficient static CMOS logic in digital circuits without other circuit techniques. Possible solutions are adopting more pipeline stages [4] and/or using edge-triggered flip-flops instead of level-sensitive latches [9] to increase the processing speed of the digital circuits. In these circuit techniques, more clock loading and sequencing elements are required, resulting in more power consumption and greater chip area. To confirm that digital outputs are correctly latched in the DAC, we employ latch clock delay technique [6] to improve the operating speed of digital circuits, and propose some derivatives and modifications.

In Fig. 7, the input data for a DAC are sampled at the rising edge of the clock signal (CLK). Therefore the digital outputs of the decoder should be ready before the rising edge of the

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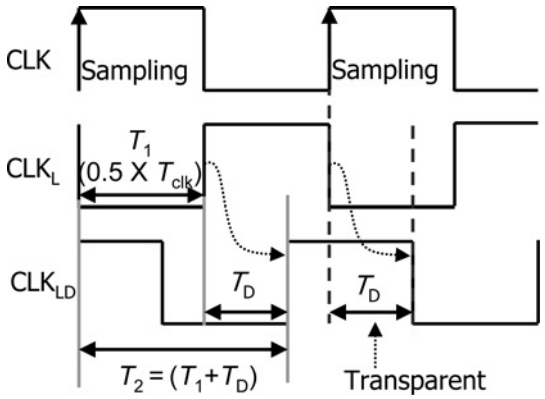

Fig. 7 *Timing diagram of latch clock delay technique*

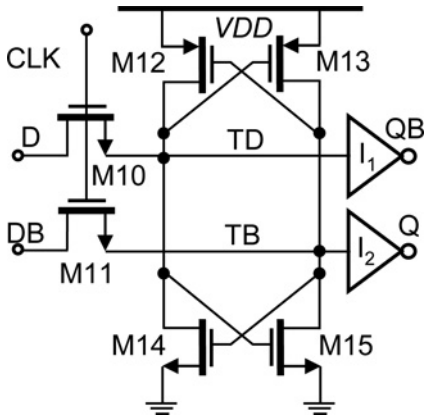

Fig. 8 *Conventional latch*

clock signal of latches (CLK_L) to avoid generating the unwanted signal. If a delay (T_D) is introduced, CLK_L will become the delayed clock signal of latches (CLK_{LD}), and the processing time of the digital circuits can be extended from half a clock period (T_1) to T_2, which is T_1 plus T_D. Increasing T_D to the maximum value, which is equal to T_1, improves the DAC's operating speed by a factor of two. However, if the minimum propagation delay of the digital circuits (T_{Pmin}) is less than T_D, the subsequent latches will capture the incorrect data. Accordingly, the value of T_D is determined by the following equation

$$\min(0.5 \cdot T_{clk}, T_{Pmin}) > T_D > 0 \quad (5)$$

Reducing T_{Pmin} decreases the available delay time, T_D. The processing time of the digital circuits is reduced, so a dummy decoder to equalise the delay between the MSBs and LSBs parts is inserted. Increasing T_{Pmin} can improve the operating speed of the digital circuits, but additional power dissipation is caused owing to buffers being inserted in the non-critical paths. In [6], T_D is designed as the time from digital inputs to the outputs of the digital circuits. In this design, the processing time of digital circuits is a little longer than half a clock period in the worst simulation conditions. As a result, T_D is not designed as the processing time of digital circuits. We review Fig. 7 and observe that CLK_L is the inversion signal of CLK, so the straightforward and power-efficient way to generate CLK_L is inserting an odd number of inverters after CLK. Therefore the propagation delay of the inserted inverters becomes T_D, and the signal after the inserted inverters becomes CLK_{LD}. To ensure the functionality in this design with regard to the process, temperature and other variations, as well as clock jitter, we design T_D as three times the inverter's delay which is about 90 ps. The processing time of the digital circuits is extended to guarantee their outputs are correctly latched. Moreover, the power consumption is reduced because static CMOS logic is employed in all the digital circuits without using more pipeline stages and/or edge-triggered flip-flops.

3.3 Compact de-glitch latch

Latches perform the final synchronisation of the control signals at the switch transistors. The conventional latch in [13] is shown in Fig. 8. In this latch, the outputs of pass transistors (M10–M11) are followed by both n-type MOS (NMOS) and p-type MOS (PMOS) cross-coupled transistors (M12–M15). Moreover, the pass transistors conduct the voltage range from ground (GND) to the degraded '1', which is the gate voltage that is almost VDD in digital circuits minus the threshold voltage. One possible solution for passing full-swing digital signals is to use transmission gates replacing NMOS pass transistors [1]. However, two-phase clock signals and extra PMOS transistors are required for this, and the clock loading has the highest switching activity in the system, so the power consumption is increased.

From the viewpoint of low power dissipation, the circuits should be designed as simply as possible. We review the conventional latch in Fig. 8. When the clock is high, if this latch does not have cross-coupled transistors (M12–M15), and the inputs, D and DB, are VDD and GND, the internal nodes, TD and TB, will be degraded '1' and GND. Under the same input conditions, if this latch is only without NMOS cross-coupled transistors (M14–M15), the PMOS transistor (M12) will be fully turned on to push the node TD which is degraded '1' up to VDD. Comparatively, the node TD will still be degraded '1' if this latch is just without PMOS cross-coupled transistors (M12–M13). In this situation, if the supply voltage is less than two times the threshold voltage, the NMOS transistor of the inverter (I_1) will not be turned on to make the node QB floating. Consequently, NMOS cross-coupled transistors (M14–M15) are removed without influencing the functionality of the latch, even at a low supply voltage. Accordingly, the compact latch proposed in this work to simplify the latch design and reduce silicon area is presented in Fig. 9. After this modification, the compact latch becomes a dynamic one, and the functionality is still correct. If the nodes, TD and TB, are VDD and GND, the PMOS transistor (M18) will always be a keeper to maintain the node TD at VDD after clock falling. The area of this latch is reduced on account of removing the NMOS cross-coupled

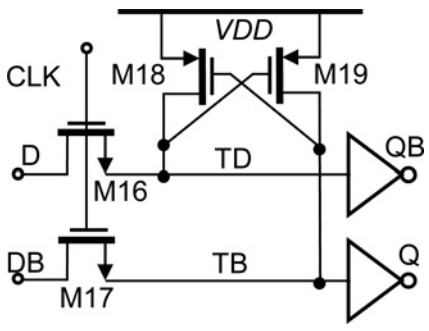

Fig. 9 *Proposed compact latch*

transistors. Furthermore, this latch brings another advantage of reducing the capacitance after the pass transistors, and thus we can reduce the required input signal strength to cut the power of the input buffers.

4 Layout considerations

The mismatch of the current source cell results from random and systematic errors. Using a sufficient transistor area alleviates the random errors and maintains the static matching, and this issue has been discussed in Section 3. The systematic errors originate from the edge effect and gradients in temperature and physical parameters, and using complex switching schemes can compensate for these [2, 16]. However, this induces the more parasitic capacitance in the source node of switching transistors. This extra capacitance further degrades the output impedance of the current source cell, especially in high signal frequencies, and therefore decreases the required SFDR. Consequently, it is not necessary to adopt the complex switching schemes due to the relatively small area of the current source array and high speed operating considerations. As a result, a simple centroid switching scheme as in [4] is employed to compensate for systematic errors with the less parasitic capacitance. The LSB current is implemented only with a unit transistor. The binary-weighted current source cell is realised with the same binary-weighted number of unit transistors connected in parallel with a finger structure to reduce the source/drain junction capacitance and silicon area. Consequently, a compact and matching current source array is achieved. In addition, the digital part is designed as compactly as possible in order to reduce the propagation delay and power dissipation. The difference in delays between the current sources and the clock is another problem that causes bad dynamic performance. The tree-like connections for both the clock net and output nets are employed to balance the delays [17]. Consequently, a compact active area with better dynamic performance is achieved, and Fig. 10 shows the chip microphotograph with an active area of 185 μm × 315 μm.

5 Measurement results

All the measurements are performed on a differential output. Both the analogue and digital supply voltages are 1.2 V. The total output current of this DAC is 1.5 mA, and the differential peak to peak output swing is less than 0.3 V. The measured DNL and INL profiles against input code numbers are shown in Fig. 11. The measured DNL and INL are less than 0.09 and 0.11 LSB, respectively.

The dynamic performance of this DAC has been measured at the conversion rates of 1.056 and 2.7 GS/s. Fig. 12 summarises the measured SFDR results as a function of the normalised input frequency at 1.056 and 2.7 GS/s. On the horizontal axis, the normalised frequency is defined as the single tone's fundamental frequency (f) divided by the sampling frequency (f_s). The measured SFDR results are more than 40 and 36 dB over the Nyquist frequency at the sampling rates of 1.056 and 2.7 GS/s. The SFDR of the DAC at 2.7 GS/s decreases because of non-linear switching transients in a shorter clock cycle. Fig. 13 shows that the measured SFDR with a near-Nyquist output signal at 2.7 GS/s is 36.07 dB. The spectrum for a two-tone test where the frequencies of the two tones are 532 and 552 MHz at 2.7 GS/s is given in Fig. 14. The figure shows IMD3 is better than 41 dB. The measurement results show that the performance of this DAC meets the requirements of both the MB-OFDM and DS-CDMA UWB systems. The power consumption with a near-Nyquist output signal at 1.056 and 2.7 GS/s are 3.2 and 5.4 mW, respectively.

In order to compare this work with other previous ones, we list the published arts, [1, 4, 7–10], with similar specifications, as well as those with other

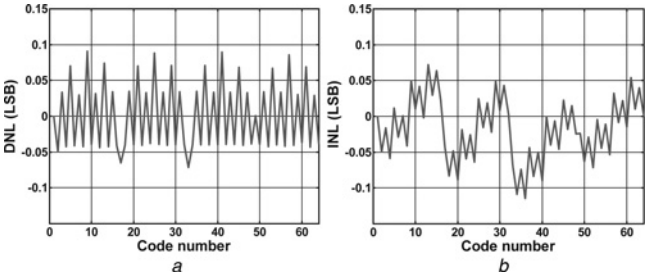

Fig. 11 *Measured DNL and INL profiles against input code numbers*

a DNL profile
b INL profile

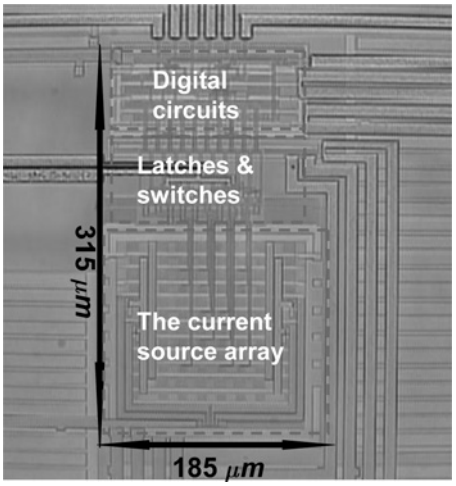

Fig. 10 *Chip microphotograph*

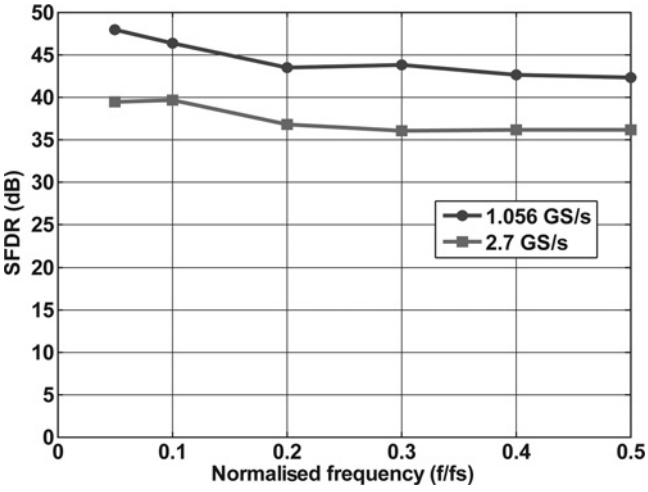

Fig. 12 *Measured SFDR results at 1.056 and 2.7 GS/s*

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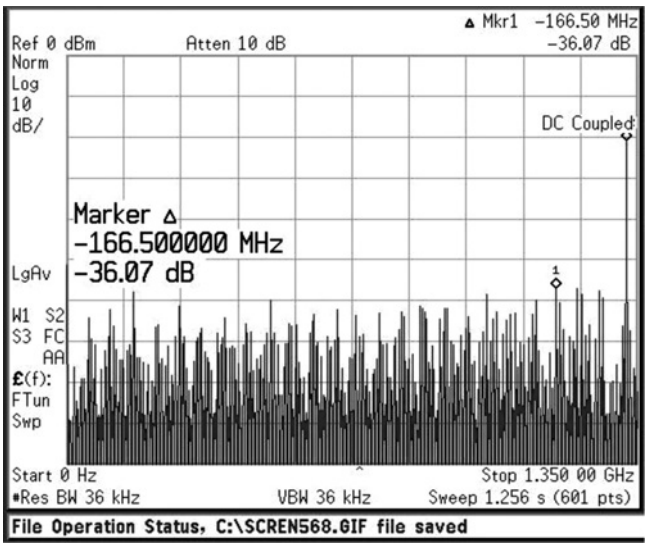

Fig. 13 *Output spectrum with a near-Nyquist signal at 2.7 GS/s*

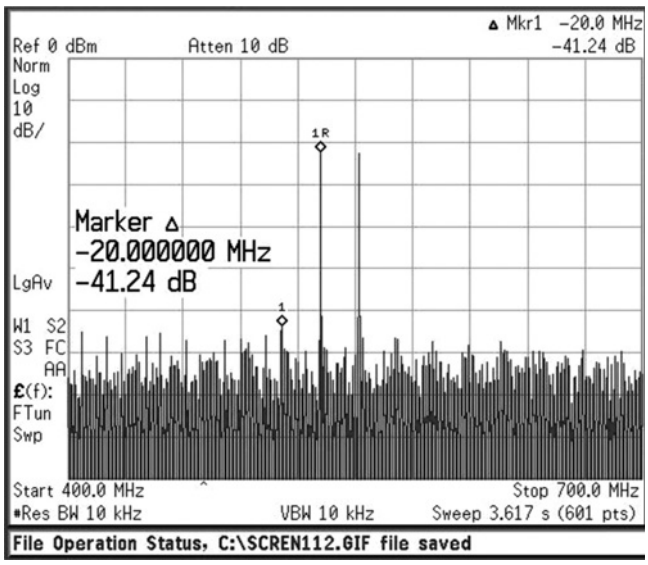

Fig. 14 *Measured output spectrum for a two-tone test with frequencies of 532 and 552 MHz at 2.7 GS/s*

Table 1 Comparison with other published arts

Reference	[1] (++)	[4] (++)	[7] (+)	[8] (++)	[9] (+)	[10] (++)	This work (++)	This work (++)
resolution	6	6	6	6	6	6	6	6
technology	0.13 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	65 nm CMOS	0.13 μm CMOS	0.13 μm CMOS
update rate	3 GS/s	2.7 GS/s	1 GS/s	1.25 GS/s	1.25 GS/s	2.4 GS/s	1.056 GS/s	2.7 GS/s
DNL	NA	0.1 LSB	0.22 LSB	0.06 LSB	<0.1 LSB	0.02 LSB	0.09 LSB	0.09 LSB
INL	0.02 LSB	0.1 LSB	0.48 LSB	0.05 LSB	<0.1 LSB	0.2 LSB	0.11 LSB	0.11 LSB
SFDR	36.2 dB @ 1462 MHz	37 dB @ 520 MHz	35.43 dB (SNDR) @ 5 MHz	48.5 dB @ 300 MHz (1.5 GS/s)	49.4 dB @ 551 MHz	36 dB @ 1.16 GHz	42.3 dB @ 510 MHz	36.07 dB @ 1322 MHz
active area	0.2 mm^2	0.76 mm^2	NA	0.08 mm^2	0.0576 mm^2	0.023 mm^2	0.0585 mm^2	0.0585 mm^2
power	29 mW	28 mW	24 mW	8 mW	6 mW	14 mW	3.2 mW	5.4 mW
FOM (fJ/conv.-step)	150	160	375	100	75	91	47	31

(+) Simulation results, (++) measurement results

Table 2 Comparison with other published arts

Reference	[18] (+)	[19] (++)	[20] (++)	This work (++)	This work (++)
resolution	6	5	5	6	6
technology	0.13 μm CMOS	0.18 μm CMOS	90 nm CMOS	0.13 μm CMOS	0.13 μm CMOS
update rate	5.4 GS/s	1.5 GS/s	2 GS/s	1.056 GS/s	2.7 GS/s
DNL	0.15 LSB	0.05 LSB	0.011 LSB	0.09 LSB	0.09 LSB
INL	0.26 LSB	0.04 LSB	0.008 LSB	0.11 LSB	0.11 LSB
SFDR	38.5 dB @ 1.35 GHz	30.3 dB @ 740 MHz	33 dB @ 980 MHz	42.3 dB @ 510 MHz	36.07 dB @ 1322 MHz
active area	0.01 mm^2	0.19 mm^2	0.375 mm^2	0.0585 mm^2	0.0585 mm^2
power	20 mW	10.4 mW	12 mW	3.2 mW	5.4 mW
FOM (fJ/conv.-step)	58	217	188	47	31

(+) Simulation results, (++) measurement results

specifications, [18–20], in Tables 1 and 2, respectively. In addition, the measurement results of this DAC are also summarised in these tables for comparison purposes. The FOM in [1] is used to assess the performance of DACs as follows

$$\text{FOM} = \frac{\text{POWER}}{2^N \times \text{SampleRate}} \tag{6}$$

where N is the resolution of the DAC. The FOM of this DAC at 1.056 and 2.7 GS/s are less than that in other published arts. The FOM is better at the sampling rate of 2.7 GS/s owing to the almost constant power consumption in the analogue part at different sampling rates and the increasing power dissipation in the digital part at increasing sampling rates. Therefore this DAC exhibits good performance with regard to power consumption and FOM at different sampling rates.

6 Conclusion

A 6-bit DAC with 5.4 mW power consumption and the FOM of 31 fJ/conversion-step at 2.7 GS/s is presented. The measured SFDR results are more than 40 and 36 dB over the Nyquist frequency at 1.056 and 2.7 GS/s, respectively. The '2(T) + 4(B)' segmented architecture combined with the pseudo-thermometer structure is proposed in this work to enhance the DAC's dynamic performance and to achieve a balance between the operating speed of the decoder and the current source cell's area. In addition, the bipolar current source cell and latch clock delay technique are adopted to reduce the power consumption. A compact layout is also accomplished by employing the proposed compact de-glitch latch and the simple centroid switching scheme. This DAC was implemented in a standard 0.13 μm CMOS technology with an active area of 0.0585 mm^2. The measured results show that this DAC satisfies the requirements of both MB-OFDM and DS-CDMA UWB applications very well, and is also suitable for other power-limited WPAN applications.

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