PAPER

A Low-Cost Bit-Error-Rate BIST Circuit for High-Speed ADCs Based on Gray Coding

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SUMMARY Real-time on-chip measurement of bit error rate (BER) for high-speed analog-to-digital converters (ADCs) does not only require expensive multi-port high-speed data acquisition equipment but also enormous post-processing. This paper proposes a low-cost built-in-self-test (BIST) circuit for high-speed ADC BER test. Conventionally, the calculation of BER requires a high-speed adder. The presented method takes the advantages of Gray coding and only needs simple logic circuits for BER evaluation. The prototype of the BIST circuit is fabricated along with a 5-bit high-speed flash ADC in a 90-nm CMOS process. The active area is only $90\,\mu\text{m} \times 70\,\mu\text{m}$ and the average power consumption is around 0.3 mW at 700 MS/s. The measurement of the BIST circuit shows consistent results with the measurement by external data acquisition equipment.

key words: *built-in self-test (BIST), bit error rate (BER), analog-to-digital converter (ADC)*

1. Introduction

Recent integrated chips achieve very high degree integration. Different kinds of blocks such as RF front-end, analog circuit, data converter, digital circuit and memory are placed on the same chip where the test of all the blocks becomes very challenging. Due to a limited pin count, on-chip test is much more economical than external test. Analog-to-digital converters (ADCs) are important interfaces between analog world and tremendous digital processing. An ADC needs many performance parameters to characterize its function and electronic behavior. These parameters can be categorized as static and dynamic ones [1]. Static parameters such as offset, gain error, differential non-linearity (DNL) and integral non-linearity (INL) are related to the transfer function of the ADC under test. On the other hand, dynamic ones like total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), and effective number of bits (ENOB) reveal the signal quality degradation after conversion at different input and sampling frequencies. The test for ADCs has been a significant research topic for a long period [1]–[10]. However, the test for bit error rate (BER) is seldom concerned. BER is an important specification for digital communication systems. BER is also a specification of ADCs. The definition of BER for ADC can be found in the application notes of Analog Devices [11]. In digital communication systems, an incorrect data transmission causes a bit error. In ADCs, an incorrect analog-to-digital conversion causes a bit error. If an ADC is employed in a digital communication system, a wrong conversion causes a wrong data transmission. BER seems to be an optional test term due to its long test time. Recently, digital communication systems such as ADC-based clock data recovery (CDR) and serial link employ ADCs as their key components. Therefore, developing a low-cost and efficient method to test ADC BER is of particular importance for debugging of such communication systems.

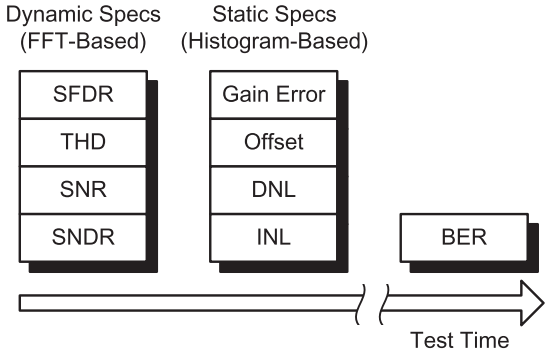

Fig. 1 Test parameters of an ADC and their relative test time.

Figure 1 shows common test parameters for an ADC. Fast Fourier transform (FFT) is a powerful tool for dynamic test. In principle, the FFT test requires at least one sample per code [1]. For an N-bit ADC, at least $0.5\pi \times (2^N - 1)$ samples are necessary for sinusoidal input stimulus. On the other hand, a histogram-based test evaluates static test parameters. A rule of thumb indicates a histogram needs around 10 to 20 samples per code to average noise. Static test with ramp and sinusoidal input stimuli need $10\times(2^N-1)$ and $5\pi \times (2^N - 1)$ samples, respectively.

BER means the total count of conversion errors during the whole test period. An analog-to-digital conversion step with a code distance larger than the predefined limit is a bit error [11], as shown in Fig. 2. In an ADC-based data transmission systems [12], [13], the transmitter transmits multi-level signal through the channel and then a receiver uses ADCs to process the signal. When the clock rate is fixed, multi-level signal transmits more information per unit time. The malfunction of the ADC possibly causes incorrect data transmission. The BER test for an ADC is time consuming. Table 1 shows the BER test time of a 1-GS/s ADC under real time test condition. An ADC with a 10^{-10} BER takes around

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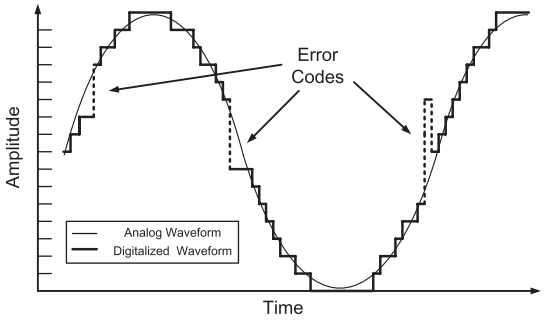


Fig. 2 Error codes in analog-to-digital conversion where dashed lines mean error codes.

Table 1 Bit error rate versus test time for a 1-GS/s ADC.

Bit error rate (BER)	Average time between errors
10^{-8}	0.1 second
10^{-9}	1 second
10^{-10}	10 seconds
10^{-11}	1.67 minutes
10^{-12}	16.7 minutes
10^{-13}	2.78 hours
10^{-14}	1.16 days

10 seconds for data collection, i.e., 10^{10} samples. The test time for BER is much longer than either static or dynamic parameters. Due to the long test time, it is almost impossible to do external BER test for massive products.

For very high-speed ADCs, e.g., GS/s flash ADCs, data collection is difficult. The real time measurement of BER requires high-speed multi-port data acquisition equipment and post data processing. If high-speed data acquisition equipment is not available and thus data are captured at lower speed, the test time will become even longer. This paper proposes a low cost BER built-in-self-test (BIST) circuit based on Gray coding. The circuit utilizes low complexity logic circuits to perform BER evaluation.

The "Low-Cost" is related to external measurement environments but not the circuit implementation. For the typical setup, all the function blocks are instruments or FPGAs. For high-speed ADCs, the requirements for instruments increase. Take the flash ADC implemented in the paper as an example. To measure the BER of a 1-GS/s flash ADC, we need instruments capable of capturing 1-GS/s output data and having sufficient memory for data collection. A 5-bit flash ADC with a 10^{-10} BER needs to collect 500-Gbyte data. Therefore, the typical BER measurement setup is very high-cost. To decrease the cost of high-speed ADC BER test, we propose the BIST circuit to replace the instruments or FPGAs.

The remainder of this paper is organized as follows: Sect. 2 describes the conventional ADC BER test. The principle of Gray coding and the proposed BIST circuit are presented in Sect. 3. Section 4 shows experimental results. Finally, we draw a conclusion in Sect. 5.

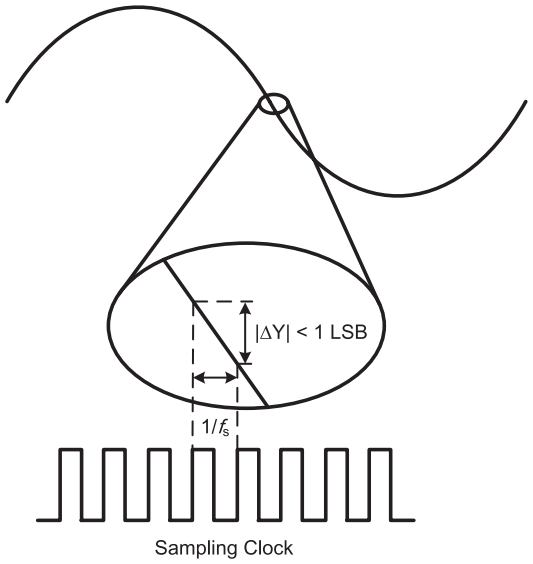


Fig. 3 Relation between sampling clock and low frequency input.

2. Conventional ADC BER Test

ADC BER test can be categorized as foreground type since it has constraints on the amplitude and frequency of the input stimulus. The amplitude variation of the input signal with respect to the sampling speed must be slow enough so the ideal code distance of two consecutive conversions is smaller than the error limit, usually 1 in low-resolution cases.

If the input signal is a dc signal, the ADC output will stay at a certain output code. In normal operation, the input signal is time variant, so the dc test is too optimistic. A periodic input signal with amplitude slightly larger than the input full-scale range is a better alternative because it can explore the entire transfer characteristic of an ADC. The input frequency must be slow enough so at least one sample is taken per code as shown in Fig. 3. Assume the input signal is a full-scale sinusoidal wave with an amplitude of $2^N/2$ where N is the resolution of the ADC under test. When the error limit is 1, the ceiling constraint between input frequency and sampling frequency can be expressed as

$$f_{in} = \left(\frac{f_s}{2^N \pi}\right) \tag{1}$$

where f_{in} is the input frequency and f_s is the sampling frequency [11]. The useful bandwidth of a Nyquist rate ADC is $f_s/2$. Hence, low-frequency input test is too optimistic as well. For a Nyquist rate ADC, if the input frequency and sampling frequency are identical, the output will be the same for each conversion. Hence, a high-frequency input test will be available if the input signal can make the code distance between successive codes smaller than the error limit as shown in Fig. 4. The ratio of the input frequency to sampling frequency can be any natural number. The constraint for high-frequency input signal can be expressed as

$$f_{in} = m \cdot f_s \pm \frac{f_s}{2^N \pi} \tag{2}$$

where m is a natural number. For an aliased sampling case, i.e., $f_{in} > 0.5 f_s$, the frequency information of the input signal is lost after analog-to-digital conversion. In other words, BER test at such high-frequency input seems too pessimistic.

Figure 5 shows the typical setup for BER test of an ADC [11] where two sets of registers record two consecutive output codes each time. An arithmetic circuit determines whether the code distance is larger than the error limit. Finally, an error counter saves the total error count.

There are commercial test machines for single-bit BER test. These machines provide known pseudorandom patterns to the circuit under test (CUT). Then, these machines perform the comparison between the known patterns and output of the CUT. The single-bit BER test only requires an XOR function to tell the difference and a counter to record errors [14]. Besides, indirect test methods estimate BER by observing the eye diagram of received data [15]. On the other hand, the BER test of an ADC is relatively complicated. The code distance of two binary codes can not be determined by simple logic operation. Moreover, commercial ADCs have a wide resolution range. Due to the widely spread resolutions and sampling frequencies, no commercial machines are available. A high-speed field programmable gate array (FPGA) board provides data acquisition and arithmetic processing up to several tens of MS/s. For high-speed data transmission applications, the sampling rate of the ADC may achieve several hundreds of MS/s to several GS/s. An automatic test equipment (ATE) with a high-speed data acquisition interface is expensive for massive product test. Therefore, a low-cost real-time ADC BER BIST circuit is an urgent and a challenging issue.

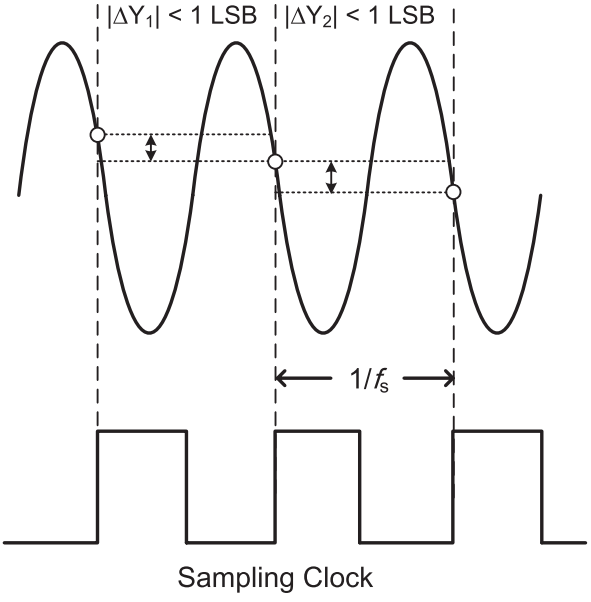


Fig. 4 Relation between sampling clock and high frequency input.

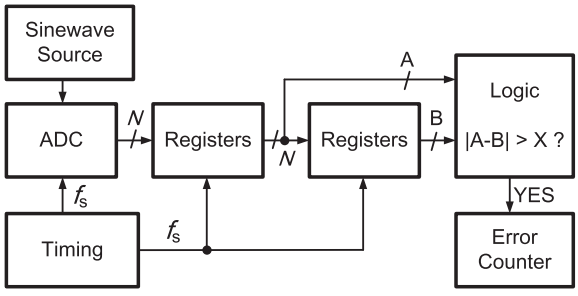


Fig. 5 A conventional setup for BER test.

3. Proposed ADC BER Test

3.1 The Proposed BIST Architecture

Flash ADCs use Gray coding to reduce sparkling errors during analog-to-digital conversion [16]. In an N-bit flash ADC, comparators converts an analog signal to a $(2^N - 1)$-bit thermometer code. To reduce the output pin count, a thermometer code must be converted to a coding style with fewer bits. Usually, a thermometer code is converted to a Gray code first instead of a binary code. Gray code is also called as reflected binary code where two successive values differ in only one bit. For some cases, one bit error of a binary code is much more serious than that of a Gray code. Take a 3-bit code as an example. The code distance of 010 and 110 in Gray code is 1, and the code distance in binary code is 4. Table 2 shows a 3-bit lookup table of decimal, binary and Gray codes. This work takes the advantages of Gray code to perform high-speed BER evaluation.

Figure 6 depicts the block diagram of the proposed BIST circuit. This BIST circuit consists of two sets of registers, a programmable clock divider, a comparison circuit, a decision circuit and a parallel-to-serial circuit. The registers triggered by a programmable clock store two successive Gray output codes. The programmable divider provides divided clocks like $f_s/2$, $f_s/4$, $f_s/8$ for high-input frequency BER test. The value of BER depends on the sampling speed, input frequency, input amplitude, etc. For dc or low frequency input signals, the measured BER is overoptimistic. On the contrary, BER test obeying (2) is too pessimistic. With the divided clocks, the BIST architecture can perform BER test at input frequencies within the range of dc to $f_s/2$. If the sampling frequency of the ADC is f_s and the output data are captured at $f_s/4$, the output bandwidth (or sampling

Table 2 Binary and gray coding.

Decimal	Binary code	Gray code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

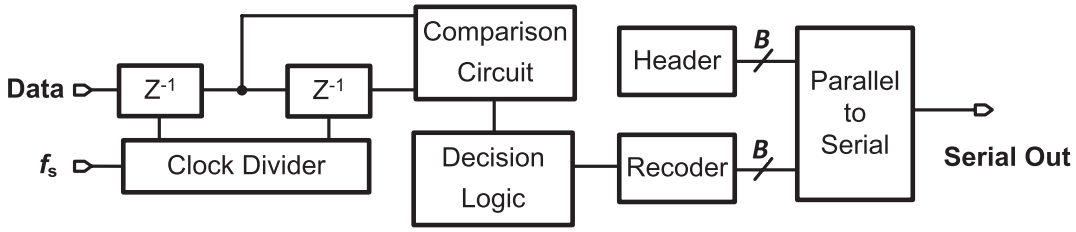


Fig. 6 The simplified block diagram of the proposed BIST circuit.

speed) will be equivalently reduced by a factor of 4. In other words, the ADC can perform BER test at $f_s/4$ or $2f_s/4$. If the division ratio is 8, the input frequency can be around $f_s/8$, $2f_s/8$, or $3f_s/8$. Eq. (2) can be rewritten as

$$f_{in} = \frac{m}{d} \cdot f_s \pm \frac{f_s}{2^N \pi d} \tag{3}$$

where d is the clock division ratio.

The comparison circuit determines if the code distance of the two successive codes is within the limit. Then, following decision logic decides to idle or increase the error counter. Conventional comparison circuit requires an adder which is often the speed bottleneck. To output the test result, this BIST architecture utilizes a parallel-to-serial circuit to reduce the pin count.

3.2 BIST Circuit Based on Binary Coding

If the output of an ADC is binary, an arithmetic circuit will be necessary to calculate the code distance of two successive codes. Figure 7 depicts a possible BIST circuit based on binary coding. A set of registers store the binary inversion of the previous code. For an N-bit ADC, an $(N+1)$-bit adder adds the current output code to the inversed code. Then, the adder adds 1 to the result to complete a two's-complement addition. For a correct conversion, there are only three possible code distances: -1, 0, 1. As shown in Fig. 7, an $(N+1)$-input OR gate (part A) detects if the code distance is 0. An $(N+1)$-input NAND gate (part B) tells if the distance is -1. Part C distinguishes if the distance is 1. If none of them triggers the bottom OR gate, the error count will increase by 1. The main speed bottleneck is the adder. For high-resolution cases, the issue becomes more serious. For low-resolution cases, ripple carry adder has sufficient speed. For high-resolution ADCs, high-speed adders like carry-lookahead or carry-select architectures should be put into consideration [17]. In general, BER test is a preferred test term for low-resolution high-speed ADCs. For a 5-bit case (6-bit adder), the critical path is 5 carry ripple delays plus 1 sum delay. If a 9-NAND full adder is used, totally 16 NAND gate delays will be consumed.

3.3 BIST Circuit Based on Gray Coding

If the output is Gray code, simple logic operation will be sufficient for BER test. For a flash ADC, we can directly use its Gray-coded output. For binary-coded ADCs such as

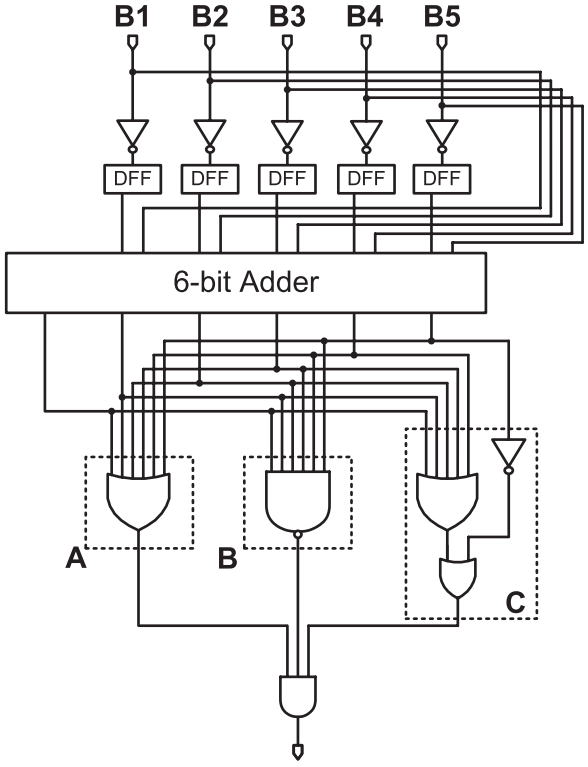


Fig. 7 BIST circuit based on binary coding.

pipelined and SAR ADCs, simple logic operation converts binary codes to Gray codes as depicted in Fig. 8. Figure 9 shows the logic implementation of the proposed BIST circuit and Fig. 10 depicts its flow chart. This BIST circuit also uses three parts to verify the difference of two consecutive codes. The current output code of this ADC is called as Code X and the previous one is called as Code $X-1$. The BIST circuit uses XOR gates to determine the difference of two codes. Part A detects if all the outputs of the XOR gates are 0. If the output of part A is 1, the two codes are identical. In this case, the error counter idles. If the two codes are different, part B will detect where is only one-bit difference. If part B finds more than one difference, the error count will increase by 1. If there is only one-bit difference, part C will determine if the code distance is 1. Part C uses the current Gray code to find a corresponding verification code. The XOR result of Code X and $X-1$ are compared to the verification code. If the result shows the code distance is not 1, the error count will increase by 1. Table 3 shows how to find

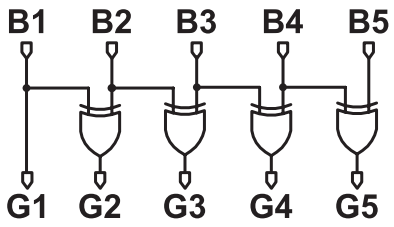


Fig. 8 5-bit binary-to-Gray conversion.

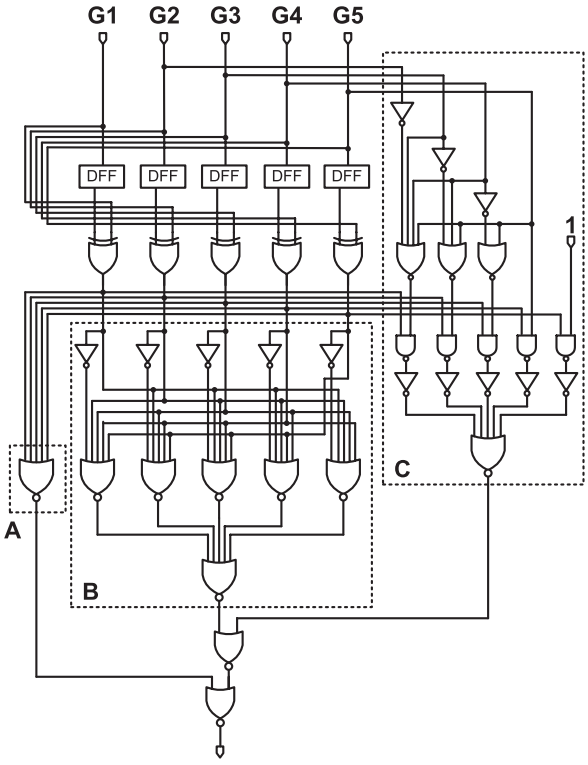


Fig. 9 BIST circuit based on Gray coding.

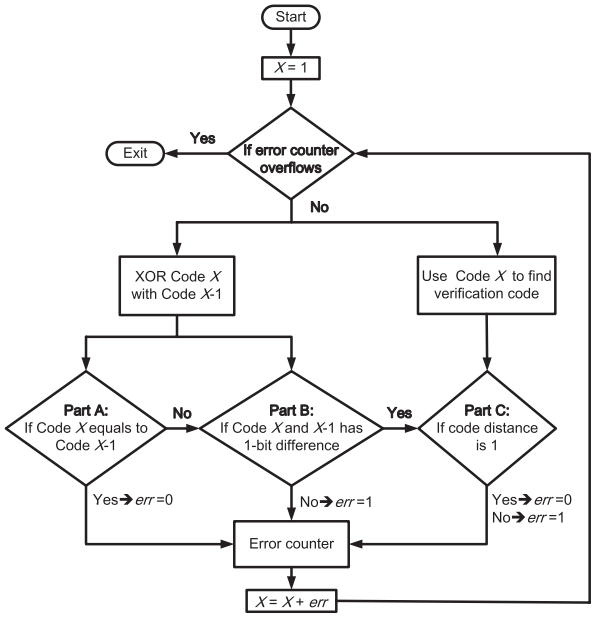


Fig. 10 Flow chart of the BIST circuit.

Table 3 How to find the verification code.

Binary code	Gray code	XOR with the previous code	XOR with the next code	Verification code
000	000	—	001	001
001	001	**001**	**010**	**011**
010	011	**010**	**001**	**011**
011	010	001	100	101
100	110	100	001	101
101	111	**001**	**010**	**011**
110	101	**010**	**001**	**011**
111	100	001	—	001

the verification code based on the current Gray code. For an output code with a decimal value i, there are only three correct values: i, i+1, and $i-1$. Part A handles the identical case, and hence the verification codes do not consider it. To build the lookup table, we perform XOR function between Gray code i and its previous code $i-1$ and next code i+1, and the results are $j-1$ and j+1, respectively. Then, the XOR result of $j-1$ and j+1 is the verification code. A 3-bit verification code $V_1V_2V_3$ for a Gray code $G_1G_2G_3$ can be expressed as

$$\begin{aligned} V_3 &= 1 \\ V_2 &= G_3 \\ V_1 &= G_2 \cdot \overline{G_3} \end{aligned} \tag{4}$$

Eq. (4) can be extended to a Y-bit general form as

$$\begin{aligned} V_Y &= 1 \\ V_{Y-1} &= G_Y \\ V_{Y-2} &= G_{Y-1} \cdot \overline{G_Y} \\ V_{Y-3} &= G_{Y-2} \cdot \overline{G_{Y-1}} \cdot \overline{G_Y} \\ &\vdots \\ V_1 &= G_2 \cdot \overline{G_3} \ldots \overline{G_{Y-3}} \cdot \overline{G_{Y-2}} \cdot \overline{G_{Y-1}} \cdot \overline{G_Y} \end{aligned} \tag{5}$$

In the binary-based design, the decision steps are performed after the adder output is available. The proposed work uses parallel decision steps. When part A and B perform logic function, part C evaluates the verification code simultaneously. Hence, the critical path of the proposed decision circuit is shorter than the binary-based design. In Fig. 9, the critical path delay is through 8 gates (including 1 NAND gate, 5 NOR gates and 2 INV gates), and the area includes about 60 NAND gates if we use a 9-NAND full adder. On the other hand, the area of the BIST circuit based on gray coding is about 22 NAND gates. Because of fewer gates and the shorter critical path, the BIST circuit of gray-code design has higher operation speed and smaller area than the binary design. The operation speed of gray-code design is about two times faster than the binary design.

3.4 Parallel-to-Serial Circuit and Clock Divider

Figure 11 shows the timing and block diagrams of the parallel-to-serial circuit. It converts parallel ADC outputs into a 1-bit stream. To simplify data acquisition, the bit

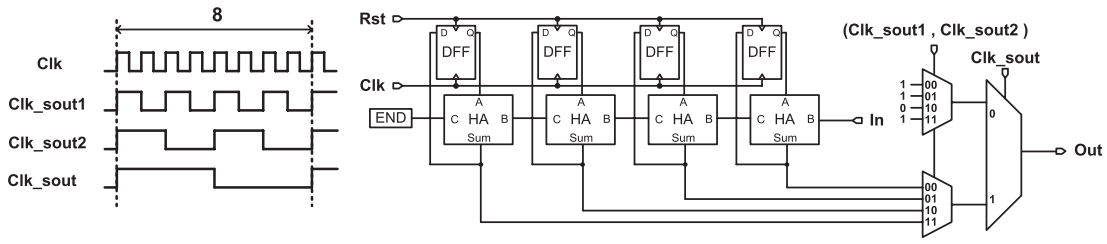


Fig. 11 The timing and block diagrams of the parallel-to-serial circuit.

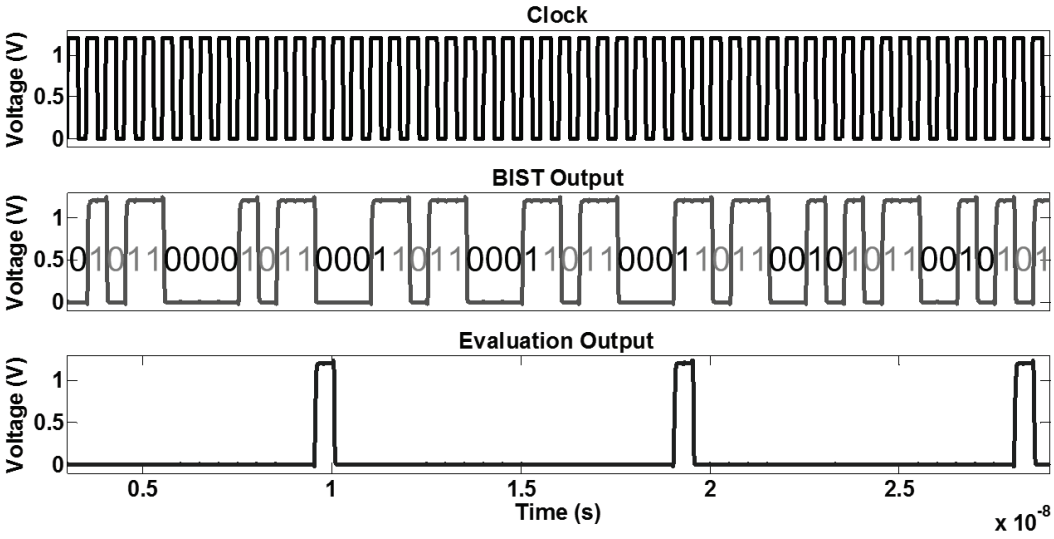


Fig. 12 Transient simulation waveforms where gray number are headers and black ones are error records.

stream composed of 4-bit headers, 1011, and 4-bit data. However, it is hard to tell the error information in the 1-bit stream without any sign or mark. The serial output needs a reference. The header is inserted between each 4-bit data for data recognition. The width of the headers and data depends on the applications. Figure 12 shows a transient simulation result where the BIST output waveform contains the information of headers (gray numbers) and error records (black numbers). A rise of the signal 'evaluation output' means a bit error. The error record updates every 8 cycles.

4. Experimental Results

A proof-of-concept prototype is fabricated in a 90-nm CMOS process with a 5-bit high-speed flash ADC. Figure 13 shows the micrographs of the whole chip and zoomed core view where the BIST circuit only occupies a small active area, $90\,\mu\text{m} \times 70\,\mu\text{m}$. When the flash ADC operates at 700-MS/s, the average power consumption of the BIST circuit is only 0.3 mW. Due to the parallel-to-serial circuit, the BIST circuit only need two additional pins, a reset pin and a serial data output. The chip is directly mounted on a PCB and connected to instruments via bonding wires. Figure 14 depicts the test setup. An RF signal generator Anritsu MG3642A with a minimum output frequency of 125 kHz serves as the input source. A pattern generator

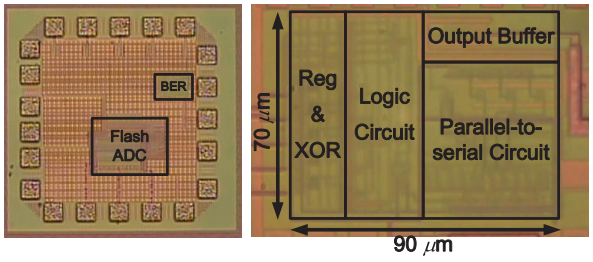


Fig. 13 Full chip micrograph (left) and zoomed core view (right).

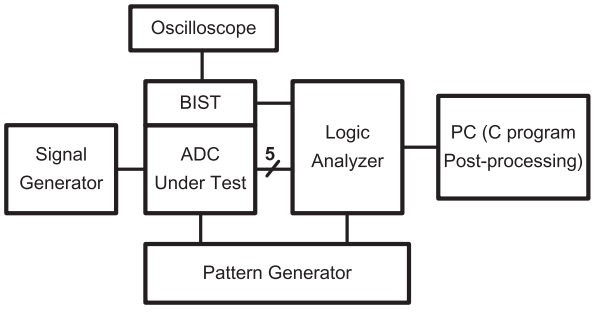


Fig. 14 Measurement setup for BIST and external test.

Agilent 81250 produces clock signal for the ADC and divided clocks for the BIST circuit and logic analyzer. Due to

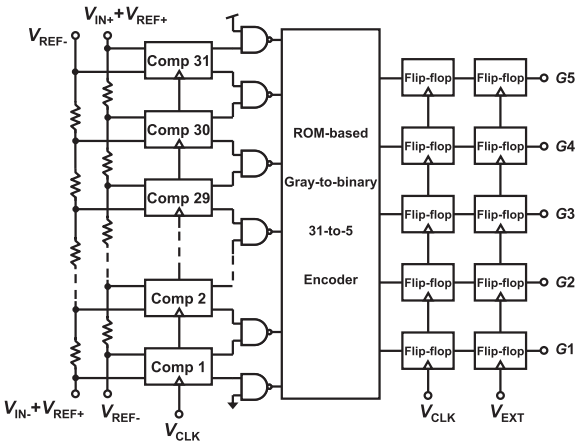


Fig. 15 Block diagram of the 5-bit flash ADC.

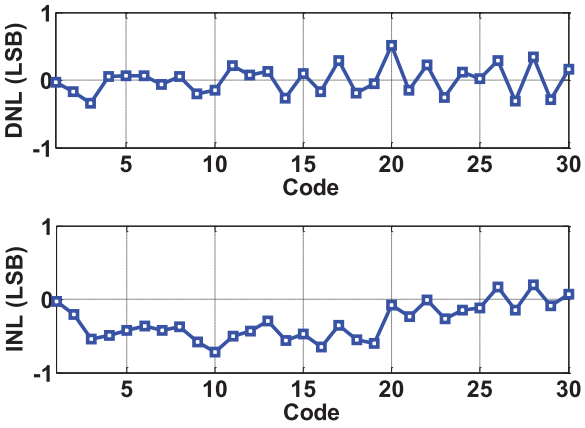


Fig. 16 Measured DNL and INL of the flash ADC.

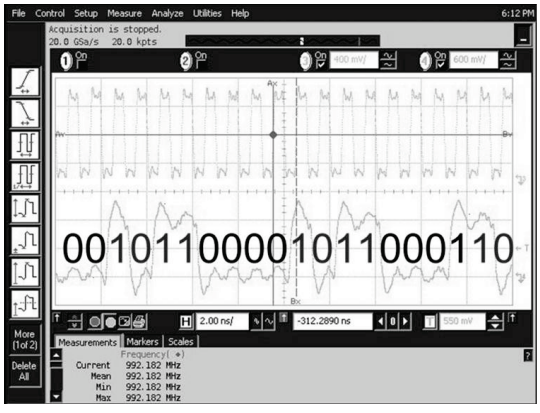
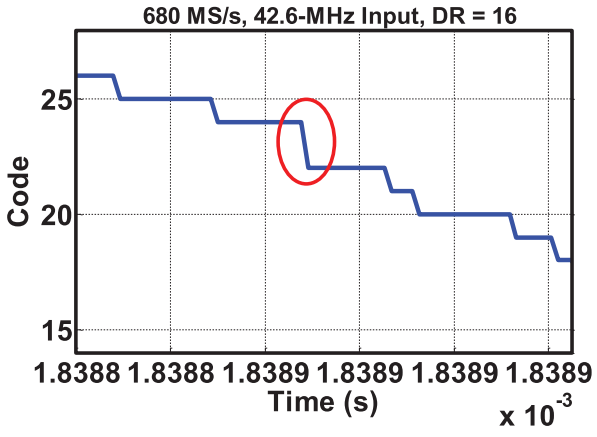


Fig. 17 Measured BIST output waveform at 1 GS/s.



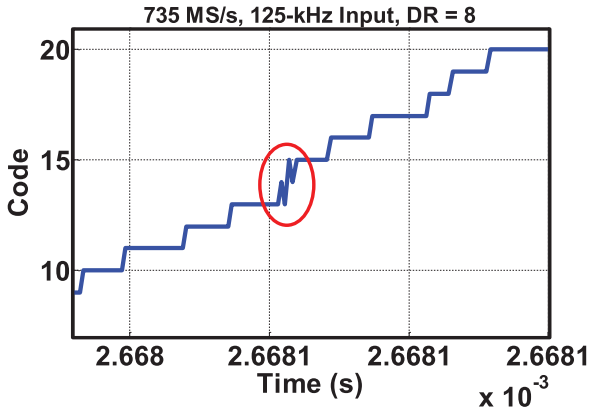


Fig. 18 Two measured error code cases (DR is clock division ratio).

the pattern generator, the prototype does not contain a programmable clock divider. The BIST output can be observed either via oscilloscope or logic analyzer. Before BER test, we tested the linearity of the flash ADC. The architecture of the flash ADC is shown in Fig. 15 where thermometer codes are converted to Gray codes [18]. V_{CLK} is the sampling clock and V_{EXT} is the divided clock. According to DNL and INL charts in Fig. 16, the ADC does not have missing code. Therefore, the ADC is suitable for BER test.

Figure 17 shows a measured BER output waveform at 1 GS/s. The gray numbers '1011' mean the headers and black numbers are the error records, respectively. The waveform is very sharp even at 1-GS/s operation. To verify the correctness of the BIST circuit, a logic analyzer Agilent 16903A captures the output codes of the flash ADC simultaneously. By comparing the BIST output and the BER derived from captured output data, we can verify the proposed BIST circuit. The employed oscilloscope Agilent 54855A has 7-GHz input bandwidth while the logic analyzer only has 200-MHz data bandwidth. Therefore, the comparison of the BIST circuit and external data acquisition equipment must be done at low speed. When the flash ADC operates at high sampling rate, the external sampling frequency must be a lower value, 1/8 or 1/16 of the ADC sampling rate. By reconstructing output data captured by the logic analyzer, Fig. 18 shows two cases of incorrect analog-to-digital conversion. These errors are elusive and difficultly found by other test terms. Table 4 lists 8 measurement cases to verify the BIST circuit. For each case, 4.2 millions of samples are captured. These cases are measured at 735 MS/s and 125-kHz input signal. The selection of the sampling frequency is

Table 4 Test results of BIST circuit and logic analyzer.

	1/8 f_s			1/16 f_s	
	Logic Analyzer	**BIST**		**Logic Analyzer**	**BIST**
Case 1	198	198	**Case 5**	19	19
Case 2	35	35	**Case 6**	93	93
Case 3	150	150	**Case 7**	63	63
Case 4	101	101	**Case 8**	50	50

based on the error count. For low sampling frequency, e.g., lower than 700 MS/s, bit errors are too few to be found. For high input frequency, e.g., higher than 800 MS/s, bit errors happen too frequently. Because the BIST circuit is digital, the error counts calculated by the BIST circuit and the logic analyzer should be the same. This table shows the BIST circuit has completely identical measurement results with the logic analyzer.

According to the experimental results, the proposed BIST circuit shows the same accuracy as external data acquisition equipment. Moreover, the BIST circuit can perform at-speed BER test and therefore has the advantage of short test time. Owing to the limited memory depth, the employed logic analyzer only collects around 4 million samples each time. At 600 MS/s, only data of 2/3 second are collected. The time consumed for loading the data to a personal computer and post data processing take at least 3 minutes. Hence, the ratio between post-processing time and practical chip running time is at least 270. This statement shows the inefficiency of external BER test. As shown in Table 1 for a BER of 10^{-10}, the real time measurement requires 10 seconds. Using a logic analyzer, the total measurement time for one bit error is around 4 minutes, an unaffordable value for massive test. This case highlights the importance of the proposed circuit. The proposed circuit achieves at-speed test including data processing and decision making.

5. Conclusion

This paper presents a reliable, high-speed, low-power BIST circuit for at-speed ADC BER test. Based on Gray coding, simple logic circuit can perform fast BER test. The silicon prototype is demonstrated with a high-speed Gray-coded flash ADC. Experimental results show the consistence between BIST and external test results. The full BIST scheme of the ADC BER test does not require any external equipment. Compared to the conventional test scheme, the proposed BER test has more flexibility in the selection of input frequency. With simple binary-to-Gray conversion, this BER test is also feasible for all binary-coded ADCs. The on-chip circuit reduces test time by two orders than external solutions. To the best of the authors' knowledge, the proposed circuit is the first silicon prototype of ADC BER BIST.

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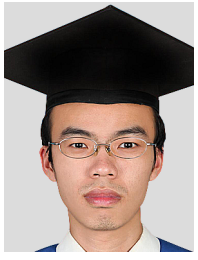

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