PAPER

A Third-Order Low-Distortion Delta-Sigma Modulator with Opamp Sharing and Relaxed Feedback Path Timing

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SUMMARY This paper proposes a third-order low-distortion delta-sigma modulator (DSM). The third-order noise shaping is achieved by a single opamp (excluding the quantizer). In the proposed DSM structure, the timing limitation on the quantizer and dynamic element matching (DEM) logic in a conventional low-distortion structure can be relaxed from a non-overlapping interval to half of the clock period. A cyclic analog-to-digital converter with a loading-free technique is utilized as a quantizer, which shares an opamp with the active adder. The signal transfer function (STF) is preserved as unity, which means that the integrators process only the quantization noise component. As a result, the opamp used for the integrators has lower requirements, as low-distortion DSMs, on slew rate, output swing, and power consumption. The proposed third-order DSM with a 4-bit cyclic-type quantizer is implemented in a 90-nm CMOS process. Under a sampling rate of 80 MHz and oversampling ratio of 16, simulation results show that an 81.97-dB signal-to-noise and distortion ratio and an 80-dB dynamic range are achieved with 4.17-mW total power consumption. The resulting figure of merit (FOM) is 81.5 fJ/conversion-step.

key words: *delta-sigma modulator, DSM, opamp sharing, relaxed dynamic element matching (DEM) timing*

1. Introduction

With development in wireless communication, the required resolution and bandwidth for analog-to-digital converters (ADCs) has increased. Delta-sigma modulators (DSMs), which are conventionally suitable for high-resolution applications, are being developed to have wider bandwidth. Thus, DSMs are becoming increasingly employed for wireless communication applications [1]–[5]. The signal-to-noise and distortion ratio (SNDR) is proportional to the oversampling ratio (OSR). To increase bandwidth for a given SNDR, a lower OSR is necessary and either a higher-order DSM architecture or a multi-bit quantizer should be manipulated. Since stability is a challenging issue for higher-order DSM architectures, a multi-bit quantizer is used in this study to increase bandwidth.

In single-loop DSMs, two kinds of structure, namely feedback and low-distortion structures, are commonly employed. For a feedback structure, the integrated signal in the loop filter includes the input signal and quantization noise, which induces high requirements on slew rate and output swing of the opamp. For a low-distortion structure [6], only quantization noise in the loop filter is processed, giving it higher linearity and making it suitable for a low power supply voltage. However, the quantization and dynamic element matching (DEM) operations are confined within the non-overlapping clock interval. Such a problem will deteriorate sharply as the resolution of the quantizer or the sampling rate increases. An architecture with a half-delay integrator has been proposed to relax this timing limitation to half a clock cycle [4]. This eases the quantizer design and relieves the bottleneck of DEM operation speed.

In a DSM, the opamp consumes most of power. Several studies were proposed to reduce the number of opamps without sacrificing their higher-order noise shaping ability. In [5] and [7], a second-order noise shaping function was achieved by using a single opamp combined with additional signal transfer paths, but the feedback factor was reduced. To retain a given settling accuracy within a specified period, the requirement on bandwidth of the opamp, and consequently the power consumption, has to be increased. This work proposes a low-distortion third-order DSM that uses only a single opamp (excluding the quantizer). Considering the thermal noise constraint, sharing the opamp of the first integrator with the second integrator is inefficient because the required capacitor size for the second integrator is smaller than the first one. In the proposed DSM, the second integrator is a double integrator and shares the opamp with the first integrator. In this way, although the feedback factor of the second integrator is lower than that of the first one, the speed requirements of the opamp for these two integrators are similar. The opamp can thus be utilized efficiently in terms of power consumption. Besides, a manipulative timing arrangement is presented based on the proposed architecture to relax the feedback path timing.

The rest of this paper is organized as follows. A brief review of low-distortion structures is given in Sect. 2. The proposed third-order DSM structure is presented in Sect. 3. Sect. 4 discusses the design issues of the proposed DSM. Simulation results are shown in Sect. 5 to demonstrate the effectiveness of the proposed design. Finally, conclusions are drawn in Sect. 6.

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2. Review of Low-Distortion Delta-Sigma Modulator Structures

2.1 Conventional Low-Distortion Structure

Figure 1(a) shows the signal flow diagram of a conventional low-distortion DSM [6], which can be realized by the circuit shown in Fig. 1(b), and its corresponding timing diagram is shown in Fig. 1(c). In all figures of this paper, the subscript "d" indicates that the falling edge is slightly delayed. C_{fwj} represents the feedforward capacitors from the input or integrator outputs, C_{sj} represents the sampling capacitors of the integrators, and C_{fj} represents the feedback capacitors in the stage j. The sampling capacitor of the first integrator (C_{s1}) samples the input signal during Φ_1. Then, the sampled input signal is integrated on the feedback capacitor (C_{f1}) during Φ_2. The output signal of this integrator is held in the next Φ_1 and simultaneously sampled on the sampling capacitor of the second integrator (C_{s2}). The operation of the second integrator is the same as that in the first stage. After the integration of the second integrator, the signals from the feedforward paths are summed in Φ_1. Note that the quantization and DEM operations must be completed within the non-overlapping interval (i.e., between Φ_1 and Φ_2) since the first integrator has to carry out its integration during Φ_2. The structure requires an extra adder to sum all feedforward signals from the modulator input and the integrators output. This limited operating interval for quantization and DEM operations is a challenging issue for high speed applications.

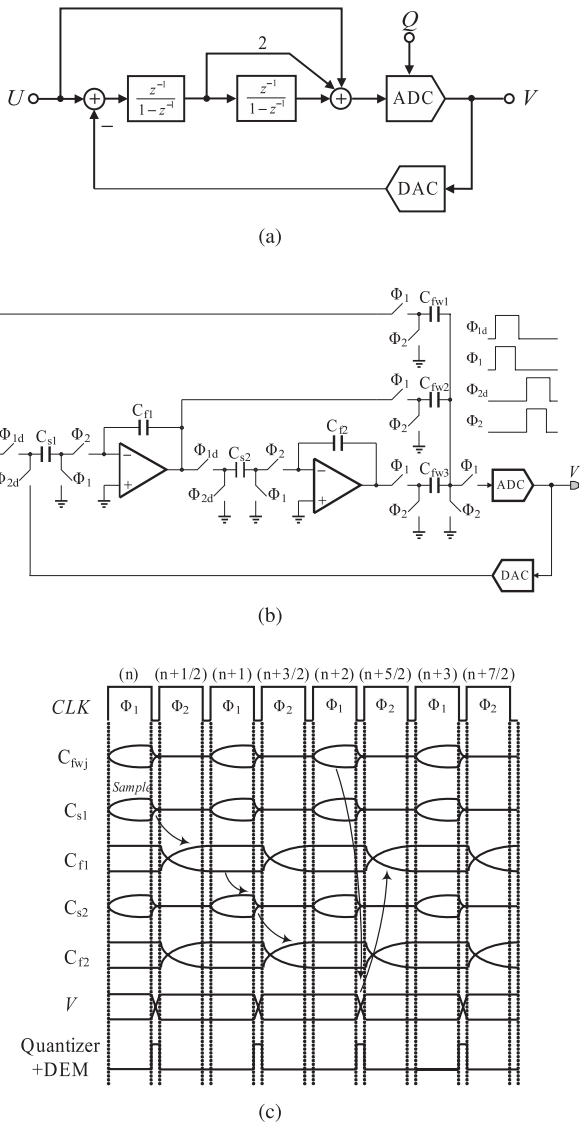

Fig. 1 Conventional low-distortion structure: (a) block diagram, (b) circuit schematic, and (c) timing diagram.

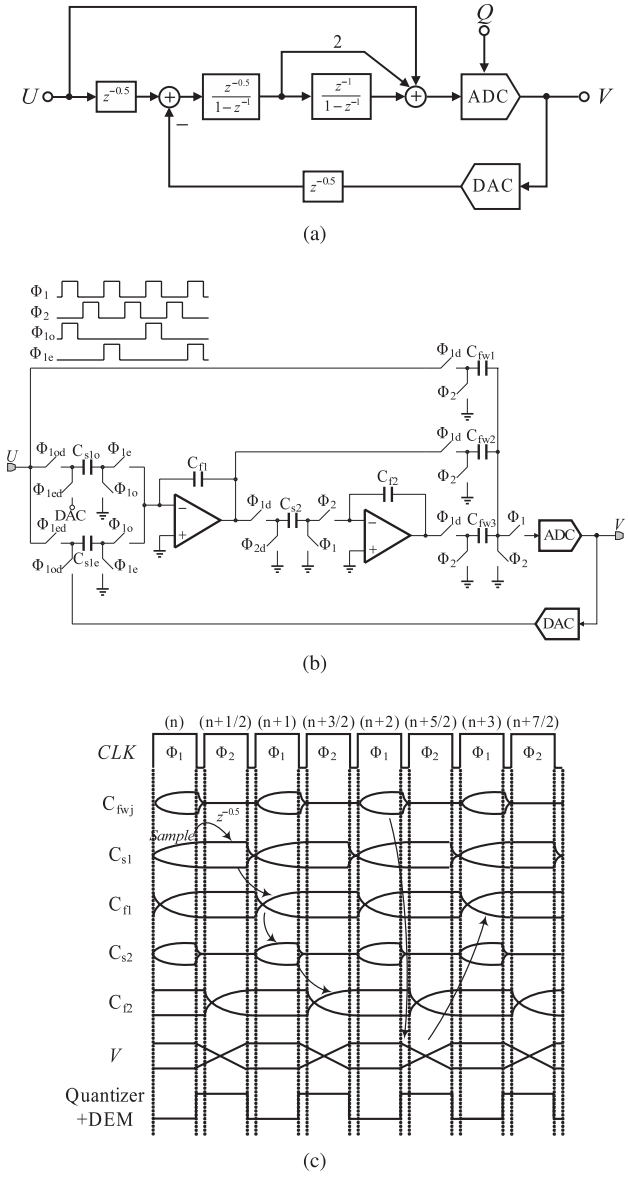

Fig. 2 Low-distortion structure with half of a clock period for feedback timing: (a) block diagram, (b) circuit schematic, and (c) timing diagram.

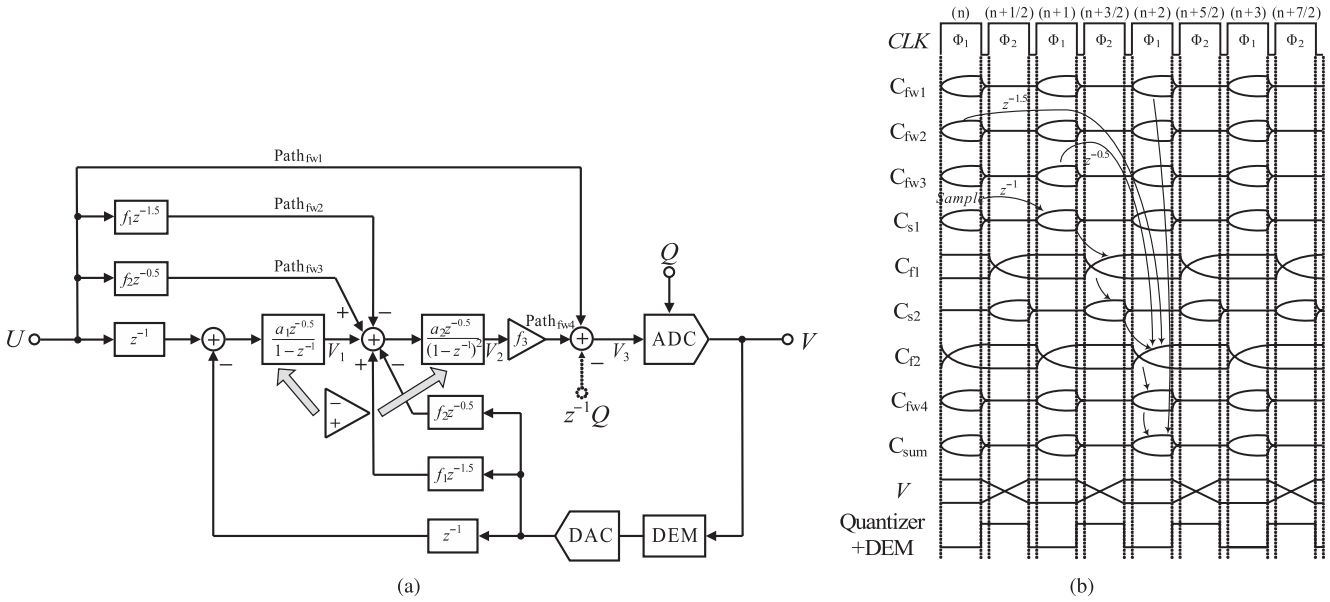

Fig. 3 Proposed third-order low-distortion DSM with opamp sharing and relaxed feedback path timing: (a) block diagram and (b) timing diagram.

2.2 Low-Distortion Structure with Half Clock Period for Feedback Timing

In the structure of Fig. 2(a), the quantization and DEM operations can be extended to half of a clock period by inserting a half delay into the input sampling path and feedback path [4]. Figures 2(b) and 2(c) show the circuit schematic and the timing diagram of the DSM, respectively. Similar to conventional low-distortion DSM, this structure also requires an adder to sum all feedforward signals.

3. Proposed DSM Architecture

3.1 Block Diagram, Timing Diagram, and Transfer Function

Figure 3(a) shows the proposed DSM architecture with coefficients $a_1 = 1$, $a_2 = 1$, $f_1 = 1$, $f_2 = 3$, and $f_3 = 1$. For reducing the output swing of integrators, the coefficients are set to $a_1 = 1$, $a_2 = 1/2$, $f_1 = 1$, $f_2 = 3$, and $f_3 = 2$. Both the input signal and the digital-to-analog converter (DAC) output signal are delayed by a full clock cycle before entering the first half-delay integrator. The second integrator is a half-delay double integrator. To retain the unity gain for the signal transfer function (STF) and to maintain the feature of low distortion, two half-delay branches and two one-and-a-half-delay branches are all summed in front of the second integrator; i.e., two delayed input-feedforward paths and two delayed feedback paths from the input and DAC are added in front of the second integrator. Accordingly, the STF and noise transfer function (NTF) of the proposed DSM without the noise-coupling path, $z^{-1}Q$, are:

$$STF(z) = \frac{V(z)}{U(z)} = 1 \tag{1}$$

$$NTF(z) = \frac{V(z)}{Q(z)} = (1 - z^{-1})^3 \tag{2}$$

The STF is unity, as in conventional low-distortion DSMs [6]. The NTF manifests a third-order noise shaping characteristic, but just two integrators are used. The signals at the integrators output and the quantizer input are:

$$V_1 = -a_1 z^{-1.5}(1 - z^{-1})^2 Q = -z^{-1.5}(1 - z^{-1})^2 Q \tag{3}$$

$$V_2 = (NTF - 1)Q/f_3 = (-3z^{-1} + 3z^{-2} - z^{-3})Q/2 \tag{4}$$

$$V_3 = U + V_2 f_3 = U + (-3z^{-1} + 3z^{-2} - z^{-3})Q \tag{5}$$

The timing diagram of the proposed DSM is shown in Fig. 3(b). C_{fw1}, C_{fw2}, and C_{fw3} represent the capacitors of the feedforward paths from the input, and C_{fw4} represents the capacitor of the feedforward path from the output of the second integrator. C_{sj} represents the sampling capacitors of the integrators, C_{fj} represents the integrating capacitor in the stage j, and C_{sum} represents the feedback capacitor of the active adder. The input signal is first sampled on C_{s1}, and then held until the end of the next Φ_1. During Φ_2, the sampled signal is integrated on C_{f1}. At the same time, the output of the first integrator is sampled on C_{s2}. The signal on C_{s2} and the signals on the feedforward and feedback branches are transferred to C_{f2} in the following Φ_1. Simultaneously, the active adder sums the feedforward signals from the modulator input and the output of the second integrator. The quantization and DEM operation are extended to half a clock period since the second integrator is active during Φ_1. With the extended timing budget, the difficulty in designing the quantizer is greatly reduced and various ADC types for the quantizer can be chosen.

From Eq. (3) and Eq. (4), in the worst case, the output

swing of the second integrator must be extended to sustain seven times the quantization noise. In order to decrease the output swing, the second integrator gain is set to 1/2, which is compensated by a 2 times gain of the feedforward path. The reduced output swing enables the usage of a power-efficient single-stage amplifier.

3.2 Opamp Sharing

In the proposed structure, opamp sharing is utilized since the two integrators are active in different phases. Therefore, third-order noise shaping can be achieved by using a single opamp if the adder in the quantizer input is realized by passive devices. The capacitor size in the second integrator can be scaled down because its thermal noise is shaped by first integrator, whose inputs thermal noise is suppressed by the OSR [8], [9]. For the same reason, the speed specification of the opamp in the second integrator is lower than that of the one in the first integrator [10]. Therefore, the opamp performance is adequately exploited by the two integrators since the increased requirements on opamp performance resulted from the smaller feedback factor of the second integrator is compromised by its reduced capacitive loading due to lower thermal noise contribution. However, the requirements on opamp performance for the second integrator may exceed those for the first integrator because the scaling factor for the latter stage is limited by the minimum unit capacitor concerning process matching. The circuit area of the proposed DSM does not greatly increase since the capacitors behind the first integrator are much smaller than those in the first integrator and the path of $f_1 z^{-1.5}$ ($f_2 z^{-0.5}$) from the modulator input and the path of $f_1 z^{-1.5}$ ($f_2 z^{-0.5}$) from the DAC output can share a switched-capacitor (SC) circuit although more paths are summed in the front of the second integrator. In this design, $C_{s1} = 16C_{s1\_u}$ is 1.2 pF due to the 4-bit DAC and C_{s2} is 0.16 pF.

The power reduction of the proposed circuit decreases with increasing operation frequency. When an opamp is shared between the first and second integrators, more switches are connected to the opamp input than there would be no opamp sharing. This results in more switches junction capacitance and routing parasitic capacitance at the opamp input. Hence, the feedback factor (β) is decreased. In an opamp-based closed-loop circuit, $\omega_{-3\,\mathrm{dB}}$ can be expressed as:

$$\omega_{-3\,\mathrm{dB}} = \beta\omega_{\mathrm{T}} = \beta\frac{g_m}{C_{\mathrm{L}}} \tag{6}$$

where ω_{T} is the open-loop unit-gain bandwidth and C_{L} is the equivalent load capacitance. To maintain a given $\omega_{-3\,\mathrm{dB}}$, g_m should be increased if the feedback factor decreases. The g_m value is proportional to the tail current of the opamp, so increasing it increases power consumption. The effect in first integrator is less than that in the second integrator because capacitors with smaller values are used in the second integrator. If the operation frequency is increased, to keep a given time constant (which is the product of the on resistance of the switches and the capacitance), the switches have to be widened. Wider switches come with the larger junction capacitance and the routing parasitic capacitance at the opamp input. Here, the junction capacitance of the off switches at the opamp input and the routing parasitic capacitance are lumped into the extra parasitic capacitance C_{p_extra}, which diminishes the feedback factor. The increase of C_{p_extra} is proportional to the increase in operation speed. Fortunately, the extra capacitance is not too large to seriously degrade the feedback factor although it increases with operation frequency. In this design, the feedback factor of the second integrator only decreases by 7 percent, i.e., the opamp power requirement increases by 7 percent, compared to that of the second integrator without opamp sharing. Consequently, as the operation frequency accelerates, the growing C_{p_extra} slightly increases power consumption. Under an 80-MHz sampling frequency this effect is minor, and the power saving advantage in the proposed opamp sharing topology is still preserved.

The adder in front of the quantizer can be either active or passive. For the passive type, the input range of the quantizer is attenuated. The reduction depends on the number of summing paths and their total capacitance. As the number of summing paths increases, the attenuation becomes more significant and the least significant bit (LSB) of the quantizer has a corresponding reduction. Under this condition, both the accuracy requirement and the design complexity for the comparator are increased for a flash-type quantizer. Nevertheless, this increase is tolerable since there are only two paths at the quantizer input in the proposed DSM architecture. For an active-type adder, the cost is the increased power consumption. However, due to the relaxed feedback path timing, the quantizer can adopt a cyclic ADC or a pipelined ADC, which can share an opamp with the active adder in the circuit implementation. Moreover, using an active adder makes it easier to employ a noise coupling technique for the DSM [11]–[15] to increase the order of the NTF without additional opamps.

4. Design Considerations

4.1 Double Integrator

In a conventional DSM, an M-order DSM generally requires at least M opamps. A double integrator [7], which is equivalent to one integrator cascading another, can be used to reduce the number of opamps. Figure 4 shows the architecture of a double integrator. Based on this concept, Fig. 5 shows

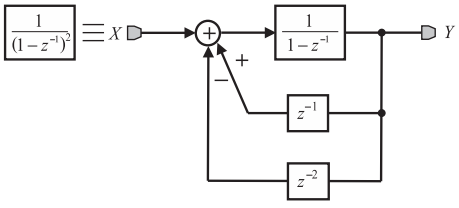

Fig. 4 Conventional double integrator architecture.

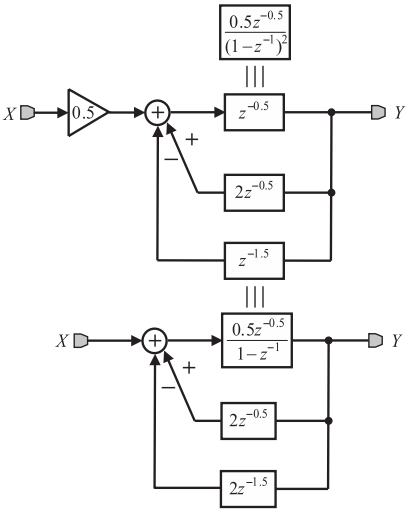

Fig. 5 Proposed half-delay double integrator architecture.

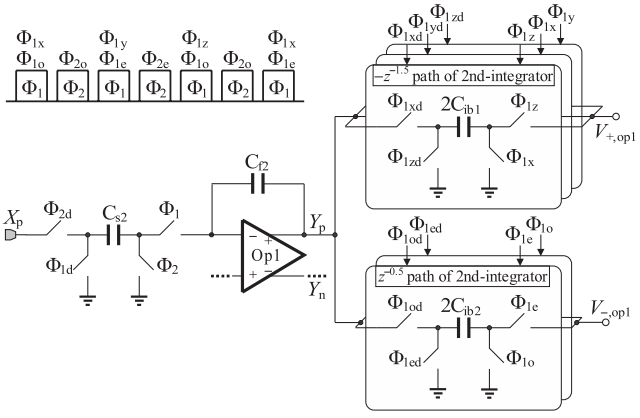

Fig. 6 Schematic of the proposed half-delay double integrator.

the proposed half-delay double integrator architecture. The transfer function of a conventional half-delay integrator is $0.5z^{-0.5}/(1-z^{-1})$. For the circuit implementation of Fig. 5, two additional switched-capacitor (SC) sampling paths are utilized to obtain $2z^{-0.5}Y$ and $2z^{-1.5}Y$. Figure 6 shows the circuit schematic of Fig. 5 where the clock signals $\Phi_{1e,o}$ and $\Phi_{1x,y,z}$ are the 1/2 and 1/3 clock frequencies of the clock signal Φ_1, respectively, for creating the analog delay. Using charge conservation for the finite opamp gain A leads to:

$$\begin{aligned} &C_{s2}Xz^{-0.5} + C_{f2}\left(Yz^{-1} - \left(-\frac{Yz^{-1}}{A}\right)\right) \\ &\quad = C_{s2}\left(0 - \left(-\frac{Y}{A}\right)\right) - 2z^{-1}2C_{ib2}\left(Y - \left(-\frac{Y}{A}\right)\right) \\ &\quad + 2z^{-2}C_{ib1}\left(Y - \left(-\frac{Y}{A}\right)\right) + C_{f2}\left(Y - \left(-\frac{Y}{A}\right)\right) \end{aligned} \tag{7}$$

Note that C_{s2}, C_{ib1}, and C_{ib2} are half the size of C_{f2}. Therefore, after rearrangement, the transfer function of a double integrator is:

$$\frac{Y}{X} = \frac{C_{s2}}{C_{f2}}\frac{C_{f2}A}{C_{f2}(A+1)+C_{s2}} \frac{z^{-0.5}}{1 - \frac{2C_{f2}(A+1)}{C_{f2}(A+1)+C_{s2}}z^{-1} + \frac{C_{f2}(A+1)}{C_{f2}(A+1)+C_{s2}}z^{-2}} \tag{8}$$

The term of $C_{f2}A/[C_{f2}(A+1)+C_{s2}]$ is the gain error. Considering the finite gain of the opamp, these two poles are shifted from DC to:

$$pole_{1,2} = \frac{C_{f2}(A+1)}{C_{f2}(A+1)+C_{s2}} \pm \sqrt{\left(\frac{C_{f2}(A+1)}{C_{f2}(A+1)+C_{s2}}\right)^2 - \frac{C_{f2}(A+1)}{C_{f2}(A+1)+C_{s2}}} \tag{9}$$

Equation (9) shows that the two poles of the double integrator are spread around $z = C_{f2}(A+1)/[C_{f2}(A+1)+C_{s2}]$. When the finite gain effect of the opamp in both the first and second integrators is taken into account, the NTF of the proposed DSM will become Eq. (10) at the bottom of the page where $G_{err1} = C_{f1}A/[C_{f1}(A+1)+C_{s1}]$ represents gain error in the first integrator, $G_{err2} = C_{f2}A/[C_{f2}(A+1)+C_{s2}]$ represents gain error in the second integrator, $L_1 = C_{f1}(A+1)/[C_{f1}(A+1)+C_{s1}]$ and $L_2 = C_{f2}(A+1)/[C_{f2}(A+1)+C_{s2}]$ mean the leakage factors of the first integrator and the second integrator, respectively. As described in Eq. (9), due to the double integrator separating two DC poles into two complex conjugate poles, the finite gain effect of the opamp moves two zeros in the NTF to high frequency and the two ones locate in conjugate positions, like the zero optimization effect [10]. In addition to the two ones, a zero in the NTF, as shown in Eq. (10), moves toward the original point in the z-domain. Its position depends on the value of L_1. The opamp gain controls the pole positions of the NTF as well, but in a single-loop DSM, the impact of pole change on performance is not significant, compared with a multi-stage shaping (MASH) DSM. Although the opamp gain controls the position of the complex zeros, optimization cannot be implemented since the opamp gain varies with process corners. Moreover, there is another advantage in the proposed DSM. Even though the structure suffers the finite gain effect, the STF is still unity and not changed because the blocks for U and V shown in Fig. 3(a) are fully symmetry. Figure 7 shows the simulation results by the SIMULINK behavior model concerning the opamp gain and kT/C noise. The SNDR only varies about 1 dB

$$NTF_{\text{finite-gain}}(z) = \frac{(1-L_1z^{-1})(1-2L_2z^{-1}+L_2z^{-2})}{1-(L_1+2L_2-3G_{err2})z^{-1}+(L_2+2L_1L_2-G_{err2}+G_{err1}G_{err2}-3G_{err2}L_1)z^{-2}-(L_1L_2-G_{err2}L_1)z^{-3}} \tag{10}$$

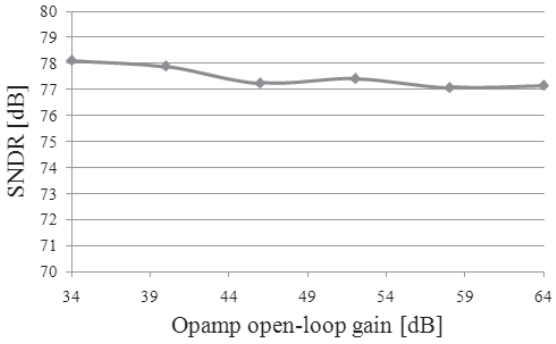

Fig. 7 SNDR of the proposed DSM with opamp open-loop gain.

for 34-dB to 64-dB opamp gain under the same kT/C noise condition. This demonstrates that the opamp gain is non-critical on the performance of a single-loop DSM using the double-integrator.

Furthermore, a differential sampling scheme is used for sampling the double integrator output of Fig. 6 to augment the feedback factor. In Fig. 8, the parasitic capacitance at the two plates of a sampling capacitor is taken into account. C_{pb} consists of the parasitic capacitance between the sampling capacitors (C_{ib2}'s) bottom plate and substrate, the parasitic capacitance from switches connected to the bottom plate, and the routing parasitic capacitance. Similarly, C_{pt} includes the parasitic capacitance between the sampling capacitors top plate and substrate, the parasitic capacitance from switches connected to the top plate, and the routing parasitic capacitance. Figure 8(a) shows shows the realization of a $2z^{-0.5}$ SC sampling path. The size of C_{ib2} is equal to half of the integrating capacitor of the second integrator. For a conventional DSM with a double integrator technique, the additional paths, the diminished feedback factor, and increased loading raise the performance requirements on opamp. To decrease the performance requirements of the opamp, a differential sampling scheme [16] is adopted, as shown in Fig. 8(b). Using this scheme, the required $2C_{ib2}$ is replaced by C_{ib2}. If the parasitic capacitance of C_{ib2} is not considered, although each output of the opamp still sees the $2C_{ib2}$ load, the feedback factor can be improved and the total capacitive load is slightly alleviated. In Fig. 8(a), if the top plates of $2C_{ib2}$ are connected to the opamp inputs during Φ_{1e} and the bottom plates of $2C_{ib2}$ are connected to the opamp outputs during Φ_{1o}, the bottom plate parasitic capacitance, $2C_{pb}$, will increase the load at each opamp output to become $2C_{ib2} + 2C_{pb}$. In contrast, if the bottom plates of $2C_{ib2}$ are connected to the opamp inputs during Φ_{1e}, the larger $2C_{pb}$ compared to the top plate parasitic capacitance, $2C_{pt}$, will degrade the feedback factor although the load at the opamp output during Φ_{1o} is smaller. Nevertheless, in Fig. 8(b), the feedback factor is increased since C_{ib2} replaces the original $2C_{ib2}$. The total load at each opamp output becomes $2C_{ib2} + C_{pb} + C_{pt}$ during Φ_{1o}, which is less than that shown in Fig. 8(a). In the differential sampling scheme, the delayed integrator output signal stored on C_{pt} is transferred to the integrating capacitor, but the effect can be neglected in

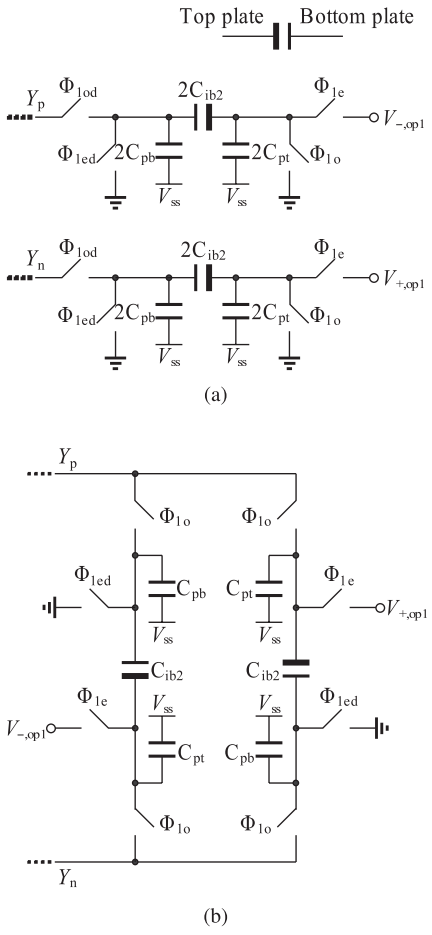

Fig. 8 (a) Conventional SC sampling scheme and (b) differential SC sampling scheme.

a single-loop DSM due to C_{pt} being much smaller than C_{ib2}. The parasitic effect is also verified during simulation by modeling the top and bottom nodes parasitic capacitances, which are approximately 0.05 and 0.4 time of the designed capacitor.

4.2 Loop Filter

For simplification, Fig. 9 shows the half-schematic diagram of the first and second integrators. In reality, they are implemented as fully differential. The clock signals Φ_{1o}, Φ_{1e}, Φ_{2o}, and Φ_{2e} are used for the $z^{-0.5}$ and z^{-1} SC sampling circuit and the clock signals Φ_{1x}, Φ_{1y}, and Φ_{1z} are used for the $z^{-1.5}$ SC sampling circuit. For SC analog-delay paths of Fig. 9, the switches surrounded by a dotted line are shared by the 15 SC sets. This means that 16 SC sets have only two switches on the right side of a capacitor. C_{f1} is the integrating capacitor of the first integrator, and C_{f2} is the integrating capacitor of the second integrator. For these two integrators to share an opamp, the integrating capacitors, C_{f1} and C_{f2}, are in integration in either Φ_1 or Φ_2. As mentioned in Sect. 3.1, the gain of the second integrator is set to 1/2, which gives $C_{s2} = 0.5C_{f2}$, $C_{fw2} = 0.5C_{f2}$, and $C_{fw3} = 1.5C_{f2}$.

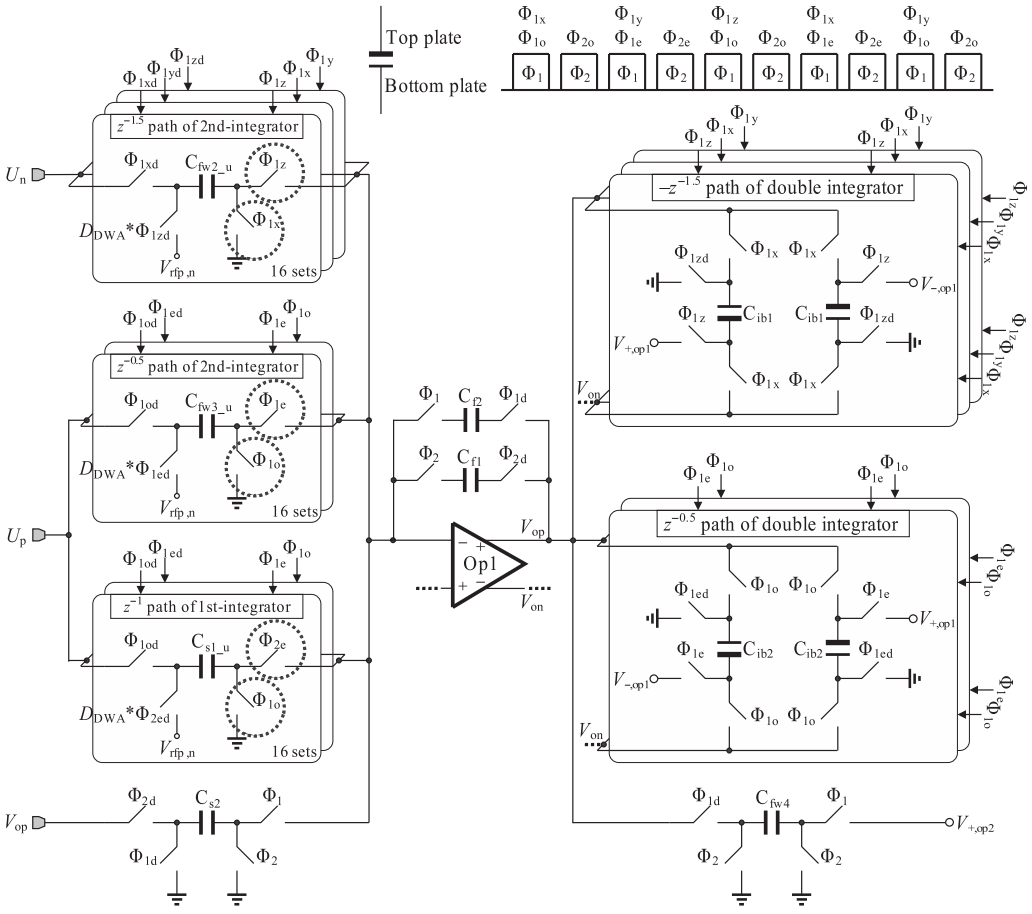

Fig. 9 Schematics of the first and second integrators.

4.3 Quantizer

Because the opamp in the active adder only works in Φ_1, the same opamp can be used for the quantizer in Φ_2. Therefore, a cyclic ADC is adopted as the quantizer for the reason of efficiently utilizing the opamp. Equation (5) indicates that the total signal delivered to the quantizer consists of the input signal plus $(NTF-1)Q$. Considering the usable output swing of the opamp, the gain of the active adder is set to 1/4. In an SC circuit, the power consumption is proportional to the output capacitive loading. So, a loading-free technique [17] for a pipelined ADC has been proposed to reduce power consumption. The basic concept of this technique is that the feedback capacitor of the $MDAC_i$ (mulitiplying DAC) in the present stage can act as the sampling capacitor of $MDAC_{i+1}$ in the next stage. Thus, the total loading of the $opamp_i$ can be reduced significantly because the sampling capacitor of $MDAC_{i+1}$ dominates the amount of total loading.

It is well known that the sampling capacitor of the latter stage can be scaled down due to the progressively decreased thermal noise contribution in the latter stage. To further reduce the power consumption of the quantizer, a cyclic ADC, shown in Fig. 10, is used; it combines the loading-free technique and the capacitor reuse technique [18]. In this work,

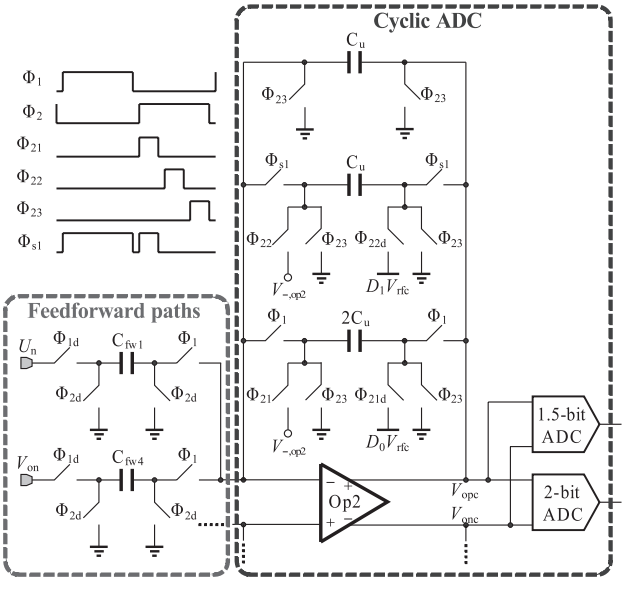

Fig. 10 Schematic of 4-bit loading-free cyclic ADC as active adder and quantizer.

the ratio of the feedback capacitors is 2:1:1 for a 4-bit 1.5-bit/stage cyclic ADC. Moreover, as mentioned earlier, the

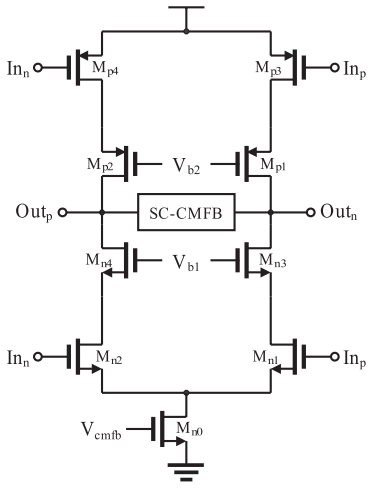

Fig. 11 Class-AB telescopic opamp.

gains of the active adder and the second integrator are individually set to 1/4 and 1/2, which gives $C_{fw1} = C_u$ and $C_{fw4} = 2C_u$. The reduced gain of the active adder leads to a larger feedback factor, which means a lower gain error and lower required opamp performance. In the sampling phase (i.e., the active adder is in operation), the second integrator output and the input signal are summed and sampled on the total feedback capacitors, and the feedback factor is 4/7. When Φ_1 goes from high to low, the 1.5-bit sub-ADC makes a decision. In Φ_{21}, the top two C_u still serve as feedback capacitors and the right side of the bottom capacitor sized $2C_u$ is connected to the DAC output to carry out the MDAC function. In Φ_{22}, the top C_u continuously acts as the feedback capacitor while another C_u becomes the DAC capacitor. Then, Φ_{23} is used to complete the digital error correction and the DEM operation and for resetting capacitors. Hence, during the bit cycling, the opamp would not be loaded by the additional sampling capacitor and the feedback factor is 1/2. For DEM implementation, the data weighted averaging (DWA) [19] method, which can shape the mismatch in first-order low-pass function, is employed. In this design, a $T_s/6$ time period, rather than just a non-overlapping time interval in a conventional low-distortion DSM, is used for DWA operation.

4.4 Opamp

It is well known that in a single-loop DSM, the opamp open-loop gain must satisfy the condition $A > OSR/\pi$ [9]. This condition can be easily met using a low OSR. Therefore, the opamp can be a single-stage telescopic type since it has a better unity-gain bandwidth than that of the two-stage type. Although telescopic opamps have a reduced output swing, this drawback is not relevant to the proposed design because the output swing of the integrators and the quantizer are within ± 150 mV. To further increase the unity-gain bandwidth of the opamp, a class-AB telescopic opamp is adopted, as shown in Fig. 11. In addition to the NMOS transistors (M_{n1} and M_{n2}), the differential input signal ($In_{p,n}$) is applied to the PMOS transistors (M_{p3} and M_{p4}). The equivalent transconductance (G_m) of the amplifier is:

$$G_m = g_{mn1,2} + g_{mp3,4} \tag{11}$$

where $g_{mn1,2}$ and $g_{mp3,4}$ are the transconductances of $M_{n1,2}$ and $M_{p3,4}$, respectively. This enhances the unity-gain bandwidth and the open-loop gain. The V_{gs} of $M_{p3,4}$ should be large because a small V_{gs} leads to excessive C_{gs}, which degrades the feedback factor.

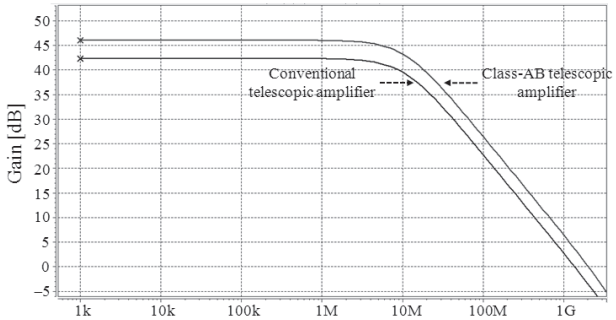

Fig. 12 AC simulation of the amplifier for the integrators.

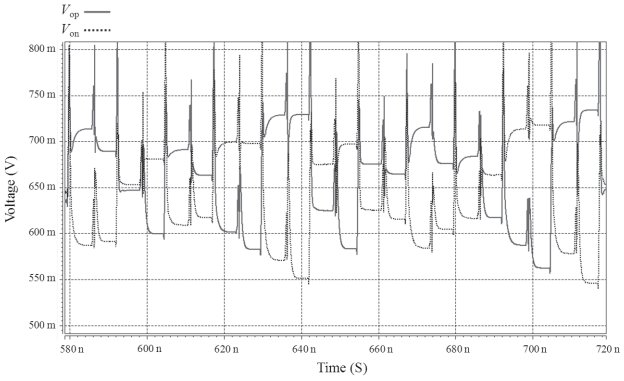

Fig. 13 Transient simulation of integrators.

Figure 12 shows the AC simulation of the amplifier for the integrators with and without the class-AB method. The unity-gain bandwidth increases from 1.36 GHz to 2.03 GHz and the gain improves by around 3.7 dB with the class-AB method; the phase margin decreases from 78.6° to 73.1°. Thus, consuming the same power, the class-AB amplifier can improve the unity-gain bandwidth by around 50 percent in this design. Figure 13 shows the transient simulation which proves that the output of the integrators swings within ± 150 mV. In this work, both the integrator and the cyclic ADC use the class-AB telescopic amplifier.

5. Simulation Results

The proposed third-order low-distortion DSM with opamp sharing and relaxed feedback path timing was implemented in a 90-nm 1P9M CMOS process. An 80-MHz sampling

Table 1 Performance summary and comparison.

Specification	Bos [1]			Waki [2]*	Lee [11]	Rajaee [13]		Nishida [14]	This work*
Technology(nm)		90		350	180	180		180	90
Supply voltage(V)		1.2		3	1.5 (A) / 1.45 (D)	1.65 (A) / 1.7 (D)		1.8	1.2
Sampling rate (MS/s)	50	90	80/320	40	60	72		40	80
OSR	250	90	20/80	100	16	8	6	20	16
Signal BW (MHz)	0.1	0.5	1.92	0.2	1.9	4.5	6	1	2.5
SNR (dB)	N/A	N/A	N/A	N/A	81	76	72.2	N/A	82.4
SNDR (dB)	77	76	65.5	80.14	81	75.5	71.8	75	81.97
Power (mW)	3.43	3.7	6.83	11	4.4 (A) / 3.7 (D)	16.4 (A) / 13 (D)		42.4 (A) / 16 (D)	2.53 (A) / 1.64 (D)
FOM (pJ/conv.-step)	2.86	0.74	1.17	3.31	0.25	0.67	0.77	6.34	0.0815

* simulation

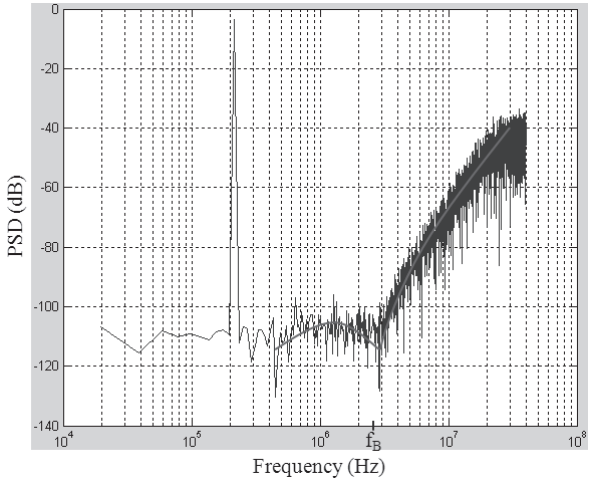

Fig. 14 PSD with −3.5 dBFS input signal amplitude.

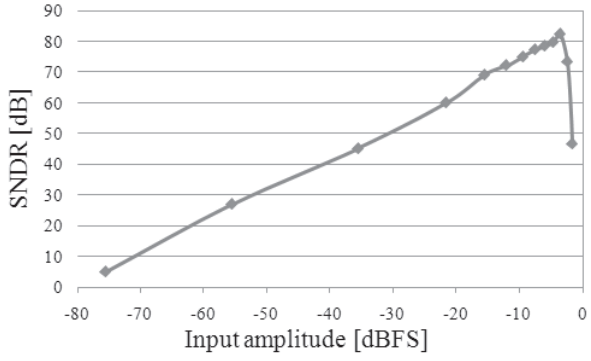

Fig. 15 SNDR versus input signal amplitude.

rate and 16-X OSR were utilized. The power supply voltages for the analog and digital circuits were both 1.2 V. Figure 14 shows the spectrum results of 4096-point fast Fourier transform analysis. The SNDR reaches 81.97 dB for an input frequency of around 200 kHz with a −3.5 dBFS input amplitude. Obviously, there are two conjugate zeros around the signal BW because of the finite gain effect in the double integrator. In addition, Fig. 15 shows the relationship between the input signal amplitude and SNDR. The dynamic range is above 80 dB. Table 1 summarizes the simulation results. With opamp sharing and class-AB telescopic opamp techniques, the analog power consumption is only 2.53 mW.

The figure of merit (FOM) for the evaluation of ADC is defined as [13]:

$$FOM = \frac{Power}{2^{ENOB} \cdot 2BW}. \tag{12}$$

A comparison with previous works, namely noise coupling [11], [14], hybrid DSM/pipelined ADC [13], multirate MASH [1], and bandpass [2] architectures, is also shown in Table 1. Simulation results show that for both SNDR and signal BW, the proposed architecture has a power-efficiency advantage and an outstanding FOM. However, we do recognize that the simulation results incluing the SNDR and FOM do not and cannot consider kT/C noise when using circuit simulator.

6. Conclusion

A third-order low-distortion DSM was proposed. It manipulates opamp sharing to fully exploit the opamp performance in the second integrator. In addition, the timing limitation of the quantization and DEM operations is extended to half a clock cycle. Therefore, a loading-free cyclic ADC can be easily adopted as the quantizer. The opamp used for cyclic ADC is shared with the active adder. The proposed architecture is suitable for DSMs with both active and passive summations in front of the quantizer. If the adder is an active type, the noise coupling technique can be used and the opamp used in the active adder can be shared with the cyclic-type quantizer. If a passive adder is adopted and a flash ADC is utilized for the quantizer, the design complexity of the comparators in the flash ADC is tolerable due to the existence of only two summing paths in front of the quantizer. Simulation results verify that a third-order DSM just needs two opamps (including loop filter, the active adder and the quanitzer) and that the proposed structure can achieve excellent power efficiency.

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