Transition-Code Based Linearity Test Method for Pipelined ADCs With Digital Error Correction

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***Abstract*—A transition-code based method is proposed to reduce the linearity testing time of pipelined analog-to-digital converters (ADCs). By employing specific architecture-dependent rules, only a few specific transition codes need to be measured to accomplish the accurate linearity test of a pipelined ADC. In addition, a simple digital Design-for-Test (DfT) circuit is proposed to help correctly detect transition codes corresponding to each pipelined stage. With the help of the DfT circuit, the proposed method can be applied for pipelined ADCs with digital error correction (DEC). Experimental results of a practical chip show that the proposed method can achieve high test accuracy for a 12-bit 1.5-bit/stage pipelined ADC with different nonlinearities by measuring only 9.3% of the total measured samples of the conventional histogram based method.**

***Index Terms*—Analog-to-digital converter (ADC), design-for-test (DfT), differential nonlinearity (DNL), integral nonlinearity (INL), pipelined, static linearity test, transition code.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are important components in mixed-signal systems. Integral nonlinearity (INL) and differential nonlinearity (DNL) are two critical linearity specifications of ADCs. In general, full-code histogram-based testing methods, either the ramp type or sinusoidal type, are used to measure the INL and DNL of ADCs [1]. Moreover, many published studies employ the histogram based method to further test the dynamic performance of ADCs, such as effective number of bit (ENOB) [2]–[5]. Large code bin width (CBW) per code is used to obtain accurate linearity performance of ADCs, but it requires a long test time and thus high test cost, especially for high-resolution ADCs.

Many innovative methods have been proposed to reduce the ADC linearity test time. They can be categorized according to their basic concepts as 1) model based methods [6]–[10] and 2) selective code based methods [11], [12].

In model based methods, behavioral models corresponding to the circuit characteristics of the ADCs under test are built. These models comprise unknown parameters which can be solved using a few measured input-output data. The number of unknown parameters is usually far less than the total number of ADC digital codes. Therefore, the test time of an ADC is significantly reduced because only a few measured samples are required. However, these methods have some limitations of test accuracy. First, the finite resolution of an ADC induces additional truncation error for the algorithmic calculation of solving model parameters. Second, the accuracy of models greatly affects that of the ADC linearity test.

In [11], authors find that error effects of ADC nonlinearity only cause CBW variations of specific codes, which are regular and repeated. As a result, only a few specific digital codes are measured and testing results of other codes are filled with measured data. The linearity test time is reduced and accurate test results are obtained. However, for this selective code based method, the architectures of ADCs under test must be known in advance because the selective codes depend on ADC architectures. The method proposed in [12] is a hybrid of the model based and selective code based methods. The number of required test codes is lower than that of model-based methods. However, this method still has the limitations of model based methods.

The digital error correction (DEC) technique has been extensively applied to relax the comparator offset requirement in pipelined ADCs [13]–[16]. However, the selective code based methods in [11] and [12] only focus on the 1-bit/stage architecture of pipelined ADCs without DEC technique. In this paper, a transition-code based method is proposed to reduce the linearity test time of pipelined ADCs with DEC. A characteristic analysis of pipelined ADCs with DEC shows that only some specific codes of each pipelined stage suffer from large nonlinearity when gain errors exist. These codes are called transition codes. Only a few transition codes of each pipelined stage need to be measured [17]. As a result, the ADC test time can be significantly reduced. Moreover, a simple digital Design-for-Test (DfT) circuit is also proposed to assist in detecting transition codes of each pipelined stage [18].

The rest of the paper is organized as follows. Section II introduces the error mechanism of pipelined ADCs. Section III describes the testing concept of the proposed transition-code based method. Transition code detection is addressed in Section IV. The complete test procedure is described in detail in Section V. Simulation results are used to demonstrate the effectiveness of the proposed method in Section VI. Finally, the conclusions are given in Section VII.

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II. Error Mechanism of Pipelined ADCs

The general architecture of a conventional pipelined ADC with DEC is shown in Fig. 1. A pipelined ADC usually consists of a front-end S/H followed by several cascaded pipelined stages. Digital logic circuits are required to perform the time alignment and the offset error correction of DEC. Each pipelined stage processes n-bit coarse quantization of the input signal V_i and gives the residual output V_{i+1} to the next stage. Functions of each pipelined stage, such as S/H, sub-DAC, subtraction, and stage amplification, are usually implemented together with a multiplying digital-to-analog converter (MDAC) circuit [13], [14].

The 1.5-bit/stage architecture is popular for constructing a high-speed pipelined ADC because it can tolerate large comparator offset with the help of DEC [13], [14]. Hence, a 1.5-bit/stage pipelined ADC is selected as an example to illustrate the proposed method. The presented method can also be applied to other architectures (1-bit/stage, 2-bit/stage, 2.5-bit/stage, etc.) used for pipelined ADCs. However, the selected test codes, which depend on the architectures of ADCs under test, should be modified based on the method mentioned in the following sections.

The ideal transfer curve of a 1.5-bit/stage pipelined stage is the curve with gray line, as shown in Fig. 2. Reference voltages, which define the operating range of a pipelined ADC, are $\pm V_{\rm ref}$. Ideal decision levels of comparators in the sub-ADC are set as $-V_{\rm ref}/4$ and $+V_{\rm ref}/4$. With the help of DEC, a $\pm V_{\rm ref}/4$ comparator offset can be tolerated. The ideal transfer function of a 1.5-bit/stage stage is given by

$$V_{\rm out} = 2V_{\rm in} + V_{dac} \tag{1}$$

where ideal stage gain is 2 and ideal DAC voltage (V_{dac}) is $\{0, \pm V_{\rm ref}\}$, which depends on digital outputs of the sub-ADC.

A typical switched-capacitor (SC) MDAC for a 1.5-bit/stage pipelined stage is shown in Fig. 3 [13], [14] . In ϕ_1, the input signal is sampled by C_s and C_f . In ϕ_2, the MDAC circuit produces residual output for the subsequent stage. Early falling clock ϕ_{1a} is used to avoid signal-dependent charge injection. The practical transfer function of a 1.5-bit/stage MDAC, including finite operational amplifier (op-amp) gain error and capacitor mismatch error, is given by (2)–(3) shown at the bottom of the page, where A is the finite op-amp gain, f is the feedback factor of the MDAC circuit, and C_{op} is the parasitic capacitance at the inverting input node of the op-amp. The stage gain and DAC voltage are affected by capacitor mismatch and finite op-amp.

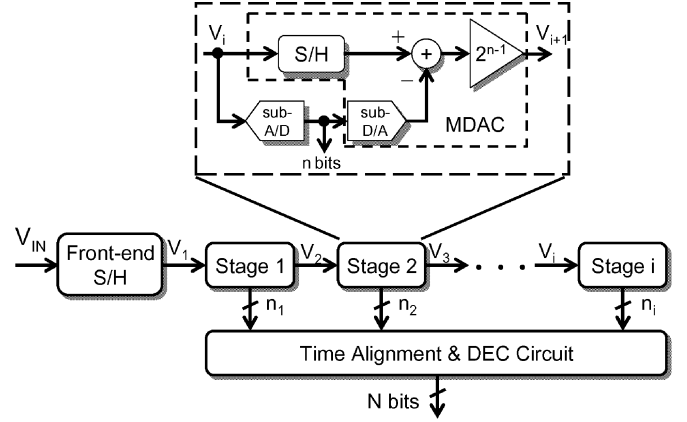

Fig. 1. Block diagram of an N-bit pipelined ADC with RSD.

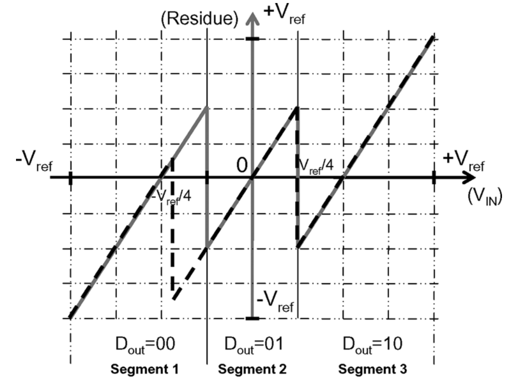

Fig. 2. Ideal transfer curve of a 1.5-bit/stage MDAC circuit.

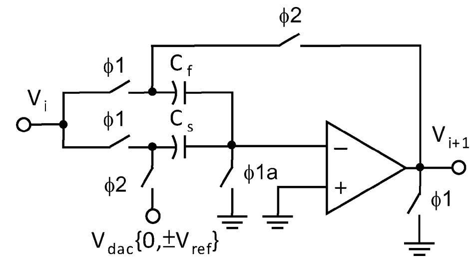

Fig. 3. Typical switched-capacitor MDAC circuit.

Critical error sources that are intrinsic in an SC MDAC circuit can be categorized into two groups as follows.

$$V_{\rm out} = \begin{cases} \left(V_{\rm in}\left(1+\frac{C_s}{C_f}\right) + V_{\rm ref}\frac{C_s}{C_f}\right)\cdot\left(\frac{1}{1+\frac{1}{Af}}\right), & V_{\rm in} < -\frac{V_{\rm ref}}{4} \\ V_{\rm in}\cdot\left(1+\frac{C_s}{C_f}\right)\cdot\left(\frac{1}{1+\frac{1}{Af}}\right), & -\frac{V_{\rm ref}}{4} \le V_{\rm in} < \frac{V_{\rm ref}}{4} \\ \left(V_{\rm in}\left(1+\frac{C_s}{C_f}\right) - V_{\rm ref}\frac{C_s}{C_f}\right)\cdot\left(\frac{1}{1+\frac{1}{Af}}\right), & V_{\rm in} \ge \frac{V_{\rm ref}}{4} \end{cases} \tag{2}$$

$$f = \frac{C_f}{C_s + C_f + C_{op}} \tag{3}$$

- Gain errors
  1) Finite op-amp loop gain
  2) Capacitor mismatch
  3) MDAC settling error
- Offset errors
  1) Comparator offset
  2) Op-amp offset
  3) Switch induced offset

Pipelined ADCs with DEC can tolerate large offset errors. However, the gain errors of an MDAC induce deviation of stage gain and DAC voltage from ideal values, which directly affect the linearity of a pipelined ADC. It is notable that other dynamic effects, such as ADC noise, test environment disturbance, would induce test error of the proposed method mentioned in the following. This issue will be addressed latter.

III. Testing Concept of Transition-Code Based Method

In the conventional histogram based method, the concept of code density is employed to estimate the INL and DNL of ADCs. The ideal distributions of every digital code corresponding to specific input signals, such as sinusoidal or ramp signals, are known in advance. As a result, when hit samples of every measured digital code are obtained, the DNL and INL of ADCs can be derived using

$$\begin{cases} DNL[i] = \frac{RW[i]}{IW[i]} - 1 \\ INL[i] = \sum_{k=2}^{i} DNL[k] \end{cases} \quad i = 2 \ldots \left(2^N - 1\right) \tag{4}$$

where IW and RW represent the normalized ideal and real code bin widths (CBWs) of the corresponding digital codes, respectively. In this method, the CBWs of every digital code need be measured, which requires a long test time. To reduce the linearity test time, a transition-code based method is developed. Its concept is introduced below.

A. Error Effects in the First Pipelined Stage

Fig. 4(a) shows the transfer curve of a 1.5-bit/stage pipelined stage. The dashed line is the ideal case, and the solid line is the real case with capacitor mismatch ($C_s < C_f$) and finite op-amp gain errors. The slope of the solid line is smaller than that of the dashed line due to gain errors. The solid line in Fig. 4(b) shows the transfer curve of an N-bit pipelined ADC whose first stage has gain errors, shown in Fig. 4(a); the following stages are ideal. The gain errors in the first stage induce large discontinuous jumps in the transfer curve of an N-bit pipelined ADC, as shown in Fig. 4(b). The discontinuous jumps in the ADC transfer curve are mainly induced by the gain errors of DAC voltages in the first stage, which are included by capacitor mismatch and op-amp gain error [19], [20]. Positions of the discontinuous jumps, around $3/8 \times 2^N$ and $5/8 \times 2^N$ digital codes, exactly match the transition edges in the residue transfer curve of the first stage. Other regions of the real ADC transfer curve have the same slope which is smaller than that of the ideal curve due to the stage gain error.

Based on the above-mentioned observations, CBWs of only the codes around the transition edges, that is, transition codes, of the first stage should be measured. Among other remaining codes, only one code should be measured because they have the same error effect. CBWs of unselected codes can be filled with that of the measured remaining code. As a result, CBWs of full codes can be obtained by measuring a few digital codes. The DNL and INL of a pipelined ADC in this case can be derived from (4). The test time is thus significantly reduced, and no complex algorithmic operations are required. It is noteworthy that the number of transition codes depends on the tolerable nonlinearity defined in ADC specifications. To accurately test

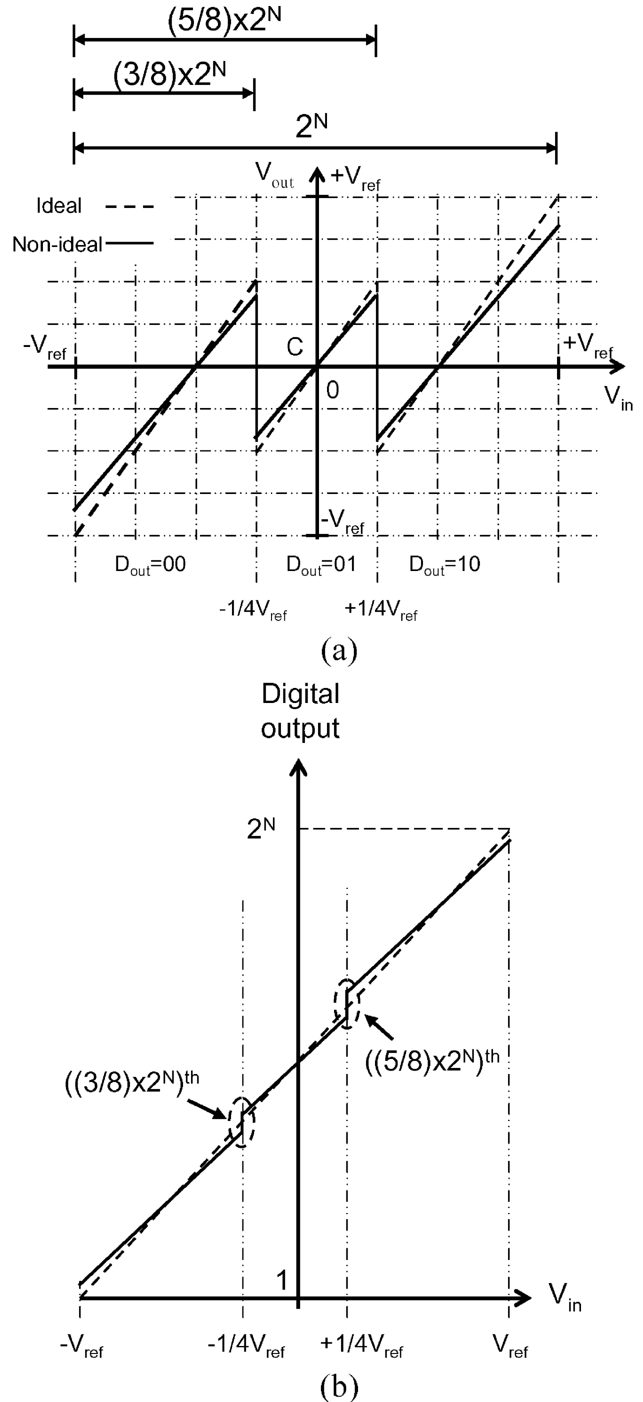

Fig. 4. (a)Transfer curve of a 1.5-bit/stage pipelined stage with gain error. (b) The transfer curve of whole pipelined ADC, which only considers gain errors in the first pipelined stage.

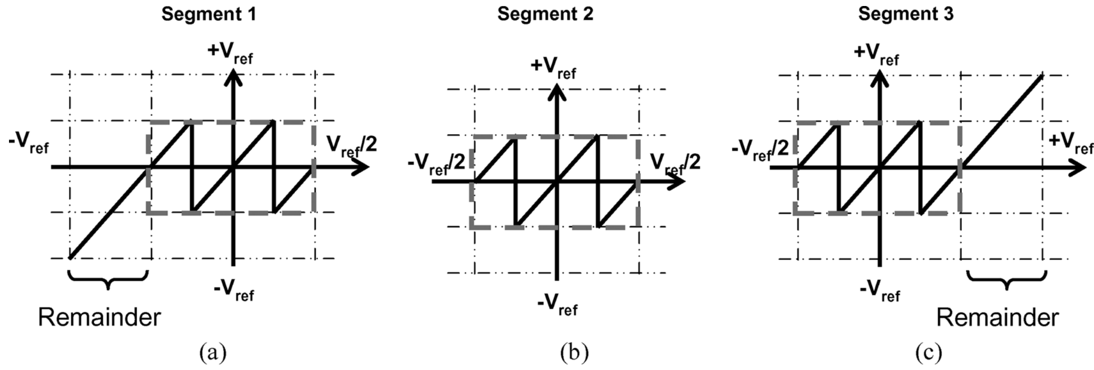

Fig. 5. Ideal transfer curve of the second 1.5-bit/stage pipelined stage corresponding to (a) the segment 1 (b) the segment 2 (c) the segment 3 of the residual output in the first pipelined stage shown in Fig. 2.

pipelined ADCs with large nonlinearity, a large number of transition codes should be selected and measured. The detailed description is given in Section V.

B. Error Effects in Multiple Pipelined-Stages

The transfer curve of the first stage is shown in Fig. 2, which comprises three segments. The corresponding transfer curves of the second stage for the three segments are shown in Fig. 5(a)–(c), respectively. The transfer curves surrounded by the dashed line have the same pattern. Therefore, CBW variations of the corresponding transition codes in these cases are the same. In other words, only two sets of transition codes among them need to be measured. As a result, although the transition edges in the latter stages of a pipelined ADC grow exponentially, only two sets of transition codes per stage need be measured. The number of required test codes is linearly proportional to the number of pipelined stages. The linearity test time is thus significantly reduced. Except for stage 1, the measured data are copied and filled into the un-selected transition codes by an interval of $2^{N\text{-}sg}$, where N is the resolution of an ADC and sg is the corresponding stage number.

IV. Transition Code Detection

A. Offset Effect in the Proposed Method

Fig. 6 shows transfer curves of a 1.5-bit/stage pipelined stage with comparator offset and op-amp offset. The comparator offset shifts transition edges right or left, whereas the op-amp offset shifts the whole transfer curve up or down (it does not affect the positions of transition edges). The DEC technique is extensively used to correct offset errors in pipelined/cyclic ADCs [13], [14]. When transfer curves of a pipelined stage shifted by offset errors do not exceed the signal range of a pipelined ADC ($\pm V_{\mathrm{ref}}$), offset errors do not degrade the linearity if DEC is used. Fig. 7 shows DNL results of a 10-bit pipelined ADC with various comparator offsets. No gain error was injected in this case. The DNL is almost perfect although there are large comparator offsets.

However, when gain errors appear in a pipelined stage, the CBWs around the selected transition codes vary dramatically, as description in the previous section. When we further consider the comparator offset, we have observed some surprising

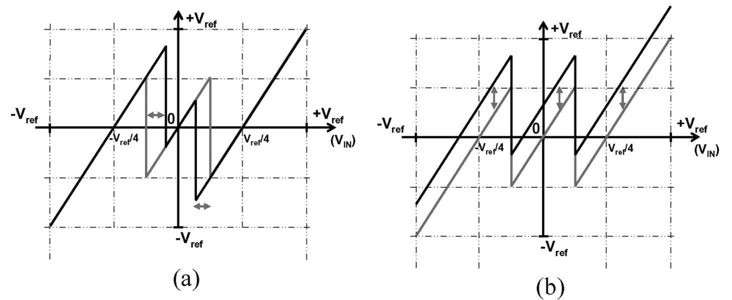

Fig. 6. Transfer curves of a 1.5-bit/stage pipelined stage, which is influenced by (a) comparator offset and (b) op-amp offset.

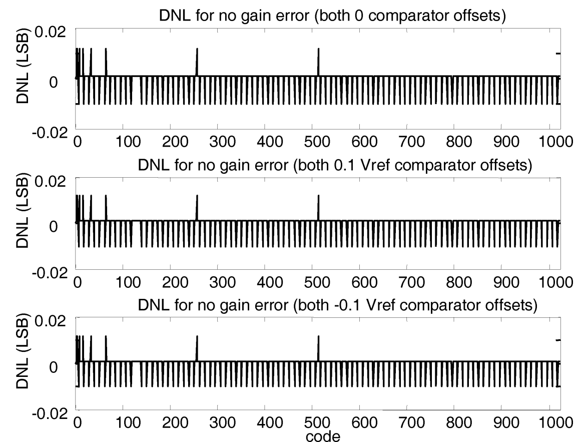

Fig. 7. DNL Results of a 1.5-bit/stage 10-bit pipelined ADC for no gain error and different comparator offsets of stage 1.

results. Fig. 8 shows DNL results of a 10-bit pipelined ADC whose first stage has positive gain error and various comparator offsets; the other stages are ideal. Positions of peak DNLs are shifted with comparator offsets. Moreover, values of peak DNLs are different for the three cases. This indicates that transition codes corresponding to each pipelined stage are shifted by comparator offsets. Because we don't know comparator offsets after fabrication, transition codes corresponding to each stage are difficult to estimate. To correctly detect transition codes, a digital DfT circuit is proposed.

It should be noted that comparator offsets do not affect the value of peak INL; only INL profiles are affected, as shown in

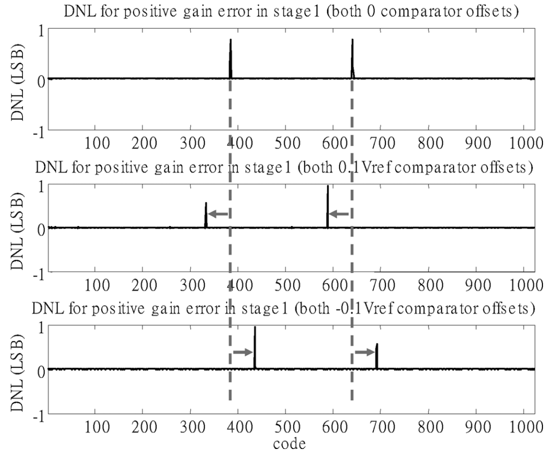

Fig. 8. DNL Results of a 1.5-bit/stage 10-bit pipelined ADC for positive gain error and different comparator offsets of stage 1.

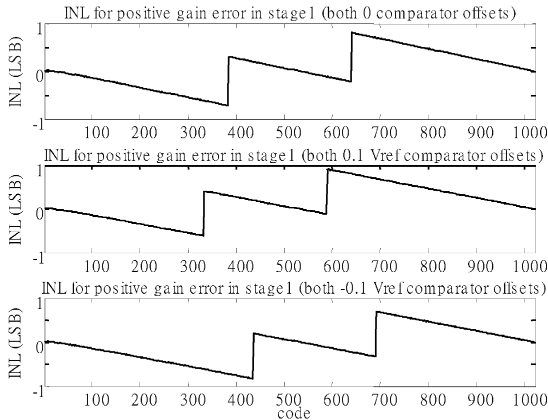

Fig. 9. INL Results of a 1.5-bit/stage 10-bit pipelined ADC for positive gain error and different comparator offsets of stage 1.

Fig. 9. As a result, the comparator offset does not affect the linearity of a pipelined ADC, the same as the well known knowledge. Moreover, because the op-amp offset does not affect the transition edges of a pipelined stage, it does not shift transition codes.

B. Proposed Design-for-Test Circuit

Two transition edges of the least significant bit (LSB) (i.e., logical transitions $0 \rightarrow 1$ and $1 \rightarrow 0$) of the sub-ADC match those of the residue transfer curve in each pipelined stage. As a result, when the coarse LSB of the target stage is forced to zero, output codes of a pipelined ADC have apparent jumps when either a ramp or slow sinusoidal input signal is applied. The required input test signal must ensure that ADC codes appear once more in an ideal case. Transition codes corresponding to this stage can be identified from the distribution of digital output. In this paper, a DfT signal generator shown in Fig. 10 is proposed to detect transition codes of each pipelined stage. This circuit produces the required test signal. The main block of the DfT circuit is a ring counter which consists of several resettable flip-flops and simple digital logic circuits. The number of phases depends on the number of pipelined stages. DfT_1 is the signal used for determining transition codes of the first stage, DfT_2 is the signal used for determining transition codes of the second stage, and so on. When one of DfT_x ($x = 1 \sim 8$) is high, the coarse LSB of the corresponding stage is forced to zero. When $DfT_1 \sim DfT_8$ are all zero, a pipelined ADC operates in normal mode. DfT_clk is a trigger signal, which is implemented with an external electrical switch. As a result, only one additional pin is required for the DfT circuit. Fig. 11 shows the circuit diagram of the proposed digital DfT circuit. In addition to the DfT gerenerator, multiple DfT Multiplexers are required to force the LSB of the sub-ADC in each stage before performing the DEC function. Fig. 12 shows digital output codes of a 10-bit, 1.5-bit/stage pipelined ADC with a ramp input signal when the LSBs of sub-ADCs in the first and second stages are forced to zero, respectively. Transition codes of the two stages can be easily identified from the distributions of the ADC output codes.

V. Test Procedure

Fig. 13 shows the test procedure of the proposed transition code based method. Because the ADC input referred offset affects the range of input stimulus for testing transition codes of each pipelined stage in the following test steps, the ADC offset must be firstly estimated. In the step 2, the practical transition codes of each pipelined stage are detected by using the proposed DfT circuit. In this step, the comparator offsets of each pipelined stage can be identified by comparing with detected and ideal transition codes. We also can determine if comparator offsets are larger than the tolerated value. In the step 3, multiple short ramp signals are used to test the detected transition codes of each stage. The test results of the un-selected codes are filled with those of selected test codes by following some specific rules in the step 4. When CBWs of all ADC codes are determined, the corresponding DNL and INL are performed using (4). Detailed descriptions of each test step are given below.

A. Estimate ADC Offset

The ADC offset is mainly sourced from the op-amp offset and switch induced offset. With the help of DEC, the ADC offset does not cause additional nonlinearity for a pipelined ADC; however, it affects the range of input stimulus for testing transition codes of each pipelined stage. Therefore, the ADC offset must be estimated before transition codes are detected and tested. The operating range of a fully differential ADC is from $-V_{\mathrm{ref}}$ to V_{ref}. Therefore, the ADC offset can be easily estimated when a zero input is used. The difference of the resulting output code and the ideal middle code (i.e., code 512 for a 10-bit ADC) is the ADC offset. Several samples ($Sample_{off_est}$) are collected and averaged to reduce the error effect of random noise. This value is determined by the amount of the ADC noise.

B. Detect Transition Codes

Large comparator offset is tolerated in a 1.5-bit pipelined stage. As a result, real transition codes of each 1.5-bit pipelined stage are possible to be shifted far away from ideal transition codes. Fig. 14 shows the concept diagram for the distribution of transition codes corresponding to the first three 1.5-bit stages. (1', 1"), (2', 2"), and (3', 3") represent the ideal transition codes corresponding to three stages, respectively. The gray and black

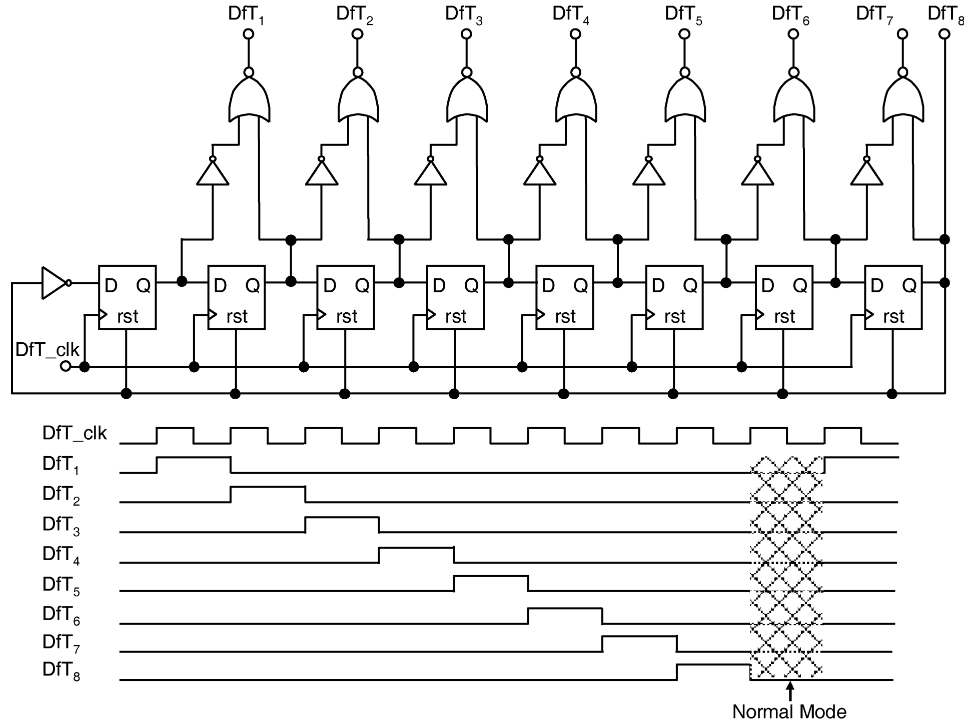

Fig. 10. DfT signal generator for identifying transition edges of each stage in a 10-bit 1.5-bit/stage pipelined ADC (eight 1.5-bit/stage stages and one 2-bit flash last stage).

array symbols represent the possible variation range of two transition codes for each stage without degrading the ADC linearity, respectively. When the detected transition codes are out of the tolerable range, it represents that too large comparator offsets occurs for the corresponding pipelined stage. The tolerant variation range of transition codes for the following stages is gradually scaled down by 2 because of the stage gain.

Transition codes of each stage and their error effects appear with a repeated and regular distribution, as described in Section III. Although there are several transition codes corresponding to each stage, only two set of transition codes must be measured. However, how to select proper transition codes of each stage significantly determines the testing accuracy of the proposed method. In the overlapped region of Fig. 14, transition codes of the target pipelined stage are possible to be the same with those of previous stages. Under this situation, the overlapped transition codes contain nonlinearities of previous stages, and the nonlinear error effect of target stage cannot thus be correctly identified. When the overlapped transition codes are selected and their measured results are duplicated for other transition codes of the target stage, the nonlinear effects of previous stages are also duplicated. As a result, the test accuracy of the proposed method is seriously degraded. To avoid this condition, the first and the last sets of transition codes of each stage, out of the overlapped region, are selected. These transition codes are impossible to be the same with those of previous stage when comparator offset does not exceed the tolerable value of DEC. The selected transition codes of the first three stages are marked with "ν" symbol in Fig. 14.

Because large comparator offset is tolerable, it is reasonable to assume that the transition codes of each stage do not exceed the tolerable range of pipelined ADCs. Based on this assumption, only a short ramp input stimulus, just cover the possible variation region of the detected transition code, is used to detect transition codes of each stage; i.e., $(2/32) \times 2^N \sim (4/32) \times 2^N$ for transition code 3'. As shown in Fig. 14, the total tolerable variation range of the selected transition codes (marked with "ν") for all stages exactly matches the whole operating range of an ADC. This indicates that the total time of the required short ramp signals equals that of the full range ramp signal. The corresponding transitions of each pipelined stage can be determined with short ramp signals. Because that the objective of the transition codes detection is to identify the transition edge (as shown in Fig. 12) instead of constructing histogram for code-width calculation, Only the ramp signals, which ensure that ADC codes appear once more in an ideal case, are required. The required code density (CD_{tr_detect}) for the transition code detection is relatively low compared with that for histogram test. Only a few samples are required for transition code detection. The required number of samples is $2^N \cdot CD_{tr_detect}$, as shown in (5). When proper transition codes are detected and selected, other transition codes can be determined because one pair of selected transition codes are repeated every $2^{(N\text{-}sg)}$ codes for the sg-th stage in an N–bit pipelined ADC. It should be noted that comparator offsets in each pipelined stage can be easily identified from the detected transition codes. This information is also employed to identify whether the comparator is in the tolerable range of a pipelined ADC under test.

C. Test Transition Codes

When small gain errors exist in pipelined stages, only two digital codes, corresponding to one transition edge in each stage, have large CBW variations. However, large gain errors lead to large nonlinearity. Eventually, missing code error could happen.

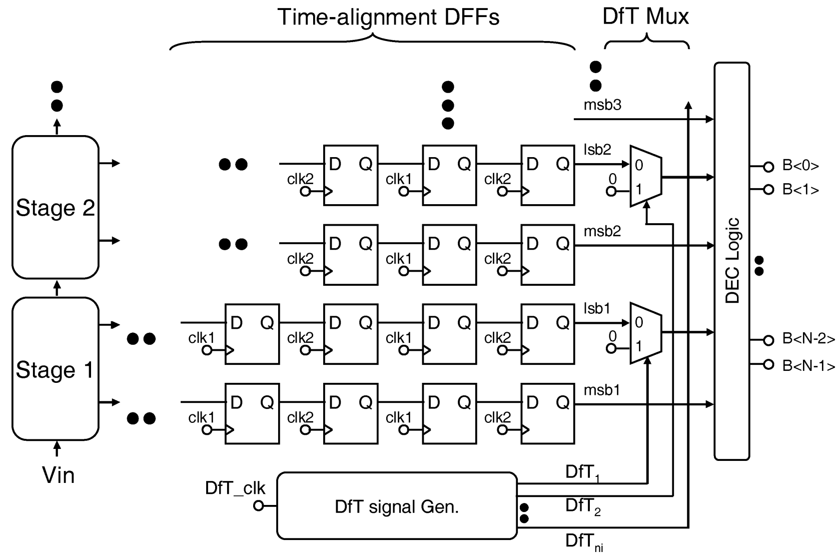

Fig. 11. Circuit diagram of the proposed digital DfT circuit.

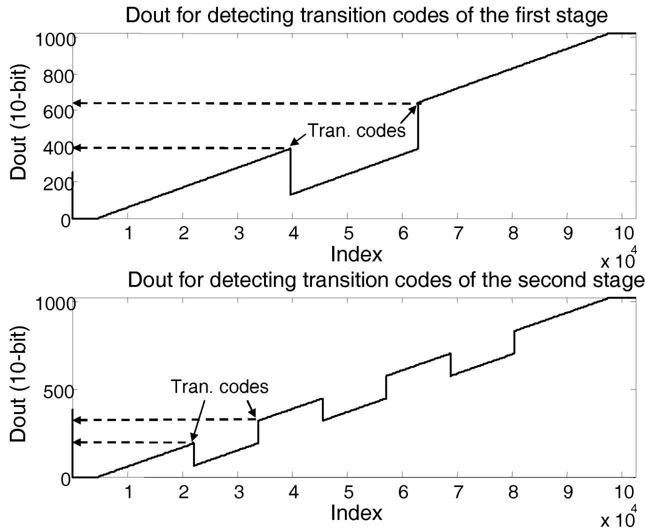

Fig. 12. Douts with a ramp input for detecting transition edges of the first stage and second stage, respectively.

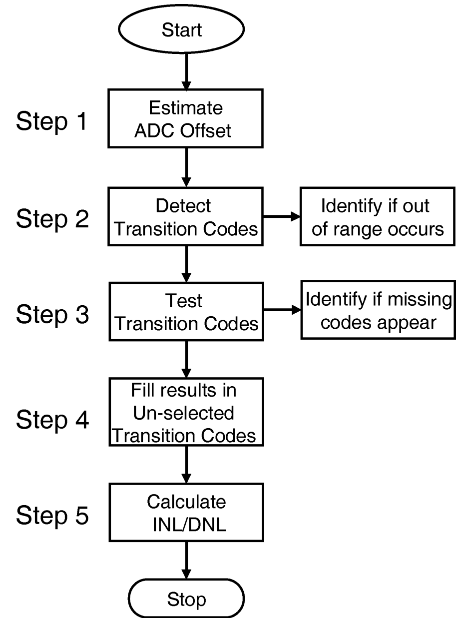

Fig. 13. Test procedure of the proposed transition-code based method.

More transition codes suffer from nonlinearity when larger gain errors exist in a pipelined stage. To accurately capture the linearity induced by gain error of each stage, a large number (m_{tr}) of digital codes around the selected transition code should be tested, as shown in Fig. 15. m_{tr} is determined from the pre-defined tolerable accuracy of ADCs under test. To accurately estimate a pipelined ADC with large gain error, a large m_{tr} value is used to detect large linearity, which requires more test time. It is noteworthy that the front-end stages usually suffer from larger nonlinearity than that of the backend stages in the general case. As a result, different m_{tr} values for different stages are used to perform good trade-off between test accuracy and test time.

Multiple short range ramp signals with small slope are employed as the test input. Large samples per code (CD_{tr_test}) can reduce the accuracy degradation caused by random noise. In this step, the CBWs of the selected transition codes are measured and recorded. It is noteworthy that a DNL resolution of an ADC under test is $1/CD_{tr_test}$ LSB in the ramp histogram method. Moreover, the DNL errors induced by limited resolution of the histogram method are accumulated to increase the INL errors. When higher resolution of ADCs are tested, higher CD_{tr_test} is required to achieve high INL and DNL test accuracy. As a result, CD_{tr_test} value is determined by the required test accuracy and the resolution of ADCs under test [21].

D. *Fill Results in Un-Selected Transition Codes*

When CBWs of selected transition codes are measured, CBWs of the unselected transition codes are filled with the measured data. Because the nonlinearities of the front-end stages usually dominate the performance of a pipelined ADC, transition codes corresponding to the front-end stages have high priority in the CBW filling process. When digital codes

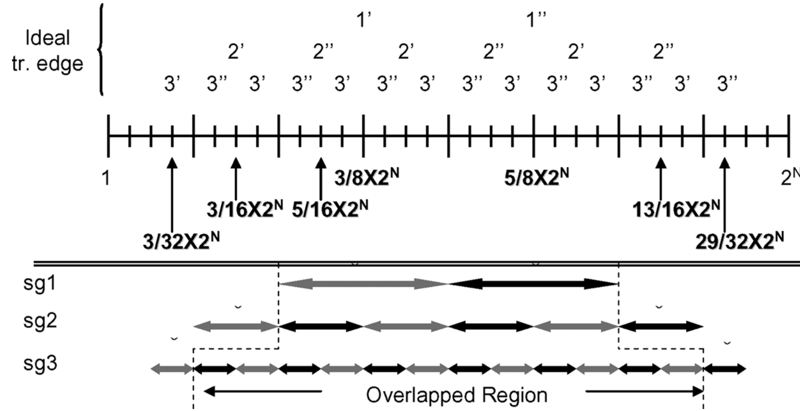

Fig. 14. Concept diagram for the distributions of transition codes corresponding to the first three 1.5-bit stages.

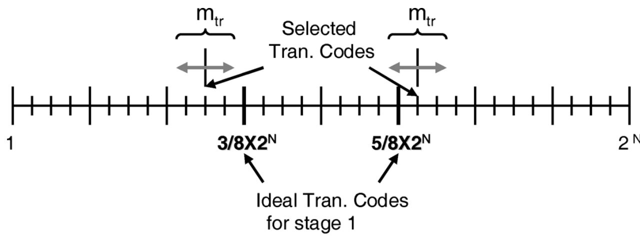

Fig. 15. Concept diagram for selecting transition code.

have been filled with their corresponding CBWs, the codes are omitted in the CBWs filling process of transition codes corresponding to the latter stages.

The curve with dash line in Fig. 2 is the curve when the stage has comparator offset. Fig. 16 shows the corresponding transfer curves of the second stages when stage 1 has comparator offset, as shown in Fig. 2. Segment 1 in the transfer curve of stage 1 is shorter than the ideal case due to the comparator offset. As a result, one transition edge of stage 2 corresponding to segment 1 disappears, as shown in Fig. 16(a). This means that there is no transition code corresponding to this transition edge in stage 2 in this case. As a result, this set of transition codes must be bypassed in the filling process of transition codes in stage 2, and their CBWs are filled with the measured data of the latter stages. Fig. 17 shows the concept diagram of identifying whether transition edges of a specific stage actually happen. Tr_{xy} represents the y-th transition code of stage x. In the ideal case, Tr_{11} is located between Tr_{22} and Tr_{23}, as shown in Fig. 17(a). Fig. 17(b) shows the condition corresponding to Fig. 16. Tr_{11} is outside the Tr_{22}-Tr_{23} interval and smaller than Tr_{22}, so it represents that Tr_{22} has disappeared. On the other hand, if Tr_{11} is larger than Tr_{23}, this represents Tr_{23} has disappeared. By identifying the relationships of transition codes corresponding to the previous and present stages, the correct distribution of transition codes of the present stage can be obtained to avoid false estimation. As a result, before the CBWs of the unselected transition codes are filled, the appearance identification of transition codes for each stage is performed first.

Finally, when the complete histogram is constructed by the filling process, the estimated INL and DNL are calculated using (4). The number of measured samples in the proposed method for an N-bit 1.5-bit/stage pipelined ADC with sg cascaded stages is

$$Sample_{total} = Sample_{off_est} + 2^N \cdot CD_{tr_\text{detect}} + \left(\sum_{i=1}^{sg} 2 \cdot m_{tr_i} \cdot CD_{tr_test} \right). \quad (5)$$

In the histogram based method, the required number of measured samples is about $2^N \cdot CD_{tr_test}$ when the CBW per code is assigned the same value with that in the transition code based method (CD_{tr_test}). When high-resolution ADCs are tested, the required number of samples in the proposed method is far less than that in the histogram based method. It is notable that the proposed method can be applied for the 1-bit/stage pipelined ADC without DEC. Because the 1-bit/stage pipelined ADC cannot tolerate any comparator offset, the corresponding transition codes of each pipelined stage do not vary significantly. As a result, the detection of transition codes is no longer to be required. Moreover, only one transition code set corresponds to each stage in the 1-bit/stage pipelined ADC because the 1-bit/stage pipelined stage has only one transition edge. The required number of samples for the 1-bit/stage pipelined ADC becomes

$$Sample_{total,1-bit} = Sample_{off_est} + \left(\sum_{i=1}^{sg} m_{tr_i} \cdot CD_{tr_test} \right). \quad (6)$$

VI. Experimental Results

A. Simulation Results

In order to verify the proposed method, a 12-bit pipelined ADC with ten cascaded 1.5-bit/stage pipelined stages and a 2-bit last stage was simulated. All simulations were conducted using the MATLAB tool. Tables I and II list simulation parameters of the pipelined ADC under test and the ADC linearity test, respectively. To accurately estimate the performance of the ADC with large nonlinearity, a large number of transition codes for the front-end stages were used (m_{tr}). Because the accuracy requirement of the latter stages gradually relaxes, the ADC nonlinearity caused by the latter stages is low. As a result, a small m_{tr} value is used for the latter stages. Every parameter is set as

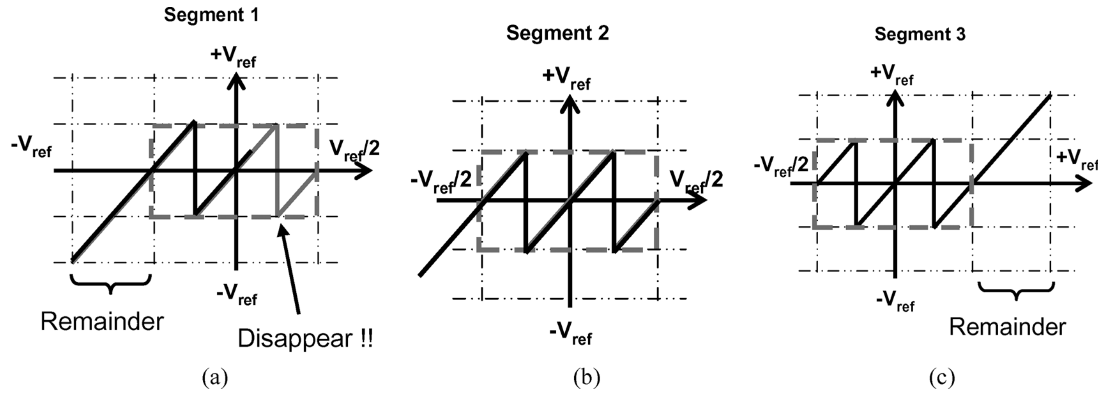

Fig. 16. The ideal 1.5-bit/stage transfer curve of the second pipelined stage corresponding to (a) the segment 1 (b) the segment 2 (c) the segment 3 of the residue output in the first pipelined stage *with* comparator offset, as the curve with dash line in Fig. 2.

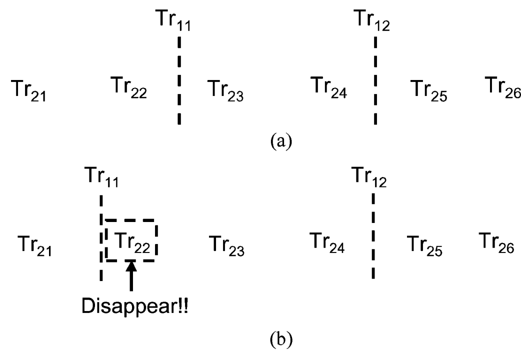

Fig. 17. Concept diagram of identifying if the transition codes appear (a) ideal case (b) real case with comparator offset in stage 1.

TABLE I
SIMULATED PARAMETERS OF PIPELINED ADC UNDER TEST.

Parameter		
Resolution	12 bit	
Architecture	1.5-bit/stage	
Swing	2 V_{pp}	
LSB	$2/2^{12}$	
Tolerable Comparator Offset	0.25 V	
Capacitor Value	Mean: 0.5 pF	Variance: 0.4 %
Op-amp Gain	Mean: 1000	Variance: 100
Input Referred Noise	Mean: 0 LSB	Variance: 0.25 LSB
ADC Offset	Mean: 0 LSB	Variance: 5 LSB
Comparator Offset	Mean: 0 V	Variance: 0.0625 V

a random variable to model the random distribution of component variation in practical cases.

Fig. 18 shows the simulated INL/DNL of the conventional histogram based method [22] and the proposed transition code based method with no additional random noise. INLs/DNLs of the two methods are almost the same. Even with many missing codes, the test result of the pipelined ADC linearity is still highly accurate. In the proposed method, only a few specific transition codes are measured and test results for the other codes are copied from the measured data. As a result, the errors induced by random noise and other disturbances are accumulated through the duplicated process to increase INL errors. Fig. 19 shows individual INLs/DNLs of the two methods with 0.25 LSB ADC random noise. The peak differences of the max/min INL and max/min DNL corresponding to the two methods are within 0.2 LSB and 0.02 LSB, respectively. Random noise induces minor additional errors compared with the case in Fig. 18. To validate the robustness of the proposed method, 50 samples of a 12-bit pipelined ADC with randomly distributed component mismatches were simulated. Fig. 20 shows histograms of differences of peak max/min INL values for the conventional histogram method and the proposed method. The estimated INL errors of 99.97% (3σ) are inside 0.3 LSB even for large ADC nonlinearity and noise. Compared with the conventional histogram based method, only 7% (28338/409600) of the total number of samples is required to achieve comparable test accuracy. When the proposed method is applied for higher resolution pipelined ADCs, the reduced test time is more apparent. The proposed

TABLE II
SIMULATED PARAMETERS OF ADC LINEARITY TEST.

Parameter			
CBW for Conventional Method	100 samples/code		
CBW for Proposed Method (CD_{tr_test})	100 samples/code		
CBW for Transition Code Detection (CD_{tr_detect})	3 samples/code		
Samples for Offset Estimation ($Sample_{off_est}$)	50 samples		
Samples of Transition Codes (m_{tr_x})	m_{tr_1}=21	m_{tr_2}=11	$m_{tr_3\sim10}$=6
Total samples for conventional method	409600		
Total samples for proposed method ($Sample_{total}$)	28338		

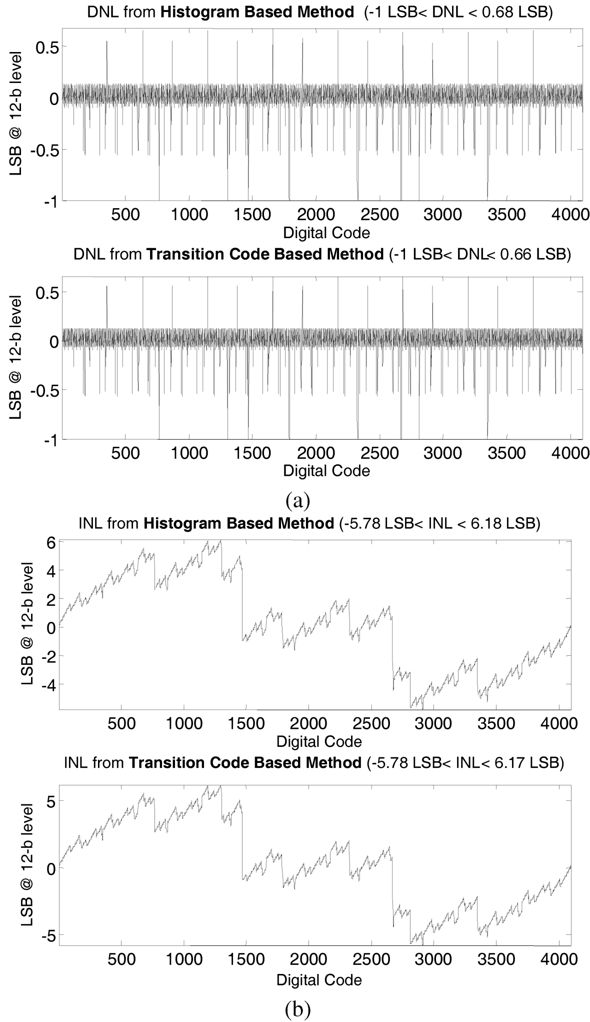

Fig. 18. (a) DNL results (b) INL results with the conventional histogram method and the proposed transition code based method under *no* additional noise.

method can be also applied for multi-bit DEC pipelined ADCs with minor refinements.

B. *Measurement Results*

A 12-bit 20-MS/s pipelined ADC was implemented in a CMOS 0.35 μm 2P4M process to verify the effectiveness of the proposed method. The die photograph of the chip is shown in Fig. 21. This prototype comprises 10 1.5-bit/stage pipelined stages and one 2-bit flash ADC. In this chip, additional capacitor tuning mechanism is used to inject the error effect of capacitor mismatch. By using this mechanism, the proposed method can be verified in a pipelined ADC with different nonlinearities.

In order to detect larger error effect, larger samples of transition codes (m_{tr_x}) than values in Table II are used. M_{tr_1}, M_{tr_2} and $M_{tr_3\sim 8}$ are set as 41, 21 and 11, respectively. Only transition codes of the first eight stages are measured. Fig. 22 shows the DNL and INL results of the pipelined ADC in a normal case without injecting additional capacitor mismatch by using the conventional and proposed methods. The measured peak absolute DNL and INL values with the conventional method are

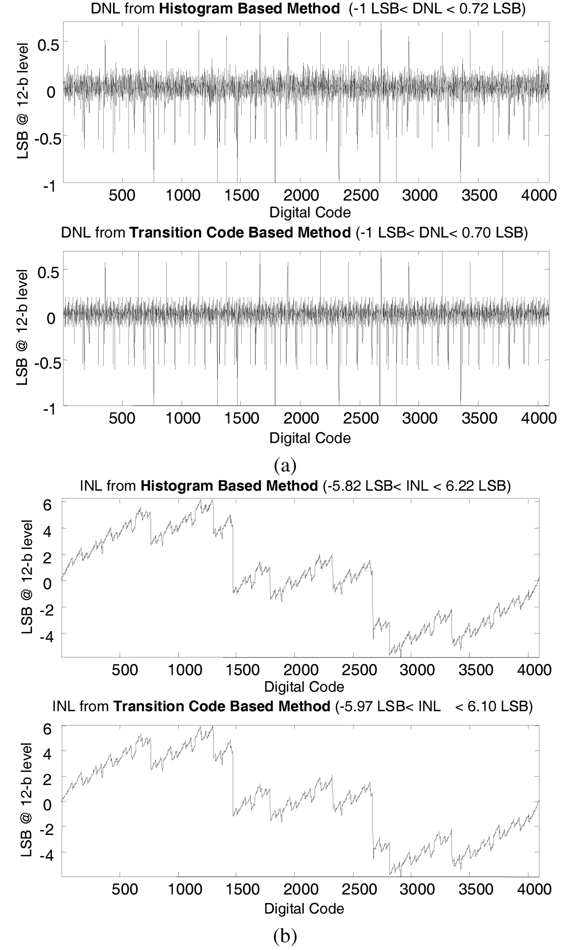

Fig. 19. (a) DNL results (b) INL results with the conventional histogram method and the proposed transition code based method under additional noise.

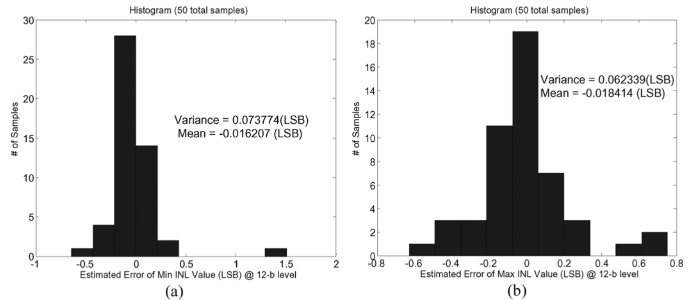

Fig. 20. (a) Histogram of difference of peak minimum INL value (b) Histogram of difference of peak maximum INL value for two methods.

0.37 LSB and 0.61 LSB, respectively. Compared with the DNL and INL results with the proposed method, the maximum differences of peak absolute DNL and INL values are 0.18 LSB and 0.15 LSB. Fig. 23 shows the DNL and INL results of the pipelined ADC with additional capacitor mismatch using two test methods. The maximum differences of peak absolute DNL and INL values between two methods are 0.27 LSB and 1.06 LSB in this case. These measured results shows that the proposed method can work well even when the pipelined ADC under test suffers from large nonlinearity. Critical INL profiles of two methods are almost the same. Additional random error

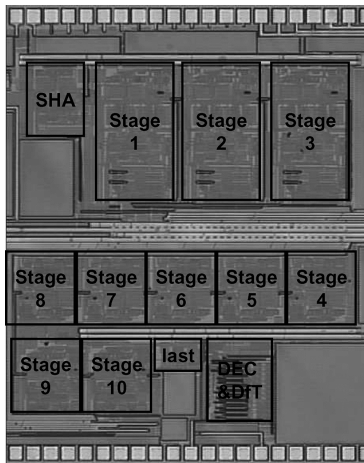

Fig. 21. Die photograph of the 12-bit pipelined ADC for demonstrating the proposed method.

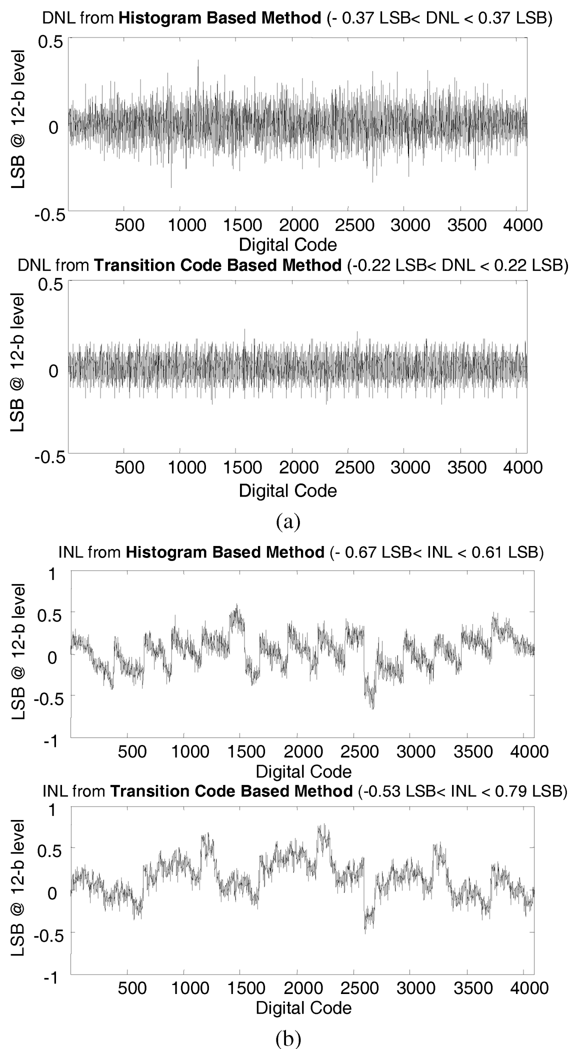

Fig. 22. (a) *Measured* DNL results (b) *Measured* INL results with the conventional histogram method and the proposed transition code based method in the Case 1.

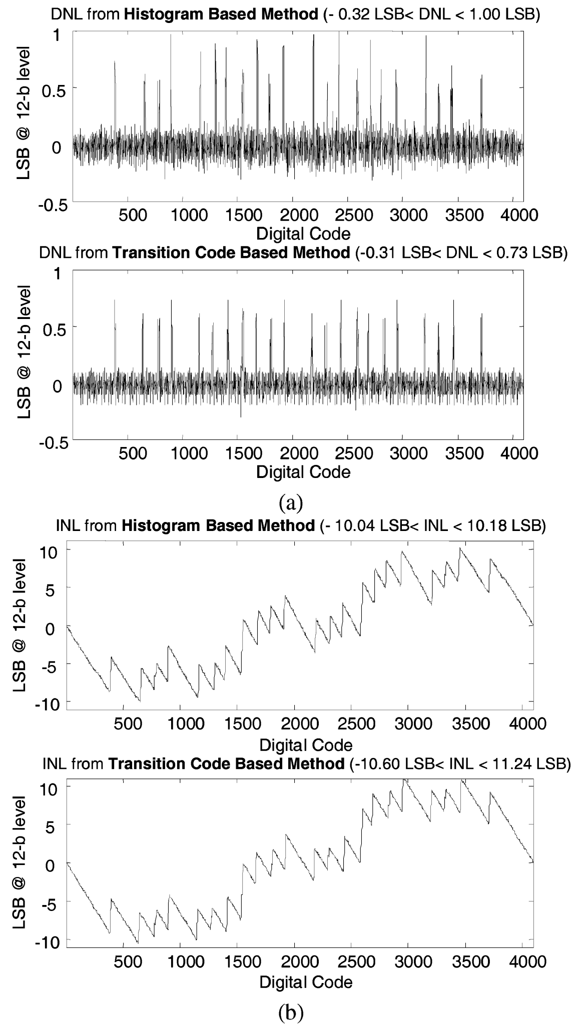

Fig. 23. (a) *Measured* DNL results (b) *Measured* INL results with the conventional histogram method and the proposed transition code based method in the Case 2.

sources, such as the circuit noise and noises from measurement environment, induce additional estimated errors. In a practical chip, additional circuit noises and nonlinearities, which are not included in the behavioral model, would induce additional test error. As a result, the measured test errors are larger than those of the behavioral simulations. Because larger m_{tr_x} values are used, the total required samples for the proposed method is higher than the value in Table I and is about 37938. Compared with the conventional histogram based method, only 9.3% (37938/409600) of the total number of samples is required to achieve comparable test accuracy.

VII. Conclusion

A transition-code based method is proposed to reduce the linearity test time of pipelined ADCs. Pipelined ADC with DEC can tolerate large comparator offset. However, large comparator offset induces large test error in the proposed method. A simple digital DfT circuit was proposed to accurately identify the transition codes corresponding to each pipelined stage. Measured results demonstrate the effectiveness of the transition-code based method. The proposed method can be used to test DEC pipelined ADCs with large nonlinearity and does not require complex algorithmic operations. The proposed method can be further applied to test various types of ADC with DEC, such as pipelined ADCs, cyclic ADCs, and subranging ADCs.

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