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A Design of Linearity Built-in Self-Test for Current-Steering DAC

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Abstract In this paper, a current-mode Built-In Self-Test (BIST) scheme is proposed for on-chip estimating static non-linearity errors in current-steering digital-to-analog converters (DACs). The proposed DAC BIST scheme is designed to verify a 10-bit segmented current-steering DAC, consist of a 5-bit coarse DAC and a 5-bit fine one. This proposed BIST scheme includes a current-mode sample-and-difference circuit to increase the sampling current accuracy and control a current-controlled oscillator (ICO). In addition, only 36 measurements are required by using the selected-code method rather than 1024 measurements for the conventionally-utilized all-code method. Compared to the conventionally-utilized all-code method, about 85-% reduction of test time can be achieved.

Keywords Built-in self-test (BIST) · Digital-to-analog converters (DACs) · Non-linearity errors · Selected-code method

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1 Introduction

The advance of microelectronic technology has made an increasing amount of integrated digital and analog systems on a single chip. Due to this trend and application, the role of the embedded high-performance digital-to-analog converters (DACs) has become more important. Among several architectures of DACs, current-steering DACs are particularly suitable for many applications such as high definition television (HDTV) and global system for mobile communications (GSM) because of the characterizations of fast, linear, and compatible with modern standard CMOS technology. Therefore, characterizing the performance of such current-steering DACs is an important concern. However, the limited controllability and/or observability make the testing difficult and costly. The on-chip built-in self-test (BIST) method which characterizes a DAC's performance is one promising strategy to improve the testability [1, 2, 4, 8, 9, 14, 21].

BIST schemes for testing static errors often adopt three approaches. In [1, 2], the errors of the testing parameters are stored directly and examined to check if any of the errors exceeds the ±0.5-LSB bounds. However, multiple voltage references and a precision gain amplifier, both of which are difficult to get, limit its feasibility. To reduce the number of reference voltages, a variable gain amplifier is used for amplifying different codes to the same level and then compares it with a single reference [21]. However, the matching issues between the resistors and offset error of op amp are problems in practical utilization. Another approach is to use the DAC in a feedback loop [8]. The input to the DAC in the feedback path of a sigma-delta modulator is switched between two codes with the opposite sign. Static errors are inferred from the average value of the output measured by using an up/down counter. However, the

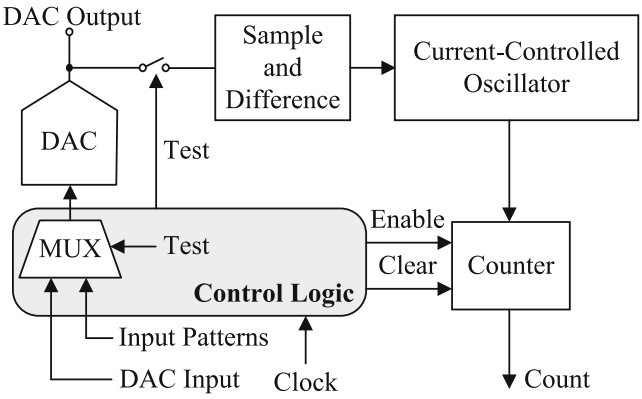

Fig. 1 The blocks of the proposed DAC BIST scheme

generated oscillation frequency may not be enough to achieve reasonable fault coverage. In addition, a high frequency clock is used and static errors are measured in terms of the number of clock cycles. In [9], the time taken by a linear ramp to cross the two consecutive levels is considered as a measure of the step size. There are two problems of this testing procedure. One is that the output voltage of DAC maybe non-monotonic. The other is that the voltage difference between adjacent codes may be too small. The two conditions could prevent comparator from operating correctly. In [4], the DAC output voltage is used for controlling a voltage-controlled oscillator (VCO) and obtaining errors in terms of the frequency shift. However, this scheme required a VCO of which the linearity needs to better than that of the DAC over the entire output range. In [14], a sampled-and-subtract circuit to measure each transition is introduced. Thus, the VCO can just operate in a smaller region rather than the entire DAC output range. Due to the smaller swing of the control voltage, the linearity requirement of the VCO is greatly reduced. But the control voltage of VCO is affected by the open-loop gain of the unity-gain amplifier. An effective BIST scheme based on establishing bounds for the current through each cell is proposed in [15]. But this requires additional current source if different bound is required. In addition, the high-gain preamplifier cannot be employed for prohibiting the circuit from saturation. This may degrade the effectiveness of offset cancellation.

If a DAC is ideal, each output step would be exactly the same size; meaning the output would ramp up in equal increment when input is increased in equal levels. Linearity is one commonly used performance metric for evaluating a DAC. Consequently, differential nonlinearity (DNL) and integral nonlinearity (INL) are often considered. DNL is the degree to which each output step (or code width) varies from the ideal step. INL indicates the deviation of the entire transfer function from the ideal characterization. In this paper, a new current mode BIST scheme which has the capacity of linearity testing for current-steering DAC is proposed. For measuring the current of current-steering DAC directly, a current-controlled oscillator (ICO) is employed in this paper. The feature of selected-code testing of the proposed DAC BIST scheme reduces the test time significantly. A current-mode sample-and-difference circuit is employed not only to directly sample the DAC output current within a small current range but also to control the ICO circuit. The generated oscillating frequency from the ICO will reflect the testing results of the current-steering DAC. In addition, the linearity of the ICO can be improved by setting appropriate bias current sources in the sample-and-difference circuit.

The paper is organized as follows: In Section 2, a new BIST scheme for current-steering DAC linearity testing is proposed. In Section 3, the corresponding circuits for accomplishing the proposed BIST scheme are discussed in

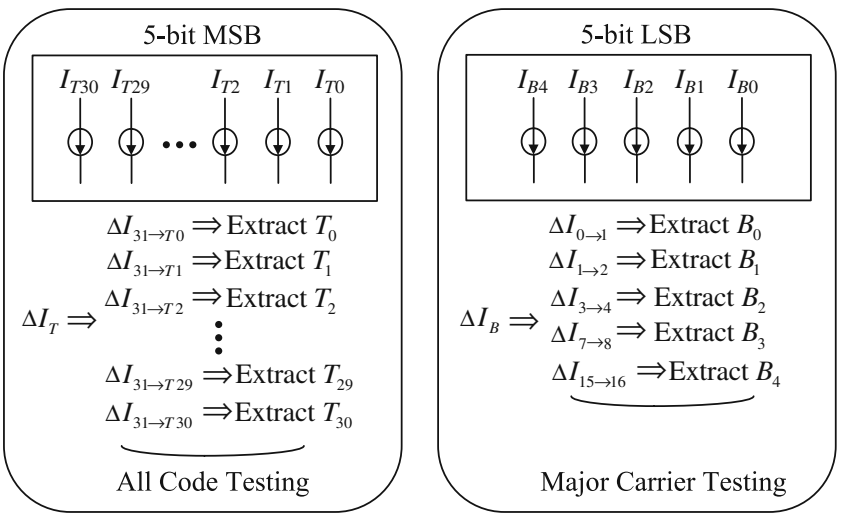

Fig. 2 Modified segmented transitions for a 10-bit (5+5) segmented current-steering DAC

detain, as well as circuit design and simulation. The simulation results are given to demonstrate the effectiveness of the proposed BIST method. Finally, conclusions are given in Section 4.

2 The Proposed BIST Scheme

The proposed BIST scheme is based on selected-code testing which has an advantage of significant test time savings. There are two main kinds of selected-code testing techniques. One is the major carrier method, and the other is the segmented method. The major carrier method usually works on a binary-weighted architectural DAC. Each binary-weighted output of the DAC is measured in turn, and then the all-code output of the DAC will be calculated by using the binary-weighted output. For a 10-bit DAC, this requires only 10 measurements. However, the levels are widely different in magnitude and are difficult to be measured accurately. On the other hand, the segmented method works for DACs which are constructed by different architectures. For example, a 10-bit DAC consists of two portions, a 5-bit coarse DAC and a 5-bit fine DAC. We can test each of the two 5-bit DACs using an all-code testing. This totally requires $2\times2^5=64$ measurements [3, 15]. In this paper, a modified segmented method is proposed. The MSB part is in the thermometer-code architecture while the LSB part is in the binary-weighted architecture. Therefore, the MSB part is measured by all-code testing while the LSB part is performed by the major carrier method. This modified method requires only $(2^5-1)+5$, or 36 measurements for testing a 10-bit current-steering DAC. In addition, the measured current step sizes are very close and are easier to be measured. We also propose a current-mode sample-and-difference circuit, which is composed of switched-current (SI) circuits, to complete the function. In addition, the proposed BIST scheme is designed and simulated for a 10-bit segmented current-steering DAC by using a standard 0.18-μm CMOS process.

The block of the proposed DAC BIST scheme is illustrated in Fig. 1. The modified testing method is based on estimating the current step size. Therefore, the current levels are close in magnitude and are easier to be measured accurately. This is accomplished by using a current-mode sample-and-difference circuit to sample the current step corresponding to the adjacent codes, a current-controlled oscillator to produce a difference frequency which is proportional to the current step size, and a counter to measure the difference frequency.

The testing algorithms of the proposed BIST scheme are described as follows:

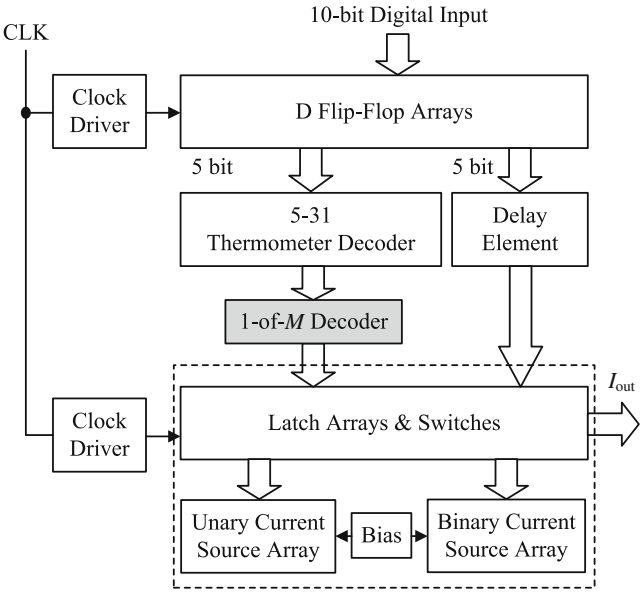

Fig. 3 The architecture of the segmented 10-bit current-steering DAC with an one-of-31 decoder

2.1 Step Size of Modified Segmented Transitions

A 10-bit current-steering segmented DAC DUT is partitioned as a 5-bit MSB part and a 5-bit LSB one in this paper. The 31 current sources are denoted from I_{T0} to I_{T30} in the 5-bit MSB part and the 5 current sources are denoted from I_{B0} to I_{B4} in the 5-bit LSB part in Fig. 2. The transitions which should be measured in the MSB part are denoted as ΔI_T and measured by all-code testing while the transitions which should be measured in the LSB part are denoted as ΔI_B and measured by the major carrier method. Consequently, there will be 31 different ΔI_T and 5 different ΔI_B are required for measurement.

2.2 Reconstruction of the DAC Curve

Once the 36 step sizes are available, the all-code step sizes can be reconstructed. The step sizes of current level are measured and described as follows:

$$\begin{aligned}
&\Delta I_{0\to1} = B_0\\
&\Delta I_{1\to2} = B_1 - B_0\\
&\Delta I_{3\to4} = B_2 - (B_1 + B_0)\\
&\Delta I_{7\to8} = B_3 - (B_2 + B_1 + B_0)\\
&\Delta I_{15\to16} = B_4 - (B_3 + B_2 + B_1 + B_0)\\
&\Delta I_{31\to T0} = T_0 - (B_4 + B_3 + B_2 + B_1 + B_0)\\
&\Delta I_{31\to T1} = T_1 - (B_4 + B_3 + B_2 + B_1 + B_0)\\
&\qquad\qquad\cdots\cdots\\
&\Delta I_{31\to T31} = T_{30} - (B_4 + B_3 + B_2 + B_1 + B_0)
\end{aligned} \tag{1}$$

The current value of the first step size, $\Delta I_{0\to1}$, is a direct measurement of the current B_0 (the step size of the least significant bit). The value of B_1 can be calculated by

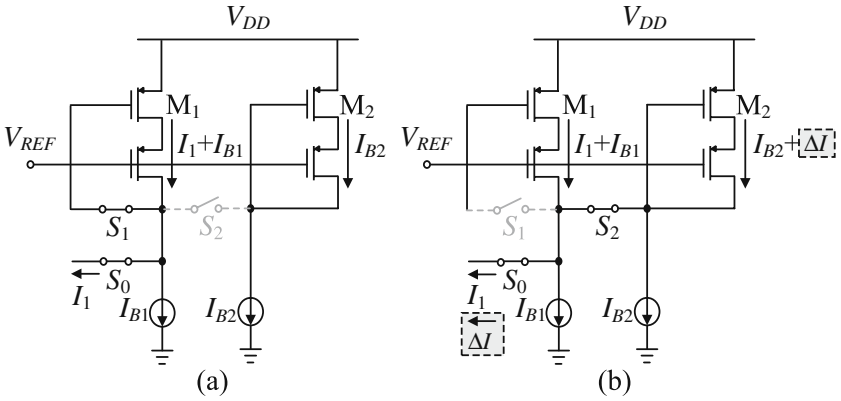

Fig. 4 The basic idea for sampling the current step corresponding to the adjacent codes **a** on phase S_1 and **b** on phase S_2

rearranging the second equation: $B_1 = \Delta I_{1\to 2} + B_0$. In the same way, we can obtain the value of B_2 from $B_2 = \Delta I_{3\to 4} + B_1 + B_0$, and so forth. The complete DAC curve can be reconstructed according to these inductive calculations. The full scale (FS) of the current range of this 10-bit current-steering DAC, consist of a 5-bit MSB and a 5-bit LSB, can be consequently expressed as follows:

$$FS = \sum_{i=0}^{4} 2^{9-i} \times \Delta I_{(2^i-1)\to 2^i} + \sum_{i=0}^{30} \Delta I_{31\to Ti} \tag{2}$$

As a result, the 36 measurements can be utilized to reconstruct the DAC curve.

2.3 Computations of DNL and INL Errors

The need for offset cancellation can be eliminated because the step size is measured in the proposed BIST scheme. This characterization also reduces the area overhead, so it reduces the cost of chip. Therefore, the average value of current step size (I_{LSBa}) after gain correction can be obtained from dividing Eq. 3 by the total number of steps. This can be written as

$$I_{LSBa} = \frac{FS}{2^N - 1} \tag{3}$$

where N is the resolution of the DAC.

After both the offset and gain errors have been removed, DNL is a measure of the deviation of the accrual step size from the theoretical change of 1 LSB. It can be evaluated in LSB units by

$$DNL_j = \frac{\Delta I_{(j-1)\to j} - I_{LSBa}}{I_{LSBa}} = \frac{\Delta I_{(j-1)\to j}}{I_{LSBa}} - 1 \qquad i = 1, 2, ..., 2^N - 2 \tag{4}$$

Then, the estimated values of the DNL can be used for estimating the INL. This is done by accumulating the corrected DNL up to the corresponding code. Therefore, the corresponding INL error expressed in LSB units can be described as follows

$$INL_i = \sum_{j=1}^{i} DNL_j \qquad i = 1, 2, ..., 2^N - 2 \tag{5}$$

As a result, the reconstructed DAC curve can be utilized to evaluate the nonlinearity errors of DAC DUT directly.

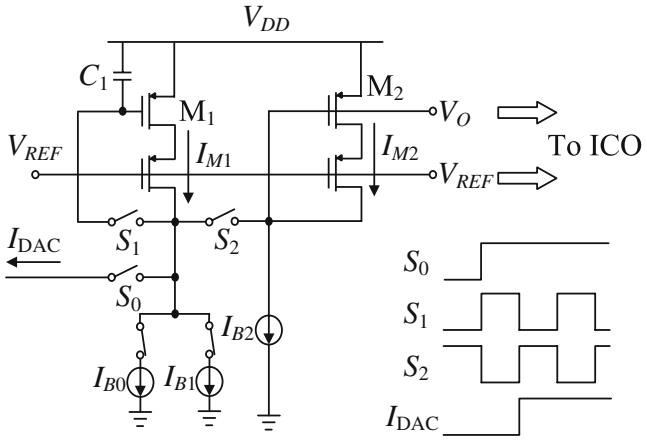

Fig. 5 The sample-and-difference circuit used in the proposed DAC BIST scheme

3 The Circuits for the Proposed BIST scheme

The proposed BIST scheme is accomplished by using a current-mode sample-and-difference circuit to sample the current step corresponding to the adjacent codes, a current-controlled oscillator to produce a difference frequency which is proportional to the current step size, and a counter to measure the difference frequency. The circuit designs and simulation results are detailed in this section to demonstrate the effectiveness of the BIST scheme.

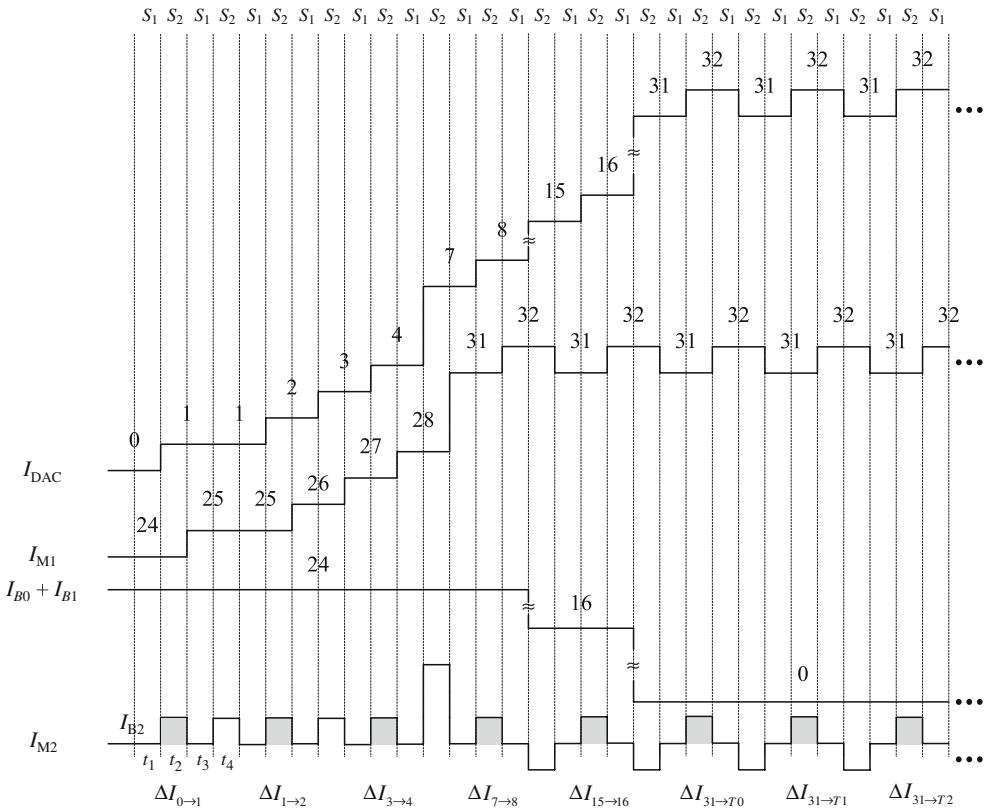

Fig. 6 Timing diagram of the current levels of I_{DAC}, I_{M1}, I_{B0}, I_{B1}, and I_{M2}

3.1 DAC DUT

Simplicity and guaranteed monotonic behavior are advantages of the binary and unary current-steering DAC, respectively. The segmented current-steering DAC combines the advantages of architectures of binary and unary [10, 11, 19]. As a result, a 10-bit current-steering DAC, consists of 5-bit thermometer codes MSBs and 5-bit binary-weighted codes LSBs, is designed as the DAC DUT in this paper. An one-of-*M* decoder is inserted in the DAC and the modified architecture of the DAC is shown in Fig. 3. Only one output of the 31-bit thermometer is high by using this one-of-*M* decoder (*M*=31 in this paper). The measured DNL error of this DAC is ranged from −0.10 LSB to +0.35 LSB and the measured INL error of this DAC is ranged from −0.60 LSB to +0.30 LSB.

3.2 Sample-and-Difference Circuit

The sample-and-difference circuit is designed by the concept of the switch-current (SI) circuit [5–7, 16, 17, 20].The operation of the sample-and-difference circuit used in the proposed DAC BIST scheme is introduced firstly. The basic idea for sampling the current step corresponding to the adjacent codes is illustrated in Fig. 4.

During the testing mode, the switch S_0 is always closed and the current is connected to the SI circuit. On phase S_1, switch S_1 is closed and switch S_2 is open. M_1 is configured in a diode-connected mode and the gate voltage of M_1, V_{g1}, settles to a value which makes the drain current I_{M1} equals to $I_{B1} + I_1$. In addition, M_2 is always in a diode configuration so that I_{M2} equals I_{B2}. Next, assume the memory switch S_1 is open just before the input current change. On phase S_2, switch S_1 is open and switch S_2 is closed. When S_1 is open, I_{M1} remains nearly equal to $I_{B1} + I_1$, assuming the gate voltage V_{g1} doesn't change and the charge injection of S_1 is small. While the input current increases a value of ΔI, the current ΔI is stored in M_2 such that I_{M2} equals $I_{B2} + \Delta I$.

A schematic of the sample-and-difference circuit used in the proposed DAC BIST scheme is illustrated in Fig. 5. This circuit consists of two memory cells (M_1 and M_2), three bias current sources (I_{B0}, I_{B1}, and I_{B2}), and three switches (S_0, S_1, and S_2). The accuracy of this cell circuit is degraded due to two main factors: channel length modulation and charge injection from the switches [5, 7, 20]. The effect of channel length modulation can be reduced by fixing the drain-source voltage of the transistor M_1. The cascode structure is employed to suppress the effect of variation of V_{ds}. In order to reduce the charge injection from the switch S_1, a capacitor (C_1) is placed in the gate of the transistor M_1. The charge injection induces

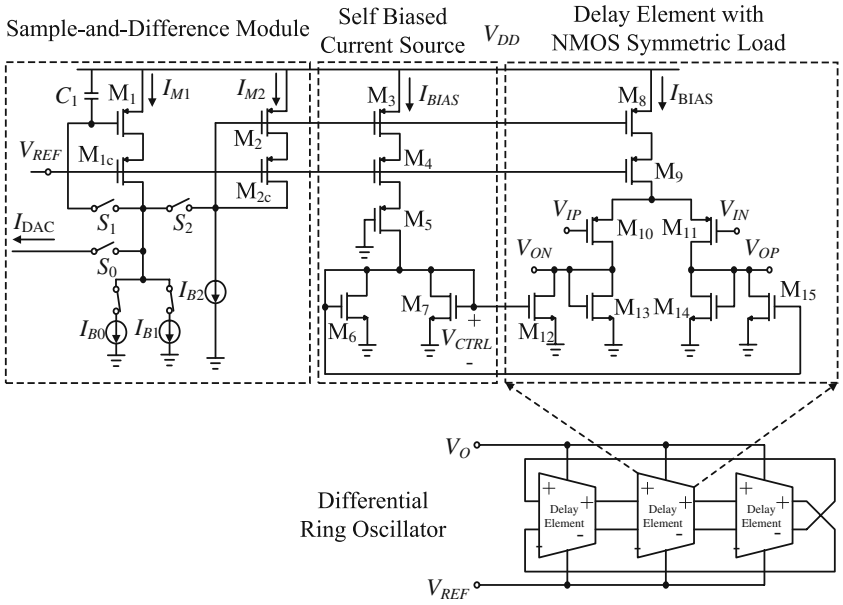

Fig. 7 Schematic of the differential ring oscillator

an error voltage on C_1, hence a relative current error $\Delta I_{\text{error}}/I$ can be expressed as

$$\frac{\Delta I_{\text{error}}}{I} = \sqrt{\frac{\mu C_{ox}(W/L)_{M1}}{2I}}\left[\frac{(WL)_{S1}C_{ox}(V_{GS}-V_t)_{S_1}}{C_1}\right] \quad (6)$$

where C_{ox} is the gate oxide capacitance per unit area, $(WL)_{S1}$ represents the product of the width and length of switch S_1, and $(W/L)_{M1}$ represents the aspect ratio of M_1. Therefore, the relative current error can be reduced by appropriately selecting the aspect ratios of M_1 and S_1, V_{GS}–V_t, and C_1.

In addition, the change in current due to the effect of junction leakage can also be suppressed by increasing the switching frequency f_{sw} by observing Eq. 7 [5, 7, 20].

$$\Delta I = \frac{g_m I_{leak}}{C_1}\frac{1}{f_{sw}} \quad (7)$$

where I_{leak} is the leakage current and g_m is the transconductance of transistor.

The bias current sources, I_{B0}, and I_{B1}, are used for not only generating the bias current for the memory cell of M_1 when the input current, I_{DAC}, is approaching zero but also reducing the range of the current, I_{M1}. In this way, the accuracy can be improved because the variation of drain-source voltage of M_1 is reduced. In order to reduce the errors of the two bias current sources, the minimum required areas of the bias current sources, I_{B0}, and I_{B1}, and the unit current cell which constructs the current-steering DAC are both determined by the mismatch equations shown below [12, 13].

$$WL = \left(A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right)\Big/ 2\left(\frac{\sigma(I)}{I}\right)^2 \quad (8)$$

The values of the mismatch parameters, A_β and A_{VT}, are dependent on the microelectronic fabrication technology. The Monte Carlo simulation illustrates that the standard deviation of the unit current ($\sigma(I)/I$) is limited to be about 0.5% for achieving a 99.7-% yield [18].

During testing mode, the current range of I_{DAC} is between zero and $32I_{LSB}$ if the value of the unit current is denoted as I_{LSB}. To reduce the current variation of the transistor M_1, two current sources, $I_{B0}=16I_{LSB}$ and $I_{B1}=8I_{LSB}$, are utilized as mentioned above. When the current step of $\Delta I_{0\to1}$, $\Delta I_{1\to2}$, $\Delta I_{3\to4}$, and $\Delta I_{7\to8}$ are measured, the two current sources (I_{B0} and I_{B1}) are both utilized to ensure the total current value are near the $32I_{LSB}$. The corresponding current levels of I_{DAC}, I_{M1}, I_{B0}, I_{B1}, and I_{M2} for detecting $\Delta I_{0\to1}$, $\Delta I_{1\to2}$, $\Delta I_{3\to4}$, and $\Delta I_{7\to8}$ during the test process are illustrated in Fig. 6.

During the period denoted as t_1, the drain current I_{M1} is equals to $I_{B0} + I_{B1}=24I_{LSB}$ and I_{M2} is equal to I_{B2}. During the period denoted as t_2, I_{M1} is nearly equal to $24I_{LSB}$ while I_{M2} is equal to $I_{B2} + \Delta I = I_{B2} + 1I_{LSB}$ ($\Delta I = 1I_{LSB}$) because I_{DAC} is equal to $1I_{LSB}$. During the period denoted as t_3, I_{M1} is equal to $25I_{LSB}$ and I_{M2} is equal to I_{B2} again. During the period denoted as t_4, I_{M1} is nearly equal to $25I_{LSB}$ and I_{M2} is equal to $I_{B2} + \Delta I$ ($\Delta I = 1I_{LSB}$). Similarly, one current source, $I_{B0} = 16I_{LSB}$, is employed to measure the current step of $\Delta I_{15\to16}$ to ensure the total current value are near the $32I_{LSB}$. When the current steps of thermometer part are

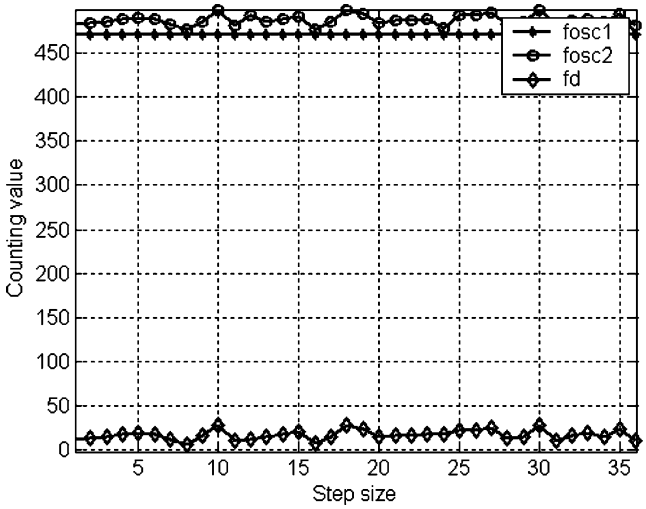

Fig. 8 The counting value with a 10-% mismatch in DAC

measured, no current source is employed because the thermometer current value is the $32I_{LSB}$. As a result, the error from the different drain-source voltage of the transistor M_1 can be suppressed and the required step sizes can be measured. The concept for detecting the current steps of $\Delta I_{15\to16}$, $\Delta I_{31\to T0}$, $\Delta I_{31\to T1}$, and $\Delta I_{31\to T2}$ are also illustrated in Fig. 6.

3.3 ICO

The drain current of M2, I_{M2}, is replicated to the bias current sources of the ICO. During phase S_1, a frequency f_{osc1} is generated from the ICO. Similarly, a frequency f_{osc2} is generated from the ICO during phase S_2. The difference frequency $f_{osc2} - f_{osc1}$ is proportional to the current step size. In addition, the measurement accuracy can be maintained over the entire output range because the same region of operation of ICO is used in the proposed BIST scheme.

The schematic diagram of the differential ring oscillator is shown in Fig. 7. It is composed of delay element with NMOS symmetric load, self bias current source, and sample-and-difference circuit. The symmetric load provides linear control over load resistance. The frequency of oscillation can be written as

$$f_{osc} = \frac{I_{BIAS}}{2 \cdot N \cdot V_{CTRL} \cdot C_{eff}} \tag{9}$$

where N is the number of delay stage, V_{CTRL} is proportional to the change of I_{BIAS}, and C_{eff} is the total capacitance at the output of delay element.

The relationship between the current of $I_{D6,7}$ and V_{CTRL} can be expressed in Eq. 10.

$$I_{D6,7} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{6,7}(V_{CTRL} - V_{th})^2 \tag{10}$$

where V_{th} and $\mu_n C_{ox}$ are dependent on the microelectronic fabrication technology.

When the value of I_{BIAS} is increased, the currents flowing through M_6 and M_7 are also increased. Next, the value of V_{CTRL} is also increased by observing Eq. 10. Consequently, the I_{BIAS} and V_{CTRL} are changed in the same direction. The frequency of oscillation is proportional to I_{BIAS} while reversely proportional to V_{CTRL} by observing Eq. 9. Because I_{BIAS} and V_{CTRL} are changed in the same direction, their effects on the frequency of oscillation will be canceled.

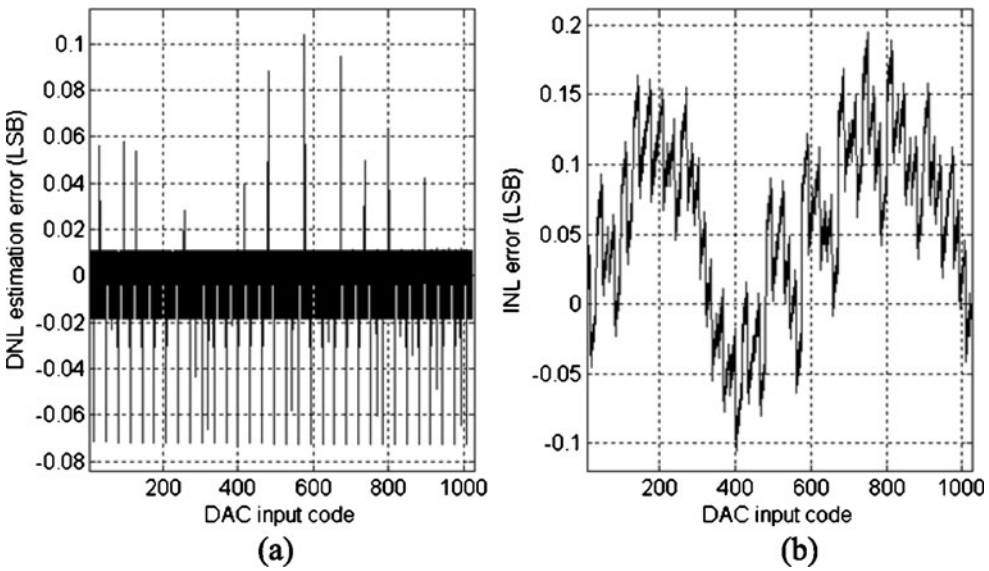

Fig. 9 **a** The DNL estimating error and **b** The INL estimating error with a 10-% mismatch in DAC

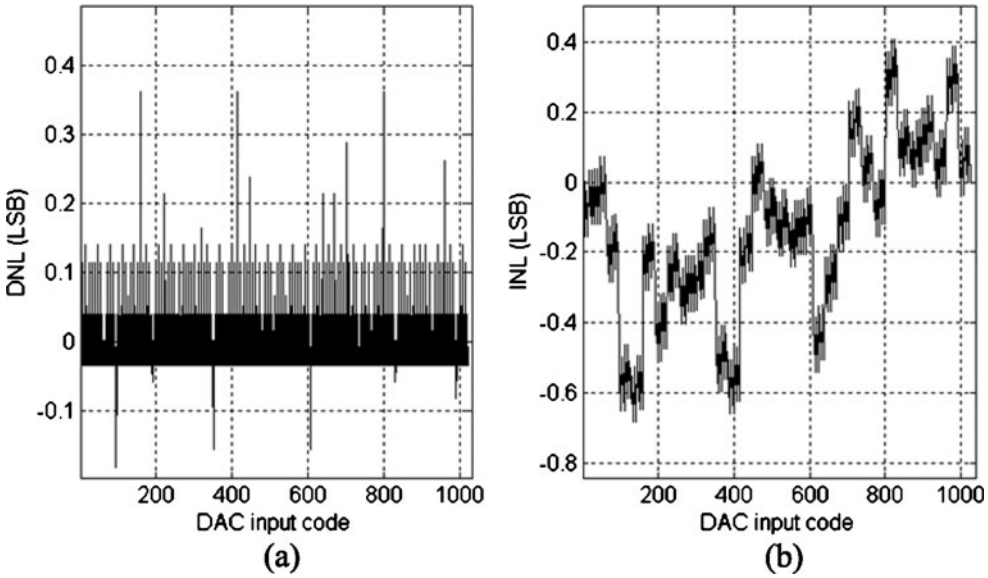

Fig. 10 **a** The DNL error and **b** The INL for the segmented 10-bit current-steering DAC

3.4 Frequency Measurement, Total Test Time, and Counter

The ICO frequency difference corresponding to a current step size can be written as

$$f_D = f_{osc2} - f_{osc1} \tag{11}$$

If a K-bit measurement resolution is required, the test period T_{test} can be written as

$$T_{test} = \frac{2^K}{f_{osc2} - f_{osc1}} \tag{12}$$

In fact, the test precision could be increased by simply increasing the test period [4].

For an N-bit segmented current-steering DAC, the B LSBs are implemented using a binary architecture while the (N–B) MSBs are implemented in a thermometer way. Depending on the modified segmented method, the total number of step sizes ($N_{\text{Step size}}$) can be measured and written as

$$N_{Stepsize} = (2^{N-B} - 1) + B \tag{13}$$

For example, there will be 36 step sizes ($N_{\text{Step size}}$=36) when N=10 and B=5.

Therefore, the total test time (T_{total}) can be expressed as

$$T_{total} = 4 \times N_{Stepsize} \times T_{test} \tag{14}$$

A constant of 4 is used in Eq. 14 because 4 test periods are required to determine a step size by observing Fig. 6. For example, the total test time is equal to 144 test periods (T_{total}=144×T_{test}) when N=10 and B=5.

As a result, the total test time is equal to 144 test periods for testing a 10-bit current-steering DAC in this paper. Compared to the conventionally-utilized all-code method, about 85-% (i.e. 1–144/1024) reduction of testing time can be achieved.

In addition, the frequency f_{os1} will be less than the frequency f_{os2} if the DAC is guaranteed to be monotonic. In other word, the number of cycles of the frequency f_{osc2} will be larger than that of the frequency f_{osc1}. Therefore, the required length of a counter (*Count*) will be determined by the frequency f_{osc2} and can be written as

$$Count = f_{osc2} \times T_{test} \tag{15}$$

The required length of a counter is less than 512 in this paper by performing the simulation. Therefore, a 9-bit counter is used for converting the frequency to a number of cycles in the proposed DAC BIST scheme.

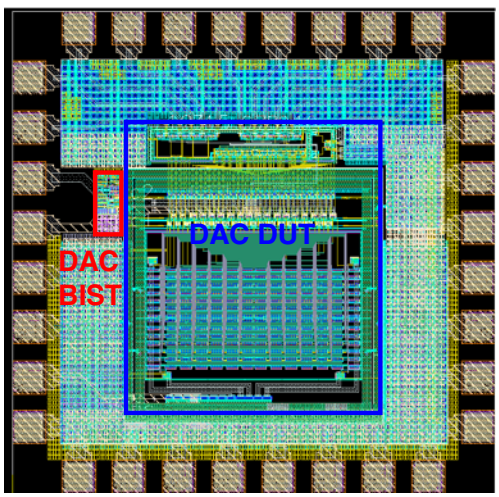

Fig. 11 The layout of the BIST scheme and DAC DUT

Table 1 Summary of the chip

Specifications	Results
Technology	0.18-μm CMOS technology
Resolution	10 bits
Measured DNL/Estimated DNL	−0.10 LSB ~ +0.35 LSB / −0.17 LSB ~ +0.36 LSB
Measured INL/Estimated INL	−0.6 LSB ~ +0.30 LSB / −0.67 LSB ~ +0.40 LSB
Supply voltage	1.8 V
Active area	0.63 mm × 0.72 mm=0.45 mm^2
BIST area	0.07 mm×0.15 mm=0.0105 mm^2
Chip area	1.16 mm×1.16 mm=1.34 mm^2

3.5 Simulations

The proposed DAC BIST scheme is composed of the above mentioned current-mode sample-and-difference circuit to sample the current step corresponding to the adjacent codes, a current- controlled oscillator to produce a difference frequency which is proportional to the current step size, and a counter to measure the difference frequency.

At first, the DAC BIST scheme is simulated for a segmented 10-bit DAC with a 10-% mismatch. The 10-% mismatch indicates that the variation of current is within 10% of the ideal value with a probability of 99.7%. The count difference for 36 step sizes is shown in Fig. 8. The curve in circle shows the counting value corresponding to f_{osc2}, the curve in asterisk shows the counting value corresponding to f_{osc1}, and the curve in diamond shows the counting value corresponding to f_D defined in Eq. 10.

By applying the simulated data of the observed counting difference, we can estimate the DNL and INL of the DAC DUT by using the proposed BIST scheme. We also calculate the DNL and INL using the theoretical equation in [3]. Comparing the estimated nonlinearity with the theoretically predication, their differences (i.e. estimation error) are small. The DNL and INL estimating errors which are shown in Fig. 9 are around to 0.1 LSB and 0.2 LSB, respectively. Therefore, the estimated nonlinearity shows good agreement with the theoretically prediction.

Next, the proposed DAC BIST scheme is also applied to the segmented 10-bit current-steering DAC DUT described in Section 3.1. The estimated DNL is ranged from −0.17 LSB to +0.36 LSB and the estimated INL is ranged from −0.67 LSB to +0.40 LSB. The estimated DNL and INL, which are shown in Fig. 10, show good agreement with the results obtained in Section 3.1.

The layout of the proposed DAC BIST scheme and DAC DUT are shown in Fig. 11. The area required for the proposed DAC BIST scheme is about 0.0105 mm^2.

The details of the chip are summarized in Table 1. The area overhead of the proposed DAC BIST scheme is about 2.4% to the active area of the DAC DUT. In [15], the BIST area overhead is about 11.1% to the active area of the DUT. Compared to [15], the proposed BIST scheme shows better area efficiency.

4 Conclusion

In this paper, a current-mode BIST scheme for current-steering DACs' linearity testing is proposed. In the proposed BIST scheme, a current-mode sample-and-difference circuit is used not only to sample the DAC output current directly within a small range but also to control the ICO. In addition, the linearity of ICO is also improved by using the proposed sample-and-difference circuit. The proposed test scheme is capable of estimating the static parameters, including non-monotonic behavior, DNL, and INL. Simulation results of a 10-% mismatch show that the maximum deviation between the estimated DNL and the theoretically predicted one is around 0.1 LSB. Also, the maximum deviation between the estimated INL and the theoretically predicted one is round to 0.2 LSB. In addition, the BIST scheme is also applied to a segmented 10-bit current-steering DAC to verify its effectiveness. Employing the proposed BIST scheme, test time and cost are greatly reduced because of the feature of modified segmented method. Only 36 measurements are required rather than 1024 measurements in the conventional-utilized all-code method for testing a 10-bit current-steering DAC. The total test time is equal to 144 test periods for testing a 10-bit current-steering DAC. Compared to the conventionally-utilized all-code method, about 85-% reduction of testing time can be achieved.

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