PAPER

A Low-Power Mixed-Architecture ADC with Time-Interleaved Correlated Double Sampling Technique and Power-Efficient Back-End Stages

Jin-Fu LIN[†a)], ***Nonmember and*** **Soon-Jyh CHANG**[†], ***Member***

SUMMARY In this paper, two techniques for implementing a low-power pipelined analog-to-digital converter (ADC) are proposed. First, the time-interleaved correlated double sampling (CDS) technique is proposed to compensate the finite gain error of operational amplifiers in switched-capacitor circuits without a half-rate front-end sample-and-hold amplifier (SHA). Therefore, low-gain amplifiers and the SHA-less architecture can be used to effectively reduce power consumption of a pipelined ADC. Second, the back-end pipelined stages of a pipelined ADC are implemented using a low-power time-interleaved successive approximation (SA) ADC rather than operational amplifiers to further reduce the power consumption of the proposed pipelined ADC. A 9-bit, 100-MS/s hybrid pipelined-SA ADC is implemented in the TSMC 0.13 μm triple-well 1P8M CMOS process. The ADC achieves a spurious free dynamic range (SFDR) of 62.15 dB and a signal-to-noise distortion ratio (SNDR) of 50.85-dB for 2-MHz input frequency at a 100-MS/s sampling rate. The power consumption is 21.2 mW from a 1.2 V supply. The core area of the ADC is 1.6 mm^2.

key words: *analog-to-digital converter (ADC), data converter, correlated double sampling (CDS), time-interleaved, successive approximation (SA) ADC*

1. Introduction

High-resolution low-power ADCs are extensively employed in display and imaging systems. For example, in high-definition TV (HDTV) applications, 8–10 bits and 75–100 MS/s high-speed data converters are usually required as high-performance video digitizers [1], [2]. The pipelined ADC is a popular selection among various ADC architectures for video applications due to its high-speed, high-accuracy, and low-power capabilities. With advances in CMOS technology, the supply voltage and the intrinsic impedance of transistors have been reduced for maintaining circuit reliability and enhancing device speed. This trend imposes stringent challenges on CMOS operational amplifier (opamp) designs. For example, long-channel devices are usually needed to meet the high-gain requirement. However, such a design loses the high-speed capability of short-channel devices provided by the advanced CMOS process. Moreover, reduced supply voltage limits the linear output range of an opamp and confines the available opamp structures. Hence, instead of employing high-gain opamps, it is preferred to exploit low-power and low-gain amplifiers in low-power pipelined ADCs. Errors caused by the finite opamp gain are then compensated with novel techniques. Many digital calibration techniques have been proposed to alleviate the finite gain error when low-gain amplifiers are used in switched-capacitor (SC) circuits [3], [4]. However, these techniques are complicated and may suffer from noise coupling. A more innovative technique, that is, the zero-crossing based design, uses digital circuits to replace high-gain opamps [5]. Correlated level shifting (CLS) [6] was proposed to deal with the problems of existing CDS techniques, but it cannot reduce the dc offset and flicker noise of applied circuits.

The time-shifted correlated double sampling technique (TS-CDS) is an effective, simple analog technique for compensating the finite opamp gain error without sacrificing power consumption or operating speed of SC circuits [7]. However, the TS-CDS technique requires a power-hungry half-rate front-end sample-and-hold amplifier (SHA). This paper proposes a time-interleaved CDS (TI-CDS) technique to eliminate the half-rate SHA while still preserving the function of the finite opamp gain error compensation in the CDS technique. The low-power potential of the CDS technique can thus be further strengthened. In addition, the back-end pipelined stages of the proposed ADC are implemented using a time-interleaved successive approximation (SA) ADC rather than a conventional opamp-based architecture. This architectural arrangement further reduces the power consumption of a pipelined ADC.

The rest of this paper is organized as follows. Section 2 briefly describes the proposed architecture. Section 3 and Sect. 4 introduce the concept and related design issues of the proposed TI-CDS technique, respectively. Section 5 presents the design considerations of the SHA-less architecture. The architectural selection and detailed implementation of the power-efficient back-end SA ADC are explained in Sect. 6 and Sect. 7, respectively. Finally, the experimental result is discussed in Sect. 8, and conclusion is made in Sect. 9.

2. Architecture of the Proposed Pipelined ADC

The architecture of the proposed 9-bit pipelined ADC is illustrated in Fig. 1. The front-end pipelined stages adopt the 1.5-bit/stage architecture to achieve high-speed operation and simple circuit implementation. The prior tech-

Manuscript received April 18, 2010.
Manuscript revised August 16, 2010.
[†]The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan.
a) E-mail: doogg@sscas.ee.ncku.edu.tw
DOI: 10.1587/transele.E94.C.89

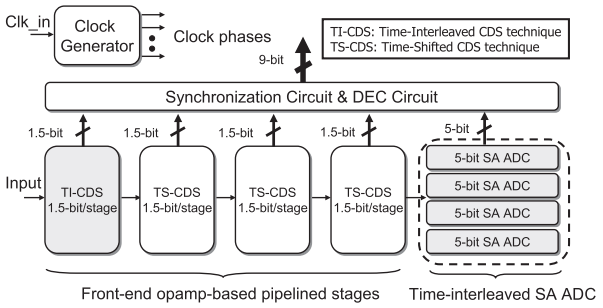


Fig. 1 Proposed architecture of a 9-bit pipelined ADC.

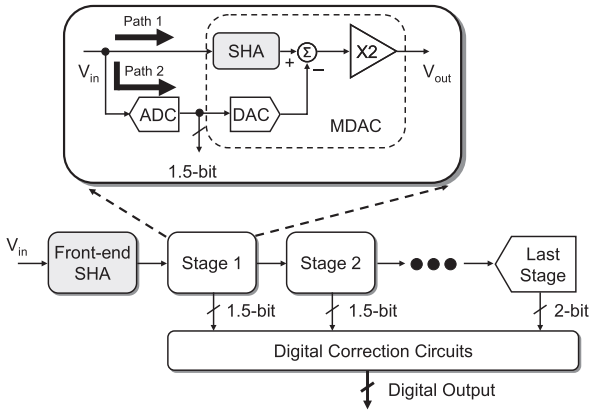


Fig. 2 Typical 1.5-bit/stage pipelined ADC architecture.

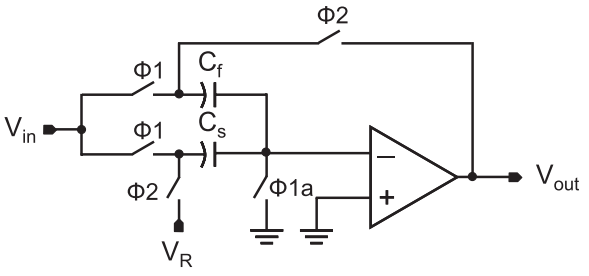


Fig. 3 Typical 1.5-bit/stage MDAC architecture.

nique, TS-CDS, can compensate the finite opamp gain error in switched-capacitor circuits without suffering the double loading problem [7]. However, when the first pipelined stage adopts the TS-CDS technique, a half-rate SHA is required. The proposed TI-CDS technique can preserve the merit of the opamp gain error compensation in the CDS technique while removing the half-rate SHA. Therefore, to eliminate the power-hungry SHA, the first pipelined stage uses the proposed TI-CDS instead of the TS-CDS technique. The latter stages still adopt the TS-CDS technique. This architectural arrangement combines TI-CDS and TS-CDS techniques to achieve the optimum speed and power performance. As a result, the front-end opamp-based pipelined stages can be implemented with low-gain and low-power amplifiers.

The SHA-less architecture is adopted in the proposed pipelined ADC. However, the first pipelined stage must be well configured to solve the timing-mismatch problem that exists in the SHA-less architecture [8]–[11]. The details about this will be addressed in Sect. 5.

For further power saving, the design of the back-end pipelined stages uses a low-power time-interleaved SA ADC instead of conventional opamp-based pipelined stages. The DAC network in an SA ADC usually grows exponentially with resolution, which causes heavy loading for the preceding pipelined stage in the proposed architecture. Therefore, the resolution arrangement between the front-end opamp-based pipelined stages and the back-end stages implemented with a time-interleaved SA-ADC must be well determined to ensure the minimum power consumption of the whole ADC. This issue is discussed in Sect. 6.

3. Correlated Double Sampling Technique

3.1 Conventional Pipelined ADC Architecture

A typical pipelined ADC with a 1.5-bit/stage architecture is shown in Fig. 2. With digital error correction (DEC), the offset requirement of comparators in sub-ADCs is greatly reduced. Therefore, in a pipelined ADC, the most critical circuit is the multiplying digital-to-analog converter (MDAC), whose accuracy dominates the accuracy of an ADC.

A typical 1.5-bit/stage MDAC architecture is implemented with an SC circuit, as shown in Fig. 3. During the sampling phase (ϕ_1/ϕ_{1a}), the input signal is sampled by C_s and C_f. During ϕ_2, C_f is connected to the opamp output and C_s is connected to the DAC output V_R. Based on the charge conservation theorem, the output of the MDAC is:

$$V_{out} = \left(\frac{C_s + C_f}{C_f}\right) V_{in} - \left(\frac{C_s}{C_f}\right) V_{ref} + e \tag{1}$$

where V_{in} is the sampled input signal; V_R is $\{0, \pm V_{ref}\}$, which depends on conversion results of the sub-ADC; and the final term is:

$$e = \frac{-1}{A}\left(1 + \frac{C_s}{C_f}\right) V_{out} \tag{2}$$

When capacitors C_s and C_f are perfectly matched, this error term (e) is only caused by the finite gain (A) of the amplifier. In a conventional pipelined ADC, a high-gain opamp is required to reduce this error. In practice, the first 1.5-bit/stage pipelined stage in a 10-bit pipelined ADC normally requires an opamp with over 70-dB dc gain. Such a high-gain opamp is usually implemented using either cascoded or gain-boosted structures which are power-hungry and have small signal swing. Correlated double sampling (CDS) was developed to deal with this problem.

3.2 Conventional CDS Technique [12]

The CDS technique is extensively employed to compensate the finite opamp gain error and dc offset in SC circuits [12], [13]. Many variations of the CDS technique

have been developed for specific applications [12]. Most of them impose limited bandwidth requirement on input signal for compensating the finite opamp gain error. In [13], a wideband CDS technique, here refer to as "the conventional CDS technique" to distinguish it from time-shifted and time-interleaved CDS techniques which will be illustrated in the next two sub-sections, was proposed. The circuit diagram of a 1.5-bit/stage MDAC with the conventional CDS technique is shown in Fig. 4. One full operation requires three clock phases. In the sampling phase, the preliminary set of capacitors ($C_{s,p}, C_{f,p}$) and the main set of capacitors ($C_{s,m}, C_{f,m}$) sample the input signal simultaneously. Then, in the preliminary amplifying phase, $C_{s,p}$ and $C_{f,p}$ are configured as an

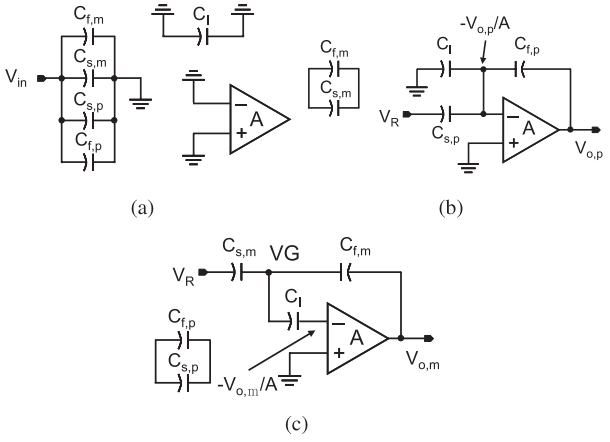


Fig. 4 Circuit diagram of a 1.5-bit/stage MDAC with the conventional CDS technique. (a) Sampling phase ($\phi 1$) (b) Preliminary amplifying phase ($\phi 2$) (c) Main amplifying phase ($\phi 3$).

MDAC topology. The finite gain error ($-V_{o,p}/A$) is stored with C_I. In the main amplifying phase, the desired error-canceled residue output is obtained. Capacitor C_I acts as an "*error-stored battery*" and is connected between the negative input of the opamp and the *VG* node. With this mechanism, the node *VG* approaches the ideal virtual ground. Assuming $C_{s,p} = C_{s,m} = C_s$ and $C_{f,p} = C_{f,m} = C_f$, the error term of MDAC with the conventional CDS technique is:

$$e \approx \frac{-1}{A^2}\left(1+\frac{C_s}{C_f}\right)\left[\left(1+\frac{C_s+C_I}{C_f}\right)V_{o,m} - \left(\frac{C_I}{C_f}\right)V_{o,p}\right] \quad (3)$$

where $V_{o,m}$ is the main amplified output and $V_{o,p}$ is the preliminary amplified output. The error term is inversely proportional to A^2, which indicates that the conventional CDS technique can equivalently double the opamp gain in decibel. Nevertheless, in practice, the effectiveness of the conventional CDS technique is degraded by additional parasitic capacitors and by the difference between $V_{o,m}$ and $V_{o,p}$. Moreover, there are two intrinsic problems in this technique: 1) it requires three clock phases, and 2) it causes double loading for the preceding circuit. These disadvantages inhibit the use of the conventional CDS technique in high-speed or low-power pipelined ADC designs.

3.3 Time-Shifted CDS Technique [7]

The time-shifted CDS technique (TS-CDS) was proposed to resolve the aforementioned problems in the conventional CDS technique by re-arranging the timing scheme [7]. The circuit diagram of TS-CDS is shown in Fig. 5. Its complete operation requires only two clock phases. In the first phase (ϕ_1), $C_{f,m}$ and Cs, m sample the main pipelined input $V_{in,m}$

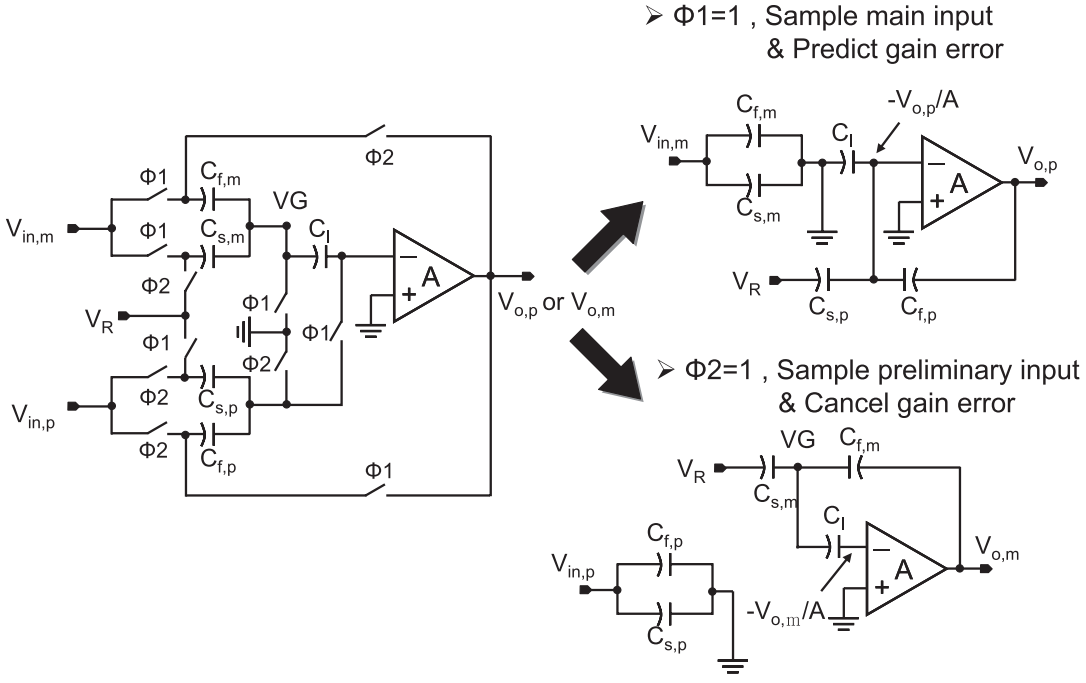
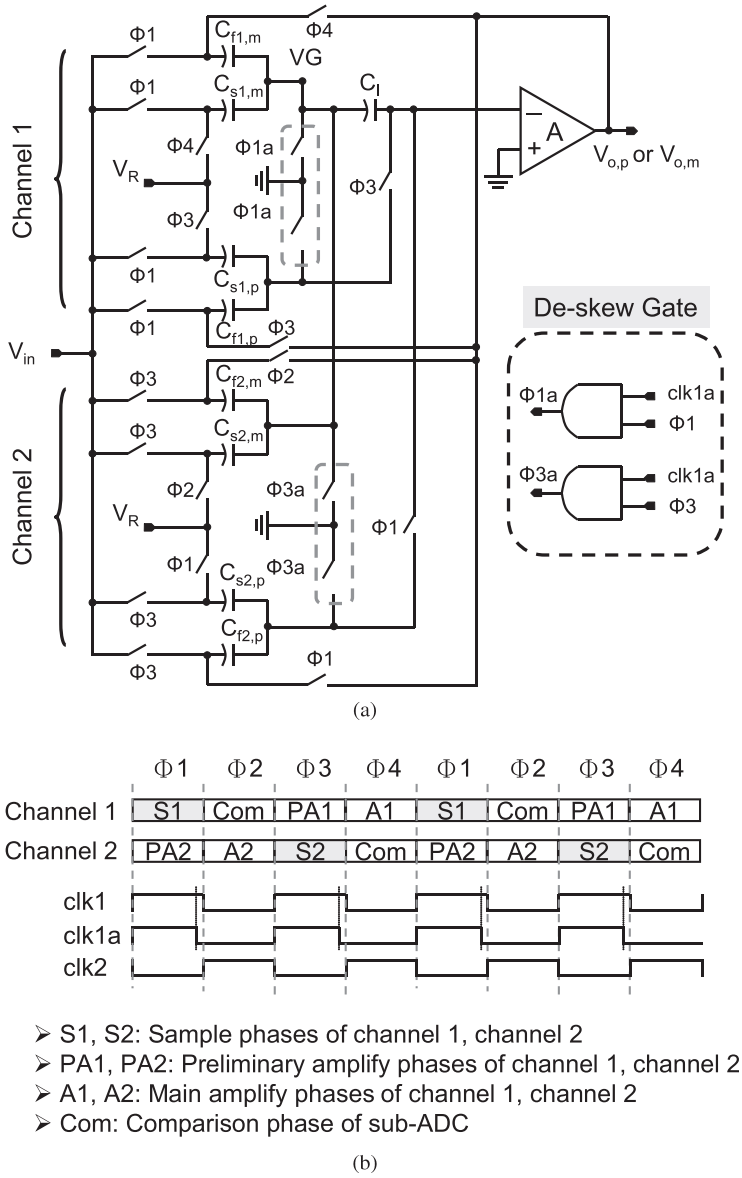


Fig. 5 Circuit diagram of a 1.5-bit/stage MDAC with the time-shifted CDS technique.



(a)

(b)

Fig. 6 (a) Circuit diagram of the proposed time-interleaved CDS technique. (b) Its timing diagram.

which is the desired error-compensated residue output of the preceding pipelined stage when the TS-CDS is used for every pipelined stage. At the same time, $C_{s,p}$ and $C_{f,p}$ perform MDAC amplification of the previous sampled input signal to predict and store the finite gain error on C_I. In the second phase (ϕ_2), C_I is connected between the node VG and the negative input of the opamp to compensate gain error in the main path. At the same time, a new input signal of the preliminary path, which is the residue output contained the finite opamp gain error of the preceding pipelined stage, is sampled by $C_{s,p}$ and $C_{f,p}$. The main and preliminary sets of capacitors are used to sample different input signals in different phases. As a result, only one set of capacitors loads the preceding pipelined stage, which mitigates the double loading problem existed in the conventional CDS technique.

However, the different input signals of two SC paths, $V_{in,m}$ and $V_{in,p}$, must be maintained at the same value to ensure the error-cancellation effectiveness of the TS-CDS technique. Consequently, a front-end SHA operated at a half sampling rate is required for the first pipelined stage with the TS-CDS technique. This SHA usually consumes a large amount of power. Moreover, due to the finite gain error, there is a certain voltage difference between $V_{in,m}$ and $V_{in,p}$. This difference is gradually accumulated in back-end pipelined stages, which not only degrades the effectiveness of TS-CDS but also induces an additional signal-dependent offset in the back-end pipelined stages. When this additional signal-dependent offset exceeds the tolerable range of the digital error correction, the circuit performance will be degraded seriously. Therefore, in order to avoid this situation, the number of pipelined stages with the TS-CDS technique has to be limited.

3.4 Proposed Time-Interleaved CDS Technique

To eliminate the half-rate SHA, the time-interleaved CDS (TI-CDS) is proposed. The TI-CDS adopts the conventional CDS technique as the core circuit and uses a time-interleaved architecture, as shown in Fig. 6. The single-ended diagram is used for clear explanation, and the fully differential circuits are implemented in this work. This technique is based on a similar concept to that used in our previous work [14], in which the TI-CDS technique is employed to implement the front-end SHA. The preliminary and main SC paths sample the input signal at the same time, which is the same as the conventional CDS technique. Therefore, a power-hungry half-rate SHA, which is employed to keep $V_{in,m}$ and $V_{in,p}$ in the TS-CDS technique the same value, is no longer required. Therefore, the power consumption of the proposed ADC can be reduced substantially. Moreover, no additional signal-dependent offset is induced.

Two channels and four clock phases are needed to complete the whole TI-CDS operation. Two channels share a single opamp. In Fig. 6, four pairs of capacitors, ($C_{s1,p}$, $C_{f1,p}$), ($C_{s1,m}$, $C_{f1,m}$), ($C_{s2,p}$, $C_{f2,p}$) and ($C_{s2,m}$, $C_{f2,m}$), are required to implement the MDAC circuit with the proposed TI-CDS technique. In ϕ_1 phase, the SC network of channel 1 samples the input signal $V_{in}[n]$ with $C_{s1,p}, C_{f1,p}, C_{s1,m}$, and $C_{f1,m}$, and that of channel 2 performs the preliminary amplification, which is used to store the finite opamp gain error corresponding to the previous sampled input signal $V_{in}[n-1]$. In ϕ_2 phase, data conversion of the sub-ADC for the sampled input signal is fulfilled, and channel 2 completes the main amplification of the previous input sample. In ϕ_3 phase, preliminary amplification of the sampled input signal is done in channel 1. At the same time, the sampling of the next input sample $V_{in}[n+1]$ is completed in channel 2. Finally, in ϕ_4 phase, the main amplification of the sampled input signal is performed in channel 1, and a comparison of the sub-ADC for the next input signal is completed. Four clock phases, i.e. sample (S), compare (Com), preliminary amplify (PA), and main amplify (A) phases, are required for two channels in the proposed TI-CDS technique. Digital output of the sub-ADC and the corrected residue output corresponding to each sampled input are produced every two clock phases. The drawback of the longer conversion time in the conventional CDS technique can be overcome by using such a time-interleaved operation. Moreover, using four clock phases instead of three phases leads to a timing advantage which makes early comparison possible [15]. One phase is preserved for the conversion of sub-ADCs. Therefore, the comparison speed of the sub-ADC is not critical. On the contrary, a short non-overlapped clock interval is usually arranged as the conversion time of sub-ADCs in a conventional pipelined ADC, which shortens the available conversion time of sub-ADCs. As a result, in the pipelined stage with the proposed TI-CDS technique, the speed requirement of sub-ADCs can be relaxed, and consequently the power consumption of sub-ADCs can be reduced.

4. Design Issues for the Proposed Time-Interleaved CDS Technique

4.1 Design Issues for the Time-Interleaved Architecture

In time-interleaved architectures, three main channel-mismatch sources normally exist [16]. The design considerations for channel-mismatch problems in the proposed TI-CDS technique are described as follows:

1. *Timing Mismatch*: This issue is mainly caused by clock skew among sampling clocks of time-interleaved paths. This problem can be mitigated when the sampling instants of multiple channels are determined by a single control clock of an additional "de-skew switch" [17]. However, the charge of the parasitic capacitance at the floating node may distort the sampling charge of each channel. To solve this problem, local "de-skew gates" rather than the de-skew switch are proposed to produce the sampling clocks of two time-interleaved channels (ϕ_{1a} and ϕ_{3a}) in this work, as shown in Fig. 6(a). The falling edges of ϕ_{1a} and ϕ_{3a} are determined by a single clock, clk1a. Clock-skew between ϕ_1 and ϕ_3 due to a physical routing mismatch can be absorbed using this circuit implementation. Local de-skew gates must be placed near the switches controlled by ϕ_{1a} and ϕ_{3a} to ensure minimum timing skew.
2. *Gain Mismatch*: The gain mismatch is mainly contributed by the capacitor mismatch and the mismatch of the finite opamp gain error in the time-interleaved architecture. In the proposed architecture, capacitor mismatch is the only source of gain mismatch because two CDS paths share a single opamp. In general, capacitor mismatch can be well-controlled to achieve 10-bit accuracy with careful layout technique.
3. *Offset Mismatch*: Two time-interleaved paths share an opamp and the CDS technique has an inherent offset-cancellation function. As a result, the offset of opamp does not cause any channel mismatch in this architecture.

4.2 Design Issues for the Double Loading Problem

The proposed TI-CDS technique has the same double loading problem as the conventional CDS technique. However, in the proposed architecture, the TI-CDS technique is only applied to the MDAC design in the first pipelined stage, and the TS-CDS technique is employed in other pipelined stages. Only the preceding circuits of the pipelined ADC, such as an anti-aliasing filter or a programmable gain amplifier, suffer the double loading caused by the first stage with the TI-CDS technique. No double loading problem exists in the back-end pipelined stages with TS-CDS technique. The TI-CDS technique seems to increase the loading of preceding circuits. However, if a TS-CDS technique, instead of a

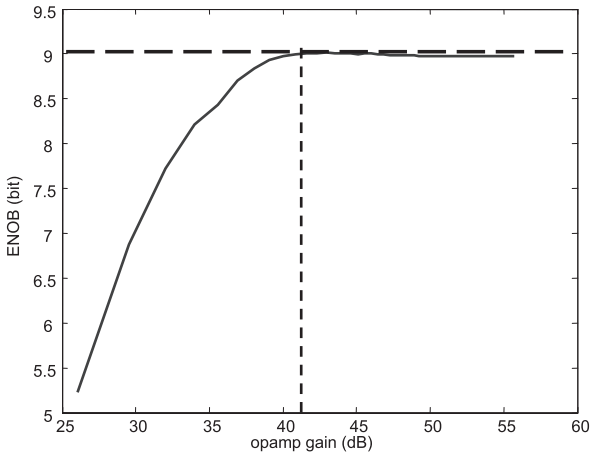


Fig. 7 Relationship of the opamp dc gain and the effective number of bits (ENOB) of proposed ADC.

TI-CDS, is used in first pipelined stage, the noise contribution of the required half-rate SHA should also be taken into consideration. Larger sampling capacitors must be adopted to compensate the additional noise imposed by the half-rate SHA. As a result, based on the same total noise, the loadings of the preceding circuits in our proposed architecture and the architecture with the TS-CDS technique are comparable.

Assume that all pipelined stages use the same capacitor value, and that the total noise of first three stages and SHA dominates that of whole ADC. The op-amp noise is not considered here to simplify analysis. Based on a fixed noise budget, the relationship between the required unit capacitor values of the 1.5-bit/stage MDAC in the time-shifted CDS (C_{TS}) and those used in the proposed technique (C_{split}) can be derived as:

$$C_{TS} = \frac{21}{13} C_{split} \tag{4}$$

A larger C_{TS} is required in the time-shifted CDS technique when the same input capacitance is assumed for the two pipelined ADCs. Moreover, when the op-amp noise is considered, the C_{TS} would be even larger due to the additional op-amp noise of the SHA. As a result, the proposed technique is more power efficient than the time-shifted CDS even though the double input capacitance of stage 1 still exists.

It should be noted that a similar but independently-derived work has been published [18]. However, our proposed technique has a comparison phase for the sub-ADC, which achieves higher speed compared with the technique in [18].

4.3 Low-Power and Low-Gain Amplifier

The behavioral model of the proposed architecture is developed with the Matlab Simulink. The relationship of the opamp dc gain and the effective number of bits (ENOB) of ADCs is shown in Fig. 7, in which only op-amp gain error is assigned in this case. To achieve 9-bit ENOB, only 40 dB

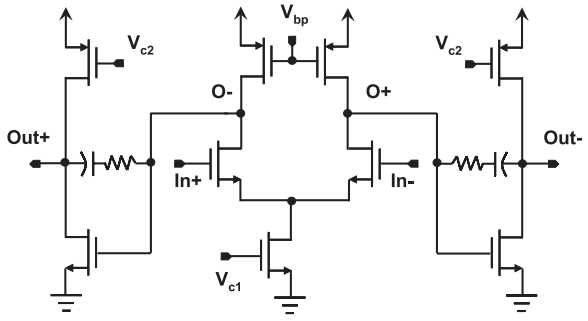


Fig. 8 Relationship of the opamp dc gain and the effective number of bits (ENOB) of proposed ADC.

Table 1 Simulated results of the low-gain amplifier.

Specification	Performance
DC Gain	51 dB
Unity-Gain Bandwidth	2.6 GHz
Phase Margin (@ $\beta = 1$)	45°
Total Power	4.5 mW
Supply Voltage	1.2 V
Output Swing (diff.)	±0.8 V
Loading	1 pF
Technology	TSMC 0.13 μm CMOS Process

opamp dc gain is required. However, additional charge injection of switches and parasitic capacitors in practical SC circuits would degrade the effectiveness of the proposed TI-CDS. These effects are not included in this model. Moreover, the opamp gain is varied with output signal. Linear op-amp gains are assigned in this model. The nonlinear op-amp gain would induce additional nonlinear error. Based on these reasons, higher opamp gain is required. In this chip, a 51 dB op-amp is used. The low-gain amplifier shown in Fig. 8 is exploited to implement the front-end pipelined stages. Conventional Miller compensation is adopted for frequency compensation. The CDS technique allows short channel devices to be adopted to achieve high-speed operation. Table 1 shows the simulation results of this low-gain amplifier with a TSMC 0.13 μm CMOS process. Total power consumption of the opamp is 4.5 mW.

5. Design Considerations for SHA-less Architecture

A front-end SHA provides a held signal to MDAC and the sub-ADC in the first pipelined stage to avoid problems caused by the timing mismatch between these two circuits, as shown in Fig. 2. The SHA-less architecture has an additional signal-dependent offset in the first pipelined stage when any timing mismatch exists. This offset is proportional to the input frequency [9]. Fortunately, with the help of the digital error correction technique, a pipelined ADC can tolerate large offset. In addition, by employing a wide-swing opamp and adopting the 1.5-bit/stage architecture in the first pipelined stage, the tolerable offset can be maximized.

The sampling networks of the MDAC and the sub-ADC in the first pipelined stage should match each other as perfectly as possible. For this purpose, a dynamic com-

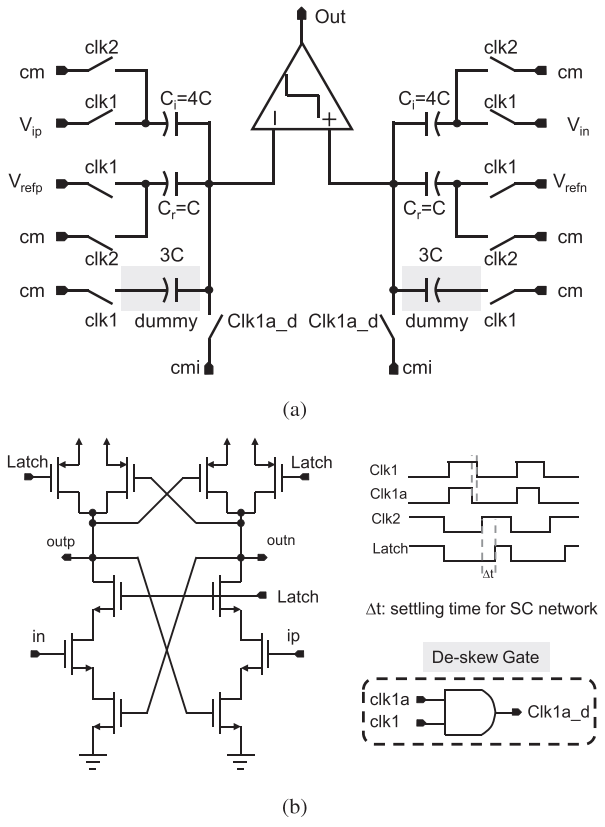


Fig. 9 (a) Dynamic SC comparator diagram. (b) Dynamic latch circuit and timing diagram.

parator with an SC sampling network is adopted, as shown in Fig. 9. The core of the comparator uses a dynamic latch circuit for the low-power operation. Clk1 and clk2 are non-overlapped clocks. When clk1/clk1a is high, the inputs, V_{in} and V_{ip}, and reference voltages of an ADC, V_{refp} and V_{refn}, are sampled on capacitors C_i and C_r, respectively. The falling edge of clk1a early falls before that of clk1. In order to match the sampling scheme of the TI-CDS MDAC in the first pipelined stage, a duplicated de-skew gate is used. The falling edge of clk1a_d, which determines the sampling instant of the comparator, is aligned with that of ϕ_{1a} and ϕ_{3a}, as shown in Fig. 6. The sampling networks for MDAC and sub-ADC are designed to match each other. The rising edge of the latch clock determines the comparison instant of the comparator. The time interval Δt is preserved for the settling time of the SC network. The threshold voltage of the comparator is:

$$\pm V_{th} = \pm \frac{C_r}{C_i} \cdot \left(V_{refp} - V_{refn} \right) \tag{5}$$

where V_{th} is the designed threshold voltage of a comparator, C_i is the input capacitor, and C_r is the reference capacitor. The ratio of C_r over C_i for the 1.5-bit/stage case is 1:4. Dummy capacitors are also employed to enhance the matching between the sampling networks of MDAC and the sub-ADC in the first pipelined stage.

6. Power-Efficient Back-End Pipelined Stage Design

6.1 Limitations for Power-Scaling of the Back-End Pipelined Stages in the Conventional Architecture

Because the accuracy requirements of the back-end pipelined stages are relaxed gradually in a pipelined ADC, the power consumption of back-end pipelined stages can be reduced by using lower accuracy circuits. However, several practical design constrains limit the achievable power reduction of back-end pipelined stages.

First, the inter-stage gain equivalently decreases the referred-to-input noise contributions of the back-end pipelined stages. The capacitances of the back-end pipelined stages can be thus scaled down. However, such a scaling cannot be unrestricted, and device mismatch and fabrication limitation determine the minimum capacitor value. Accordingly, the minimum loadings of the back-end pipelined stages are usually determined by the minimum capacitor value, which limits the power scaling capability of back-end pipelined stages. Moreover, in the practical layout of the back-end pipelined stages, the routing parasitic capacitance would dominate the total output loading of op-amps. This issue further limits the amount of the power scaling for the back-end stages. Second, the power consumption of sub-ADCs and bias generators in the back-end pipelined stages cannot usually be reduced too much. As a result, the power consumption of these circuits is constant value and becomes the bottleneck of the power reduction of the back-end pipelined stages. Due to above-mentioned discussions, how to further reduce the power consumption of the back-end pipelined stages is an important design issue in a low-power pipelined ADC design. This issue is rarely addressed in previous works.

6.2 Resolution Selection of a Time-Interleaved SA ADC

An SA ADC adopts a binary search algorithm to complete analog-to-digital conversion. Each algorithmic cycle processes single-bit/multi-bit conversion [18]. As a result, multiple algorithmic cycles are required to complete one data conversion. An SA ADC only requires one active component, i.e., a comparator. Other circuits are passive capacitor arrays and digital control circuits. Data conversion can be sped up with the short-channel devices provided in the advanced CMOS process. As a result, SA ADCs can significantly benefit from advances in the digital CMOS process. In recent high power-efficient ADC designs, SA ADCs have become the best candidate for low/medium resolution and low-power applications [19]–[22]. This research trend has motivated the use of an SA ADC to replace conventional opamp-based designs applied for the back-end pipelined stages.

The DAC in a conventional SA ADC is usually implemented with a passive capacitor array due to its low-power

potential. The total capacitance of DAC exponentially increases with resolution. This not only limits the conversion speed of an SA ADC but also heavily loads the preceding pipelined stage when it is employed to implement the back-end pipelined stages. In other words, without carefully choosing the resolution of the back-end SA ADC, the total power of the proposed ADC may be even larger than that of an implementation using conventional opamp-based pipelined stages. Therefore, the resolution of a back-end SA ADC must be decided carefully for the minimum total power consumption of the proposed pipelined ADC.

In general, the power consumption of opamps is proportional to their output loading capacitances and makes up the major part of the total power consumption of a pipelined ADC. Other circuits, such as the clock generator, sub-ADCs, and digital circuits, have almost constant power consumption when the resolution is determined. As a result, in this work, the optimum resolution of the back-end SA ADC is decided by comparing the total output loading capacitance of each pipelined stage in various topologies.

The total output loading capacitance of a pipelined ADC combined with the back-end SA ADC is calculated according to the simplified circuit model shown in Fig. 10(a). The front-end circuit indicates an anti-aliasing filter or a programmable gain amplifier (PGA) when an ADC is integrated in a practical system. The input capacitor of the ADC loads the front-end circuit. This loading capacitor should be considered for fair comparison.

The 1.5-bit/stage architecture is adopted to implement the front-end pipelined stage for high-speed operation and simple design. The loading capacitance of each pipelined stage includes the feedback loading capacitance and the sampling capacitance of the next pipelined stage. In addition, the loading capacitance of the preceding pipelined stage of the back-end SA ADC is the feedback loading capacitance and the total capacitor value of the binary DAC adopted by a conventional SA ADC. As a result, the total loading of a pipelined ADC combined with the back-end SA ADC is given as:

$$\begin{cases} C_{total} = \left(C_{f,1} + C_{s,1} + C_{subadc}\right) \\ \qquad + \sum_{k=1}^{N_{pipe}-1} \left(C_{s,k} // C_{f,k}\right) \\ \qquad + \sum_{k=1}^{N_{pipe}-1} \left(C_{f,(k+1)} + C_{s,(k+1)} + C_{subadc}\right) \\ \qquad + \left(C_{s,N_{pipe}} // C_{f,N_{pipe}} + 2^{N_{sa}-1} \cdot C_{u,sa}\right) \\ C_{s,i} = C_{f,i} = \mathrm{Max}\left(\frac{C_{1,pipe}}{G^{k-1}}, C_{min}\right), k = 1 \ldots N_{pipe} \\ N_{adc} = N_{pipe} + N_{sa} \end{cases} \quad (6)$$

where C_{total} represents the total output loading of the proposed ADC, as shown in Fig. 10(a). The three terms are the loadings of the front-end circuit, pipelined stages except for the preceding stage of the SA ADC, and the preceding pipelined stage of the SA ADC, respectively. N_{adc}, N_{pipe}, and N_{sa} are the effective resolutions of whole ADC, opamp-based pipelined stages, and the back-end SA ADC, respectively. The input capacitor value (C_{subadc}) of the sub-ADC is set as the same value in every pipelined stage. For

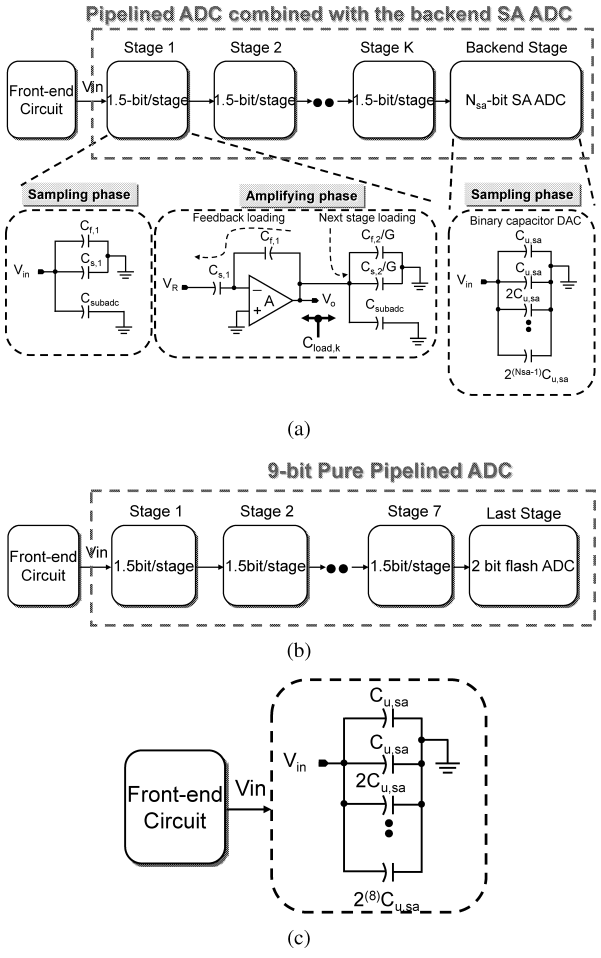


Fig. 10 Circuit model for (a) the proposed 1.5-bit/stage pipelined ADC with the backend SA ADC; (b) a 9-bit conventional pipelined ADC with a 1.5-bit/stage architecture and a 2-bit last stage; (c) a 9-bit pure SA ADC.

Table 2 Parameters used in the total loading calculations.

Parameter	Value
N_{adc}	9 bits
C_{subadc}	50 fF
C_{u_pipe}	400 fF
C_{min}	100 fF
C_{sa}	20 fF
G	2

the power optimized design, the MDAC capacitors in each pipelined stage ($C_{s,k}$ and $C_{f,k}$) are scaling down gradually by a scaling factor, G, which is 2 for the 1.5-bit/stage architecture [22]. However, the capacitor value must be limited for device matching and manufacturing considerations. In this work, we set 100 fF as the minimum capacitor value (C_{min}) for the front-end pipelined stages and 20 fF as the unit capacitor value for the back-end SA ADC ($C_{u,sa}$). The capacitor of the first pipelined stage ($C_{1,pipe}$) was determined based on KT/C noise consideration. The total loading of a 9-bit proposed ADC versus the resolution of the back-end SA ADC is shown in Fig. 11, where $C_{1,pipe}$ is set as 0.4 pF. Parameters used in the total loading calculations are listed in Table 2.

In Fig. 11, the dashed parabolic-like curve represents the total loading of the proposed architecture. The leftmost point means that the architecture is constructed by 7-bit front-end pipelined stages and 2-bit back-end SA ADC, and the rightmost point means that the architecture consists of 1-bit front-end pipelined stages and 8-bit back-end SA ADC. From this curve, a 5-bit or 6-bit SA ADC may be the proper choice for minimum total loading based on the parameters listed in Table 2. The horizontal dashed line means the total loading of a 9-bit pure pipelined ADC shown in Fig. 10(b). When the resolution of back-end SA ADC is less than 8 bits, the proposed architecture still has low-power advantages over a 9-bit conventional pipelined ADC. Moreover, the total loading of a 9-bit pure SA ADC, denoted with solid line in Fig. 11, is much larger than those of the other two architectures. This means that a high-resolution pure SA ADC heavily loads the front-end circuit, and consequently consumes larger power in the front-end circuits despite the core of the 9-bit pure SA ADC being power-efficient. As a result, when the power consumption of the preceding circuits of ADCs is considered, the low-power advantage of pure medium/high-resolution SA ADCs would be lost unless the heavy input loading problem can be solved.

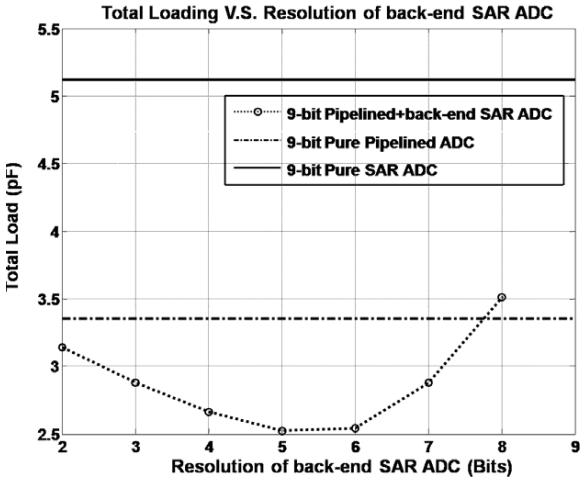


Fig. 11 Total loading of a 9-bit proposed ADC versus the resolution of the back-end SA ADC.

Moreover, a flash ADC is also a candidate to implement the back-end pipelined stages. The main advantage of a flash ADC is its high-speed operation potential. However, a conventional flash ADC usually requires many comparators and consumes lots of power. As a result, for ADCs operated around 100 MS/s, the power efficiency of a flash ADC is much lower than that of a SA ADC.

7. Circuit Implementations and Design Considerations for Back-End SA ADC

The timing of the front-end pipelined stages and that of the

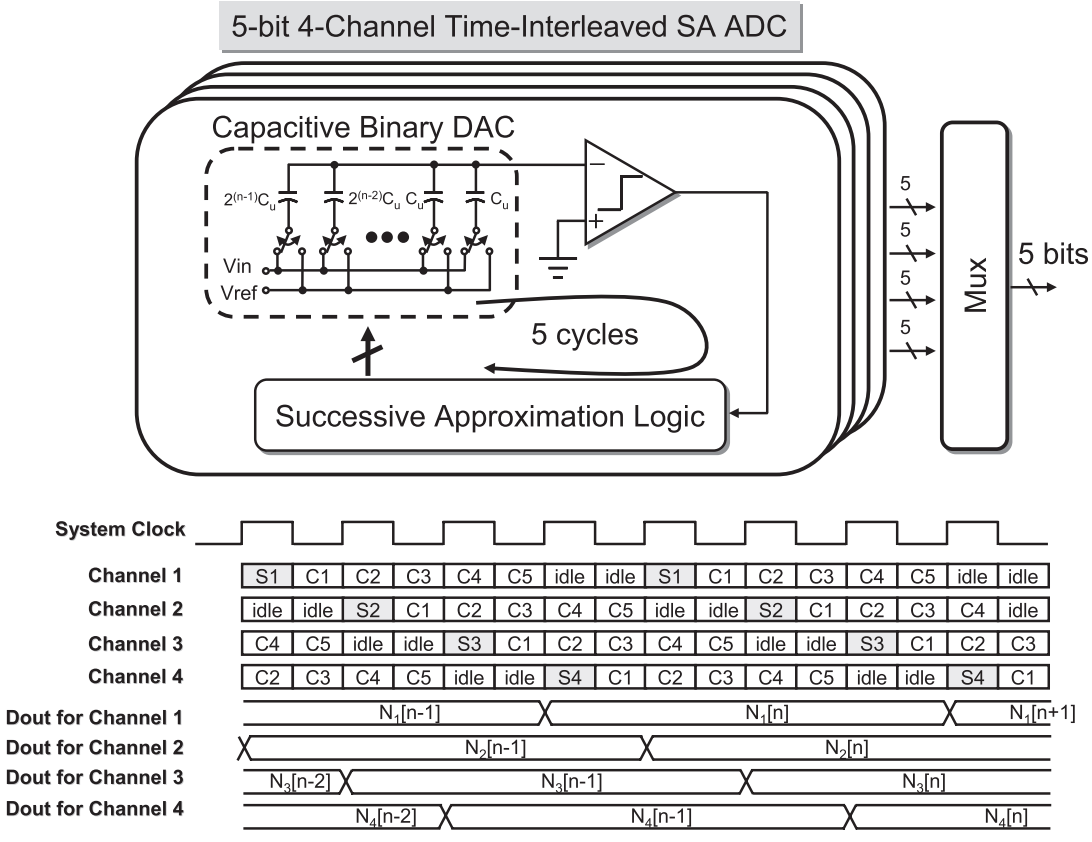


Fig. 12 Circuit diagram of the 5-bit 4-channel time-interleaved SA ADC used for the back-end stage in our proposed architecture and its arranged timing diagram.

back-end SA ADC must be synchronized. The clock frequency of the back-end SA ADC must be much higher than that of the front-end pipelined stages to achieve the same throughput rate. As a result, how to synchronize two different frequencies of clocks becomes one critical problem. The time-interleaved architecture and proper timing are employed to overcome this problem. The single-ended version of circuit diagram is shown in Fig. 12. The fully differential circuits are adopted in this work. A 5-bit 4-channel time-interleaved SA ADC is used to implement the back-end stage for power saving. Each channel is allocated 8 clock cycles, including one sampling phase, two idle phases, and five conversion phases. Every phase is synchronized with the system clock. The total data throughput rate of the time-interleaved SA ADC is the same as that of an implementation with conventional opamp-based pipelined stages which completes a valid digital output per clock cycle. Each SA ADC comprises one comparator, one binary capacitive analog-to-digital (DAC) circuit, and digital control logic circuit. The preceding pipelined stage of the time-interleaved SA ADC is loaded by the time-interleaved SA ADC only during sampling phases of each channel (S1, S2, S3, and S4). As a result, only one channel at its self sampling phase would load its preceding pipelined stage. Moreover, no high-speed clock is required, which reduces the power consumption of clock buffers in the time-interleaved SA ADC.

As illustrated in Sect. 4.1, there are channel mismatch problems in the time-interleaved architecture, including gain, offset, and timing mismatching. Since the preceding pipelined stage of the time-interleaved SA ADC has an inherent sample-and hold, the problem of timing mismatch can be resolved without any overhead. The main source of gain mismatch is the DAC gain mismatch among channels, which is usually determined by capacitor mismatch. The gain mismatch can be easily controlled at 5–6 bit accuracy with careful layout technique. An offset mismatch among multiple channels of the time-interleaved SA ADC is mainly caused by the mismatch of the comparator offset. To reduce the offset mismatch of the time-interleaved SA ADC, a low-offset comparator with the output offset storage (OOS) technique is shown in Fig. 13 [24]. This comparator consists of two cascaded preamplifiers and a dynamic latch. The offset of the preamplifier can be canceled with the OOS technique, and the equivalent input offset contribution of the latch is divided by the gain of two preamplifiers. The total input referred offset of the comparator can thus be controlled at a very low level. The bandwidth and power consumption of the preamplifier are not stringent because of its large allowable settling time which is about half of the system clock period.

In practice, only three time-interleaved SA ADCs are enough to operate 5-bit data conversion. Additional channel is preserved for future calibration of channel mismatches [25]. However, in this work, this technique is not applied yet. Channel mismatches of the time-interleaved SA ADC are conquered with analog techniques mentioned above.

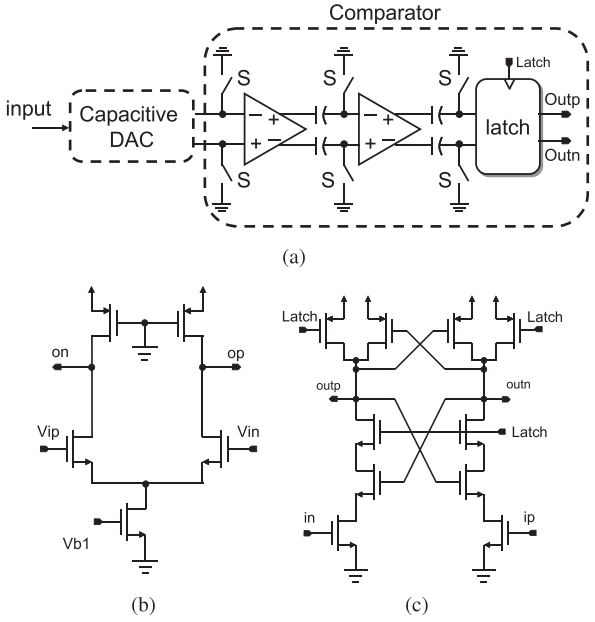


Fig. 13 (a) Comparator diagram with output offset storage (OOS) technique. (b) Preamplifier circuit. (c) Dynamic latch.

8. Experimental Results

The prototype ADC has been fabricated in a TSMC 0.13 μm triple well 1P8M CMOS process. The die photograph is shown in Fig. 14. The core die area occupies about 1.6 mm^2 (1.6 mm $\times$ 1 mm). The power consumption is 21.2 mW from a 1.2 V power supply at a 100 MS/s sampling rate.

The dynamic specifications, including SNDR, SFDR, THD, were analyzed by fast Fourier transform (FFT) with the MATLAB CAD tool. The specifications of the static linearity, including integral nonlinearity (INL) and differential nonlinearity (DNL), were measured based on the code density testing method [26]. The measured DNL and INL are shown in Fig. 15. The absolute peak DNL and INL

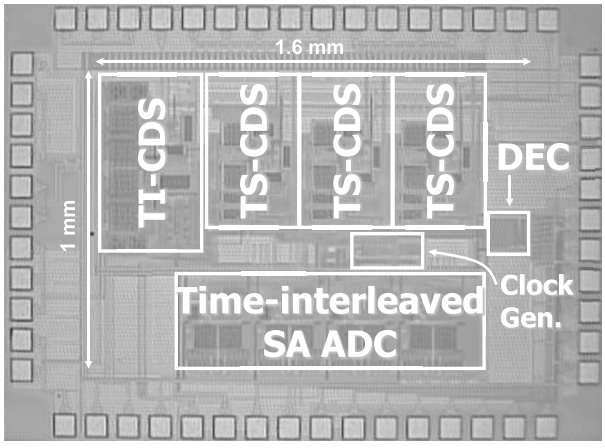


Fig. 14 Circuit diagram of the 5-bit 4-channel time-interleaved SA ADC used for the back-end stage in our proposed architecture and its arranged timing diagram.

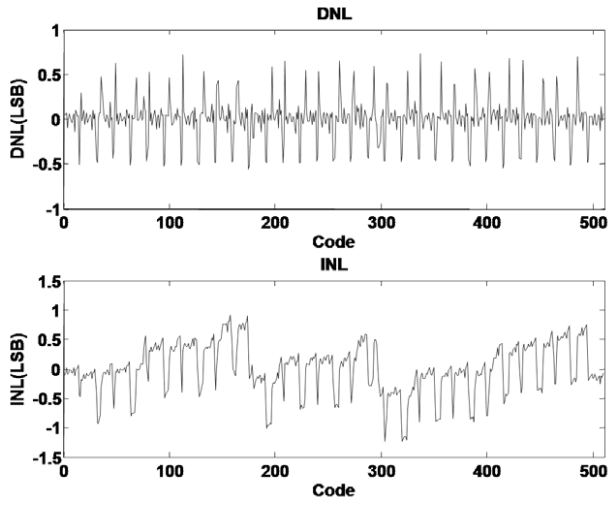


Fig. 15 Measured DNL and INL.

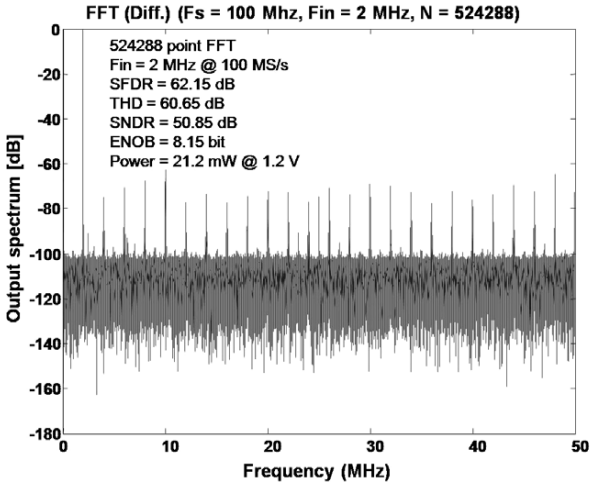
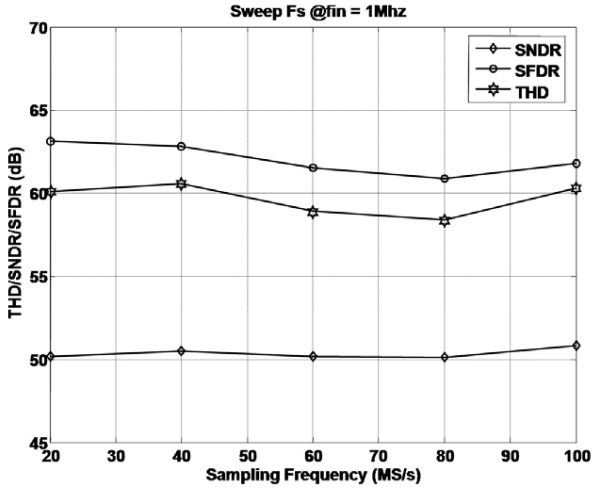
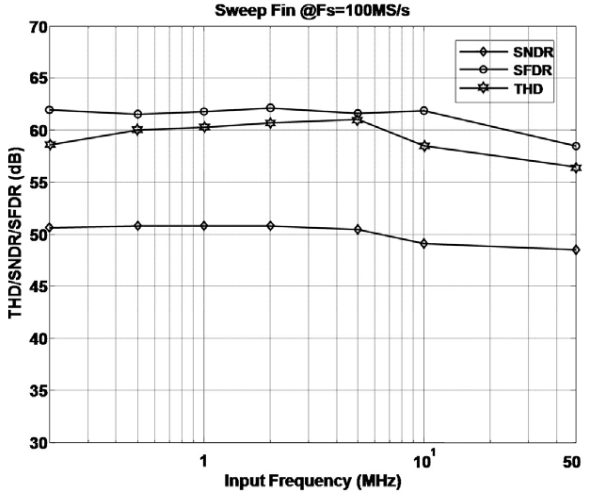


Fig. 16 The measured spectrum at a 100 MS/s sampling rate and a 2 MHz input signal.



(a)



(b)

Fig. 17 Measured THD, SFDR, and SNDR versus (a) sampling rate (@Fin = 1 MHz) (b) input frequency (@Fs = 100 MS/s).

are within ±0.61 LSB and ±1.19 LSB, respectively. Apparent DNL peaks appear periodically every 32 digital codes, which are suspected to come from the exceedingly accumulated signal-dependent offset in the TS-CDS technique mentioned in Sect. 3.4. Too large comparator offset of the sub-ADC in the front-end pipelined stages maybe reduces the tolerable offset margin allocated for accumulated signal-dependent offsets caused by the TS-CDS pipelined stages. The dynamic performance at a 2 MHz input frequency is shown in Fig. 16. The SNDR, SFDR, and THD are 50.85 dB, 62.15 dB, and 60.65 dB, respectively. The ENOB is about 8.15 bits. Figure 17(a) shows the dynamic performance versus sampling rate at a 1 MHz input frequency, and Fig. 17(b) shows the dynamic performance versus input frequency at a 100 MS/s sampling rate. The SNDR is 48.48 dB at a 49 MHz input frequency. The dynamic performance versus input signal level is shown in Fig. 18. The peak SFDR is about 61.22 dB. The measured results of the proposed ADC are summarized in Table 3. A comparison with other re-

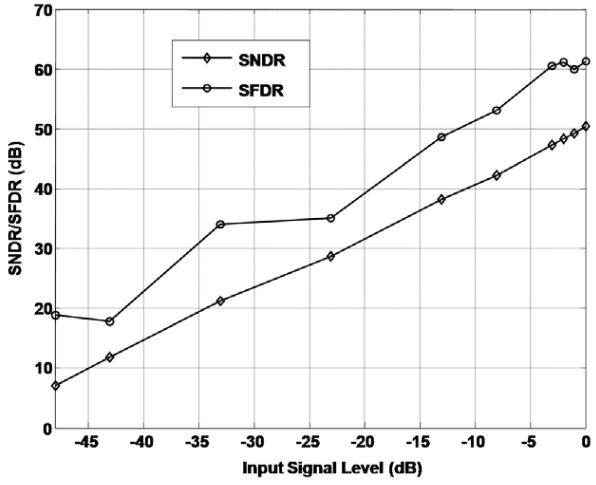


Fig. 18 SFDR and SNDR versus input signal level.

Table 3 Performance summary.

Resolution	9 bits
Sampling Rate	100 MS/s
Power Supply	1.2 V
Input Range (diff.)	± 0.8 V
SNDR @ f_{in} = 2 MHz	50.85 dB
SFDR @ f_{in} = 2 MHz	62.15 dB
DNL	−0.58 LSB−0.61 LSB
INL	−1.19 LSB−0.85 LSB
Power Consumption (Exclude the reference buffer)	21.2 mW
Core area	1.6 mm^2

Table 4 Comparison with reported pipelined ADCs implemented in a 0.13 μm CMOS process.

V_{DD} (V)	Resolution (Bits)	F_s (MHz)	Power (mW)	FOM (pJ/step)	Ref.
1.2 / 3.3	10	205	92.5	0.81	B. Hernes [3]
1.2	10	220	135	1.47	B. Hernes [27]
1.2	10	100	45.6	1.20	Y. J. Kim [28]
1.5	10	80	33	0.80	O. Stroeble [29]
1.2	9	100	21.2	0.75	This work

ported pipelined ADCs implemented with a 0.13 μm CMOS process is listed in Table 4. The figure of merit (FOM) of ADC, given by Eq. (7), is used to evaluate the ADC performance.

$$FOM = \frac{Power}{2^{ENOB} \cdot F_S} \tag{7}$$

The proposed architecture has a better FOM than those of other state-of-the-art works.

9. Conclusion

The TI-CDS technique is proposed to eliminate the required half-rate front-end SHA in the TS-CDS technique to enhance the low-power potential of the CDS technique. For further power reduction, the back-end pipelined stages are implemented with a low-resolution power-efficient time-interleaved SA ADC. Due to these architectural innovations, no high-gain opamp is required in this work. Therefore, the pipelined ADC with our proposed architecture is more compatible with the advanced digital CMOS process. Compared with a pure SA ADC, our proposed pipelined ADC has more low-power potential for 10-bit or higher resolution applications in the advanced CMOS process.

Acknowledgment

The authors would like to acknowledge the fabrication and measurement support provided by the National Chip Implementation Center (CIC), Taiwan.

References

[1] T. Nezuka, K. Misawa, J. Azami, Y. Majima, and J. Okamura, "A 10-bit 200-MS/s pipeline A/D converter for high-speed video signal digitizer," Proc. IEEE Asia Solid-State Circuits Conf., pp.31–34, Nov. 2006.

[2] Y.-J. Kim, Y.-J. Cho, D.-H. Sa, and S.-H. Lee, "A 10 b 200 MS/s 1.8 mm^2 83 mW 0.13 μm CMOS ADC based on highly linear integrated capacitors," IEICE Trans. Electron., vol.E90-C, no.10, pp.2037–2043, Oct. 2007.

[3] B. Hernes, J. Bjrnsen, T.N. Andersen, A. Vinje, H. Korsvoll, F. Telst, A. Briskemyr, C. Holdo, and O. Moldsvor, "A 92.5 mW 205 MS/s 10b pipeline IF ADC implemented in 1.2 V/3.3 V 0.13 μm CMOS," ISSCC Dig. Tech. Papers, pp.462–463, Feb. 2007.

[4] K.W. Hsueh, Y.K. Chou, Y.H. Tu, Y.F. Chen, Y.L. Yang, and H.S. Li, "A 1 V 11b 200 MS/s pipelined ADC with digital background calibration in 65 nm CMOS," ISSCC Dig. Tech. Papers, pp.546–547, Feb. 2008.

[5] L. Brooks and H.S. Lee, "A zero-crossing-based 8-bit 200 MS/s pipelined ADC," IEEE J. Solid-State Circuits, vol.42, no.12, pp.2677–2687, Dec. 2007.

[6] B.R. Gregoire and U.K. Moon, "An over-60 dB true rail-to-rail performance using correlated level shifting and an opamp with only 30 dB loop gain," IEEE J. Solid-State Circuits, vol.43, no.12, pp.2620–2630, Dec. 2008.

[7] J. Li and U.K. Moon, "A 1.8-V 67-mW 10-bit 100 MS/s pipelined ADC using time-shifted CDS technique," IEEE J. Solid-State Circuits, vol.39, pp.1468–1476, Sept. 2004.

[8] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC," IEEE J. Solid-State Circuits, vol.35, no.3, pp.318–325, March 2000.

[9] D.Y. Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," IEEE Trans. Circuits Syst. I, vol.51, no.11, pp.2123–2132, Nov. 2004.

[10] B.G. Lee, B.M. Min, G. Manganaro, and J.W. Valvano, "A 14b 100 MS/s pipelined ADC with a merged active S/H and first MDAC," ISSCC Dig. Tech. Papers, pp.248–249, Feb. 2008.

[11] K.J. Lee, E.S. Shin, H.S. Yang, J.H. Kim, P.U. Ko, I.R. Kim, S.H. Lee, K.H. Moon, and J.W. Kim, "A 90 nm CMOS 0.28 mm^2 1 V 12b 40 MS/s ADC with 0.39 pJ/conversion-step," Symp. VLSI circuits Dig. Tech. Papers, pp.198–199, June 2007.

[12] C.C. Enz and G.C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," Proc. IEEE, pp.1584–1614, Nov. 1996.

[13] K. Nagaraj, T.R. Viswanathan, K. Singhal, and J. Vlach, "Switched-capacitor circuits with reduced sensitivity to amplifier gain," IEEE Trans. Circuits Syst., vol.CAS-34, no.5, pp.571–574, May 1987.

[14] J.F. Lin and S.J. Chang, "A high-speed pipelined analog-to-digital converter using modified time-shifted correlated double sampling technique," Proc. Int. Symp. Circuits and Syst., pp.5367–5370, May 2006.

[15] Y. Chiu, P.R. Gray, and B. Nikoli, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," IEEE J. Solid State Circuits, vol.39, no.12, pp.2139–2151, Dec. 2004.

[16] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," IEEE Trans. Circuits Syst. I, vol.48, no.3, pp.261–271, March 2001.

[17] M. Waltari and K. Halonen, "Timing skew insensitive switching for double-sampled circuits," Proc. Int. Symp. Circuits and Syst., pp.61–64, June 1999.

[18] Y.J. Kook, J. Li, B. Lee, and U.K. Moon, "Low-power and high-speed pipelined ADC using time-aligned CDS technique," Proc. IEEE Cust. Int. Circuits Conf., pp.321–324, Sept. 2007.

[19] Z. Cao, S. Yan, and Y. Li, "A 32 mW 1.25GS/s 6b 2b/step SAR ADC in 0.13 μm CMOS," ISSCC Dig. Tech. Papers, pp.542–543, Feb. 2008.

[20] S.W.M. Chen and R.W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," IEEE J. Solid-State Circuits, vol.41, no.12, pp.2669–2680, Dec. 2006.

[21] J. Craninckx and G. Van der Plas, "A 65 fJ/Conversion-Step 0-to-

50 MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90 nm digital CMOS," ISSCC Dig. Tech. Papers, pp.246–247, Feb. 2007.
[22] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. Van der Plas, and J. Craninckx, "An 820 μW 9b 40 MS/s noise-tolerant dynamic-SAR ADC in 90 nm digital CMOS," ISSCC Dig. Tech. Papers, pp.238–239, Feb. 2008.
[23] D.W. Cline and P.R. Gray, "A power optimized 13-b 5-Msamples/s pipelined analog-to-digital converter in 1.2-μm CMOS," IEEE J. Solid-State Circuits, vol.34, no.3, pp.294–303, March 1996.
[24] B. Razavi and B.A. Wooley, "Design techniques for high-speed, high-resolution comparators," IEEE J. Solid-State Circuits, vol.27, no.12, pp.1916–1626, Dec. 1992.
[25] K.C. Dyer, D. Fu, S.H. Lewis, and P.J. Hurst, "An analog background calibration technique for time-interleaved analog-to-digital converters," IEEE J. Solid-State Circuits, vol.33, no.12, pp.1912–1919, Dec. 1998.
[26] J. Doernberg, H.S. Lee, and D.A. Hodges, "Full-speed testing of A/D converters," IEEE J. Solid-State Circuits, vol.SC-19, no.6, pp.820–827, Dec. 1984.
[27] B. Hernes, A. Briskemyr, T.N. Andersen, F. Telst, T.E. Bonnerud, and Moldsvor, "A 1.2 V 220 MS/s 10 bit pipeline ADC implemented in 0.13 μm digital CMOS," ISSCC Dig. Tech. Papers, pp.256–257, Feb. 2004.
[28] Y.J. Kim, H.C. Choi, S.W. Yoo, S.H. Lee, D.Y. Chung, K.H. Moon, H.J. Park, and J.W. Kim, "A re-configurable 0.5 V to 1.2 V, 10 MS/s to 100 MS/s, low-power 10b 0.13 μm CMOS pipeline ADC," Proc. IEEE Cust. Int. Circuits Conf., pp.185–188, Sept. 2007.
[29] O. Stroeble, V. Dias, and C. Schwoerer, "An 80 MHz 10b pipeline ADC with dynamic range doubling and dynamic reference selection," ISSCC Dig. Tech. Papers, pp.462–539, Feb. 2004.

Jin-Fu Lin was born in Changhua, Taiwan, in 1981. He received B.S. degree from the Department of Electrical Engineering, National Chi-Nan University (NCNU), Taiwan, in 2002. He obtained his M.S. degree in Electronic Engineering from National Cheng Kung University (NCKU), Taiwan, in 2004. He is currently working toward the Ph.D. degree. His research interests include low-power ADC design and test.

Soon-Jyh Chang was born in Tainan, Taiwan, in 1969. He received BS degree in Electrical Engineering from National Central University (NCU), Taiwan, in 1991. He obtained his M.S. and Ph.D. degrees in Electronic Engineering from National Chiao-Tung University (NCTU), Taiwan, in 1996 and 2002 respectively. He joined the Department of Electrical Engineering, National Cheng Kung University (NCKU), Taiwan, in 2003, and he has been an associate professor there since 2008. His research interests include design, testing, and design automation for analog and mixed-signal circuits. Dr. Chang has served as chair of IEEE SSCS Tainan Chapter since Jan. 2009. He also served as a technical program committee member for VLSI-DAT, A-SSCC and ATS in 2009. He was one of the recipients of Greatest Achievement Award from National Science Council, Taiwan, 2007.