An Asynchronous Binary-Search ADC Architecture With a Reduced Comparator Count

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***Abstract*—This paper reports an asynchronous binary-search analog-to-digital converter (ADC) with reference range prediction. An original N-bit binary-search ADC requires $2^N - 1$ comparators while the proposed one only needs $2N - 1$ ones. Compared to the (high speed, high power) flash ADC and (low speed, low power) successive approximation register ADC, the proposed architecture achieves the balance between power consumption and operation speed. The proof-of-concept 5-bit prototype only consists of a passive track-and-hold circuit, a reference ladder, 9 comparators, 56 switches and 26 static logic gates. This compact ADC occupies an active area of $120 \times 50\ \mu m^2$ and consumes 1.97 mW from a 1-V supply. At 800 MS/s, the effective number of bits is 4.40 bit and the effective resolution bandwidth is 700 MHz. The resultant figure of merit is 116 fJ/conversion-step.**

***Index Terms*—Asynchronous analog-to-digital converter (ADC), Binary-search analog-to-digital converter (ADC), successive approximation register (SAR).**

I. Introduction

DIGITAL wireless communication applications such as ultrawideband (UWB) and wireless personal area network (WPAN) need low-power high-speed analog-to-digital converters (ADCs) to convert RF/IF signals into digital form for baseband processing. Considering latency and conversion speed, the flash ADC is often the most preferred selection in high-speed communication applications [1]–[3]. Fig. 1 shows a simplified block diagram of a flash ADC. The component count of a flash ADC grows exponentially with resolution. The hardware complexity of a flash ADC depends on its resolution and utilized techniques such as interpolation, resistive averaging and calibration. Generally speaking, fully parallel ADCs suffer from high power consumption and large area overhead. On the contrary, a successive approximation register (SAR) ADC has features of low power dissipation and small area. Fig. 2 illustrates a simplified block diagram of a SAR ADC where the analog-to-digital conversion is based on the binary-search algorithm [4], [5]. Since SAR ADCs need several comparisons to complete one conversion, a sample-and-hold (S/H) circuit is necessary to retain data. The comparator determines the polarity of the difference between the sampled input signal and reference voltage. The decision of the comparator triggers the SAR logic which subsequently controls the DAC to prepare the reference voltage for the next comparison. SAR logic operation and reference settling limit the conversion speed of a SAR ADC. The highest single-channel operation speed of the previously reported SAR ADCs is 625 MS/s [4]. The ADC in [4] utilizes a 2-bit/step structure. A multi-bit/step structure requires several DACs to generate reference voltages for the comparators. Moreover, a multi-bit/step structure is more complicated than a non-multi-bit/step one because the mismatches between DACs and comparators affect performance. For non-multibit/step SAR ADCs, the highest conversion rate is 300 MS/s [5]. The 6-bit work in [5] uses seven comparison phases to complete one conversion, thus yielding a 0.86-bit/step structure.

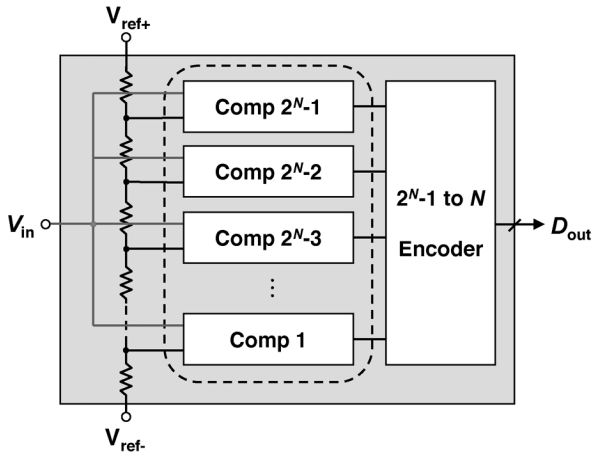

Fig. 1. Block diagram of a flash ADC.

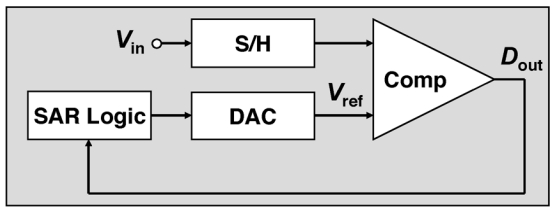

Fig. 2. Block diagram of a SAR ADC.

Fig. 3 depicts the simplified block diagram of a binary-search ADC which is a transitional structure between flash and SAR ADCs [6]. This ADC uses a binary-search algorithm similar to that of a SAR ADC. This ADC also requires several comparisons for one conversion. The comparator count of an N-bit binary-search ADC is $2^N - 1$, the same as an N-bit flash ADC. A binary-search ADC seems to have disadvantages of both ADCs:

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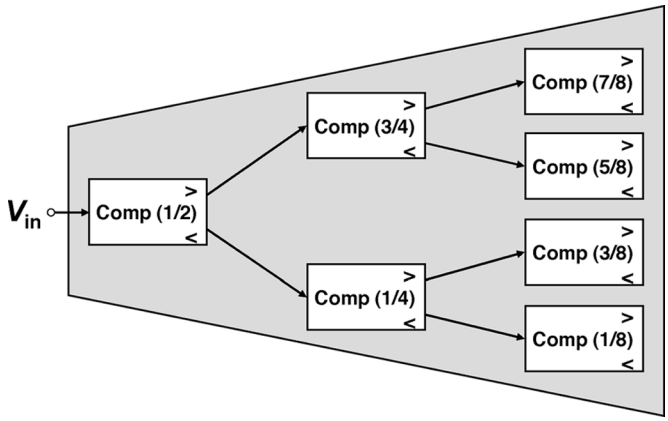

Fig. 3. Block diagram of a binary-search ADC.

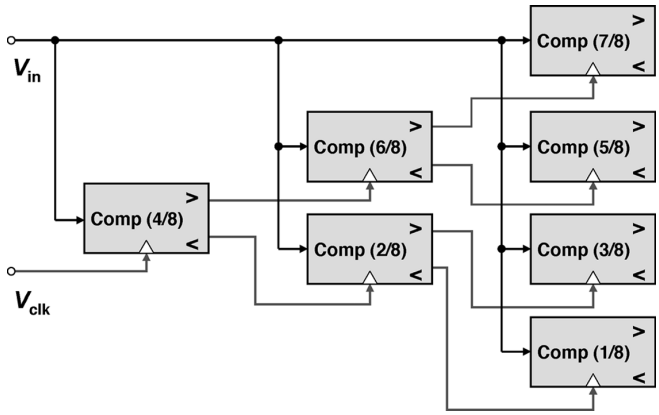

Fig. 4. The original asynchronous binary-search ADC.

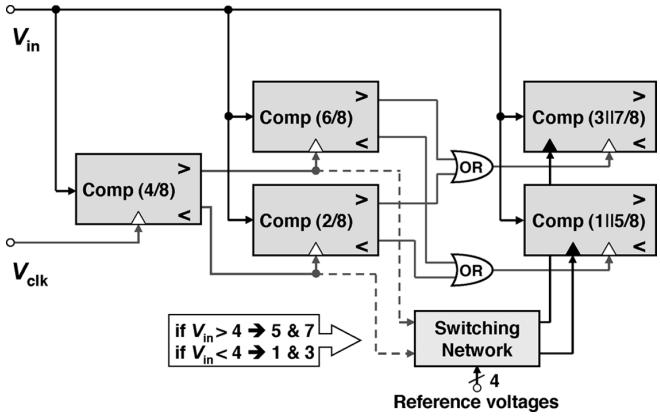

Fig. 5. An asynchronous binary-search ADC with reference range prediction.

the low speed of a SAR ADC and large hardware overhead of a flash ADC. Consequently, this ADC is seldom used in practical applications. However, from another point of view, it has advantages of flash and SAR ADCs. Although there are $2^N - 1$ comparators in an N-bit ADC, only N comparators are activated in one conversion. Therefore, a binary-search ADC has lower power consumption than a flash ADC. Like a flash ADC, the conversion time of a binary-search ADC does not contain reference voltage settling time because the reference level of each comparator is a fixed voltage value. A binary-search ADC has higher operation speed than a SAR ADC. Compared to the high speed, high power flash architecture and low speed, low power SAR architecture, a binary-search ADC achieves the balance between operation speed and power consumption. This paper reports an asynchronous binary-search ADC with reference range prediction. The comparator count of the proposed ADC increases linearly with resolution, rather than exponentially in an original one. The maximum conversion speed of the 5-bit prototype achieves 800 MS/s at the cost of 2-mW power consumption.

The remaining part of this paper is organized as follows: Section II describes the operation principles of the proposed binary-search ADC. Section III discusses the design considerations of the ADC architecture and building blocks. Section IV investigates the design constraints of the ADC. Section V shows the experimental results of the prototype. Finally, we draw a conclusion in Section VI.

II. Binary-Search ADC With a Reduced Comparator Count

When we implement an ADC based on the binary-search algorithm, there are two options in architecture: synchronous and asynchronous. A synchronous ADC is compact but requires a high frequency clock, usually several times the sampling frequency. Furthermore, each time interval must tolerate the worst case, i.e., the longest comparator delay, in a synchronous case. The identical time intervals result in non-optimized operation speed. In the best case, an asynchronous ADC operates two times faster than a synchronous one [5]. From the aspect of architecture, a binary-search ADC is inherently suitable for asynchronous operation. Because the output signal of the previous stage can serve as the trigger signal of the present stage, a binary-search ADC does not require additional clock generation circuit. This arrangement avoids the requirement of a high frequency clock and leads to optimum operation speed.

Although a binary-search ADC is theoretically realizable, no silicon design is found in recent publications except [6]. The prototype in [6] demonstrates the first binary-search ADC. The 7-bit work achieves 150-MS/s operation with an incredible power dissipation of 133 μW. The impressive power efficiency shows an attractive alternative to SAR ADCs in medium resolution applications. We can foresee the growing value of the binary-search ADC in data converter design community. Fig. 4 depicts an original 3-bit asynchronous binary-search ADC [6]. The number in the comparator represents the position of the reference level in the full scale range. The first comparator compares the input signal with the middle reference level, 4/8. Depending on the decision of the first comparator, either Comp (6/8) or Comp (2/8) is activated. If Comp (6/8) is activated, then it will activate Comp (7/8) or Comp (5/8). The ADC repeats this procedure until the final bit is obtained. The original binary-search ADC suffers from large hardware overhead as a flash ADC due to the exponential relation between the resolution and comparator count. Fig. 5 shows the proposed asynchronous binary-search ADC. The core idea of the proposed work is based on [6], and a structural modification reduces the count of decision elements. Similarly, the clock

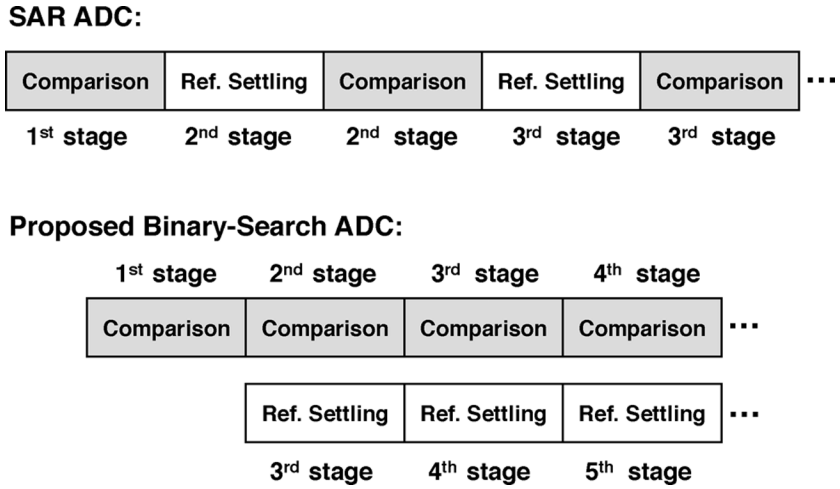

Fig. 6. Comparison of timing diagrams of a SAR ADC and the proposed ADC.

signal is only applied to the first comparator. The output signals of the first comparator are the trigger signals of the 2nd-stage comparators. Once the first comparator makes the decision, one of the 2nd-stage comparators starts the comparison. The decision of the first comparator also serves as the control signal of the reference switching network of the 3rd stage. There are four possible reference levels in the 3rd stage. If the output of the first comparator shows $V_{\rm in} > 4/8$, then only 5/8 and 7/8 are the possible references since 1/8 and 3/8 are smaller than 4/8. The selected reference voltages, e.g., 5/8 and 7/8, are connected to the 3rd-stage comparators via the reference switching network. The comparison of the 2nd-stage comparator and reference voltage switching of the 3rd stage occur simultaneously. The settling time of the switched reference voltages must be shorter than the comparison time. When the comparison of the 2nd stage completes, the triggered 3rd-stage comparator begins its comparison. At this time, the reference voltages of the 3rd-stage comparators have already settled. The accuracy of comparison is guaranteed and no conversion time is wasted.

Fig. 6 displays the simplified timing diagrams of a SAR ADC and the proposed one. After each comparison, the SAR logic and DAC prepare the new reference voltage for the next comparison. The comparator remains idle until the new reference voltage settles. On the contrary, the comparison time and reference settling time of the proposed ADC are overlapped. Theoretically, the proposed architecture achieves the same operation speed as an original binary-search ADC. Table I summarizes the features of the four architectures. The proposed architecture has fewer comparators than flash and original binary-search ADCs but more than a SAR ADC. Binary-search ADCs run at higher speed than SAR ADCs. As for power consumption, binary-search ADCs are as low power as SAR ADCs. This table shows the binary-search ADCs have the best power efficiency. In conclusion, the proposed ADC achieves a good compromise between hardware, operation speed and power consumption.

Note the table only mentions the comparator count and does not consider other hardware because the four architectures need different building blocks. For example, a flash ADC needs an encoder, a SAR ADC has a capacitive DAC network and the proposed ADC requires a switching network. It is difficult to do a fair comparison of these blocks since their design principles are quite different. If only considering the proposed architecture, we can foresee the difficulty of the switching network design in high resolution versions. For a resolution higher than 6, the exponentially growing switching network will pose a design challenge to this ADC.

TABLE I
COMPARISON OF ADC ARCHITECTURES

ADC Structure	Comparator	Speed	Power	PW / Speed
Flash	2^N-1	1	2^N-1	2^N-1
Original Binary-Search	2^N-1	1/*N*	1	*N*
Proposed Binary-Search	2*N*-1	1/*N*	1	*N*
SAR	1	<1/*N*	1	>*N*

III. PROTOTYPE IMPLEMENTATION

To demonstrate the proposed architecture, this section shows the design and implementation of a 5-bit proof-of-concept prototype. The main advantage of this architecture is the reduced comparator count but this benefit comes at the expense of complicated reference switching network design. For example, the control signal of the switching network of the 3rd stage is the output of the 1st stage while the control signals of the 4th stage are the outputs of the first two stages. In other words, more control signals are necessary for LSB stages, resulting in complicated switching network design. Design tradeoffs exist between the analog circuit, i.e., comparator, and digital circuit, i.e., switching network. In this work, the performance degradation induced by digital circuits is minimized by proper switching network design. The following subsections describe the details of the ADC architecture and building blocks.

A. ADC Architecture

Fig. 7 depicts the block diagram of the 5-bit 800-MS/s ADC which simply consists of a passive track-and-hold (T/H) circuit [6], a reference ladder, 9 comparators, 56 p-type switches and 26

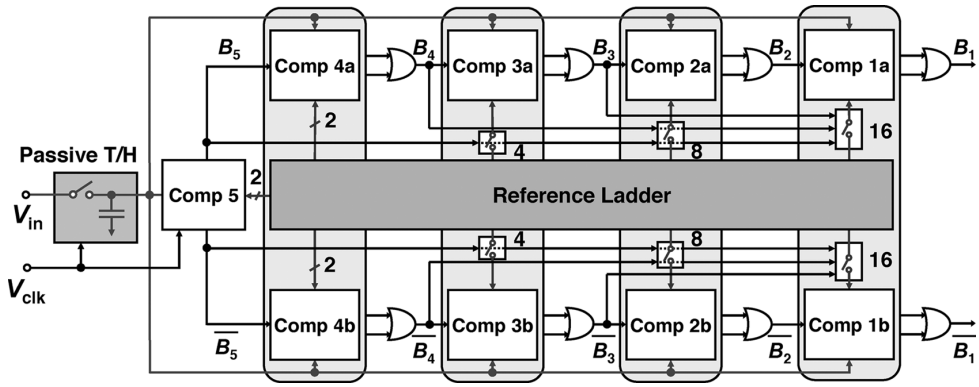

Fig. 7. Block diagram of the 5-bit 800-MS/s asynchronous binary-search ADC.

static logic gates. The first comparator, Comp 5, determines the reference voltages of the 3rd-stage comparators, Comp 3a and 3b. Since the reference voltages are differential, one pair of reference voltages is selected among two pairs to each comparator. The 1st-stage and 2nd-stage comparators together select the reference voltages of the 4th-stage comparators. In this case, one pair of reference voltages is selected among four pairs. Likewise, the reference voltages of the 5th-stage comparators are decided by the first three stage comparators. One pair of reference voltages is selected among eight pairs. The logic circuits in this work employ static types to minimize power consumption. Because the comparators are activated successively in a conversion, this ADC uses a latch-based comparator without static power consumption. In the reset phase, both outputs of a comparator are forced to ground (logic 0). If the comparator is triggered, one output will be $V_{\rm DD}$ (logic 1) and the other will be ground because of latch regeneration. True single phase CMOS (TSPC) flip-flops running at full clock rate synchronize the comparator output signals. For measurement, the synchronous data are then sampled by TSPC flip-flops clocked by an external trigger signal.

B. T/H Circuit

Like a SAR ADC, a binary-search ADC requires a sampling circuit to hold sampled input signals for repeating comparisons. An original N-bit binary-search ADC requires 2^N-1 comparators. Thus, the sampling circuit has to drive 2^N-1 comparators. Although most of the comparators are inactive, the cutoff transistors still induce parasitic capacitance to the sampling circuit. The proposed work only needs $2N-1$ comparators, which simplifies the sampling circuit design.

Fig. 8(a) depicts a classic active T/H circuit for high-speed sampling. The switch samples input signals; the capacitor holds the sampled signals; the source follower serves as a voltage buffer to drive subsequent circuits. Low supply voltage in scaled CMOS processes limits the linearity of the source follower. Consequently, the employed T/H circuit only consists of a switch and a capacitor as shown in Fig. 8(b). The passive T/H circuit provides high quality sampled signals for the comparators. Nonetheless, without an active voltage buffer, the sampled signal is sensitive to kick-back noises induced by comparator activity. This work decreases the disturbance by reducing the transistor size of the input pairs of the comparators.

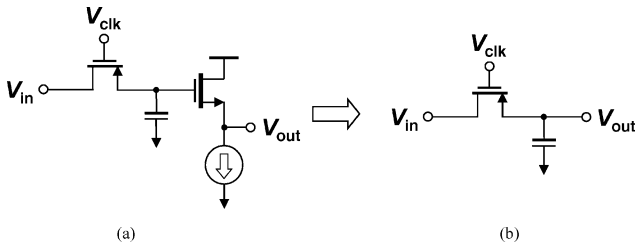

Fig. 8. (a) An active T/H circuit and (b) a passive T/H circuit.

C. Switching Network

The proposed structure reduces the number of comparators at the expense of increased complexity in the switching network which tends to grow exponentially with resolution. Fig. 9 shows a 3-bit single-ended switching network as an example. The reference voltages of the first two stages are directly connected to their comparator inputs. In the 3rd stage, the reference voltages are connected to comparator inputs via switches. For each comparator, one of the two switches is on at a time. In the 4th stage, one reference voltage is selected from four possible ones. Consequently, when the resolution increases, the control logic of the switching network of the LSB stages becomes complicated. Although the hardware complexity increases, the control signal generation time of each stage is still controlled the same. Fig. 10 shows the general connection of the control signal generation circuit. Take the 5th stage as an example. When the comparison of the 4th stage begins, the ADC starts to prepare the references of the 5th stage. The required control signals are the outputs of the first three stages. At this moment, the outputs of the first two stages are already settled. Once the output signal of the 3rd stage triggers the control signal generation circuit of the 5th stage, the control signal will be ready after one AND gate delay. Except the first two stages, the control signal generation time of each stage is only one AND gate delay. In conclusion, the control signal circuits do not reduce operation speed in spite of their complexity.

In summary, the proposed work shifts the design difficulty from analog domain to digital one. The analog circuit, i.e., comparator, concerns both accuracy and speed. On the other hand, only operation speed is important for a digital circuit, i.e., switching network. Since the operation speed is not affected by the switching network, it is advantageous to exploit this tradeoff

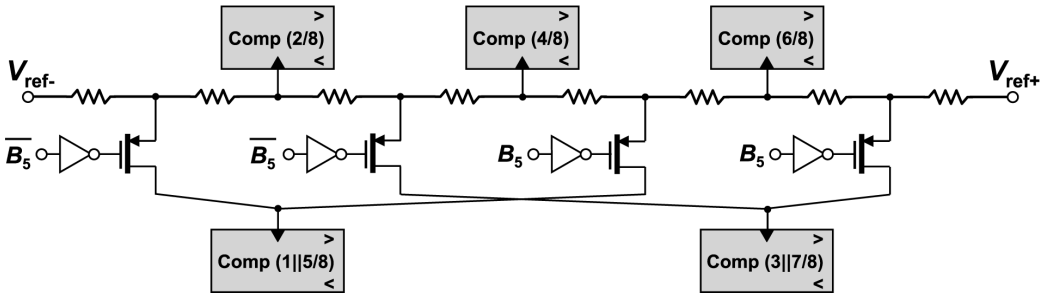

Fig. 9. Reference ladder and switching network of a 3-bit case.

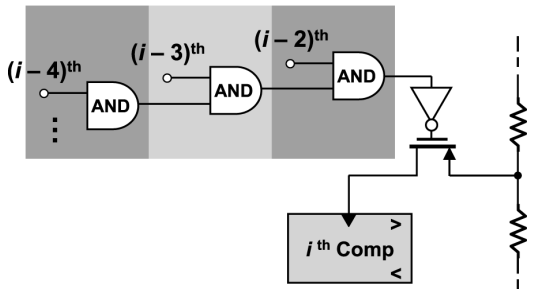

Fig. 10. Control circuit of the switching network.

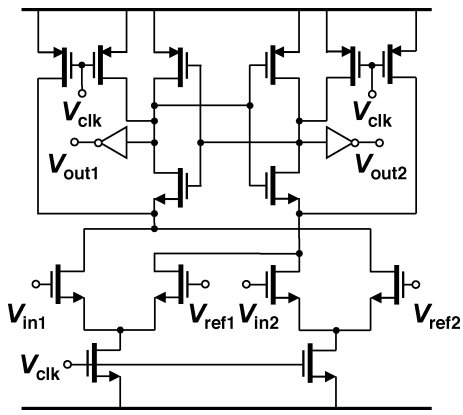

Fig. 11. Dynamic comparator without static power consumption.

toward minimizing the comparator count. If offset calibration is necessary for enhancing ADC accuracy, the small number of comparators in this work simplifies calibration circuits and reduces area overhead.

D. Dynamic Comparator

Both amplifiers and comparators are extensively used in ADC design. The bias conditions of an amplifier have great influence on its parameters such as gain and bandwidth. Process, temperature and supply voltage variations may cause the drift of bias conditions. Unlike amplifiers, comparators inherently have strong immunity against these variations. In comparator design, the primary concern is the matching properties rather than bias conditions. Generally speaking, comparators have better power efficiency and more robust performance than amplifiers.

The comparator is the main analog building block of this ADC. Unlike flash ADCs, comparators in this ADC are not always running. Hence, a comparator structure without static power consumption is selected. Fig. 11 depicts the schematic of the 4-input dynamic comparator. The regeneration latch placed above the input pair amplifies the difference between input and reference signals into digital level. Compared to comparators with multiple or static current paths [7], there is only one dynamic path in the employed one, resulting in excellent power efficiency.

IV. Design Constraints of the ADC

This ADC must guarantee the total settling time is shorter than total comparison time in each stage. Under this constraint, the required reference voltages are settled before the next comparison. The total reference settling time contains the control signal generation time and RC settling time of the references while the total comparison time is the sum of comparison time of the comparator and required gate delay. According to the aforementioned discussion, the control signal generation time is one AND gate delay. The required gate delay of the comparator is one OR gate delay. Thus, the constraint can be expressed as

$$T_{\mathrm{AND}} + T_{\mathrm{RC},n+1} < T_{\mathrm{cmp},n} + T_{\mathrm{OR}} \quad \text{where } n \geq 2 \tag{1}$$

where $T_{\mathrm{RC},n+1}$ is the RC settling time of the $(n+1)$th stage, $T_{\mathrm{cmp},n}$ is the comparison time of the nth stage and $T_{\mathrm{AND}}, T_{\mathrm{OR}}$ are the gate delays. T_{AND} and T_{OR} are small and similar values in an advanced CMOS process. Hence, only the comparison and settling time should be carefully concerned. In the worst case of the RC settling time, the maximum resistance node is at the middle of the resistor ladder and the maximum capacitance node is the input of a last stage comparator. Assume the total resistance of the ladder is R_{total}, the equivalent resistance at the middle of the ladder is $R_{\mathrm{total}}/4$. The maximum resistance $R_{\max}$ is $R_{\mathrm{total}}/4$ plus the on-resistance of a switch $R_{\mathrm{sw,on}}$. For an LSB comparator, there are 2^{N-2} switches connected to each input node where one switch is on and the rest are off. If the parasitic capacitance induced by an off switch is C_{sw}, the total capacitance is around $2^{N-2}C_{\mathrm{sw}}$. The settling behavior of an ideal RC system can be expressed as

$$V(t) = V(0) + [V(\infty) - V(0)]\,(1 - e^{-t/\mathrm{RC}}) \tag{2}$$

where $V(0)$ is the initial voltage, $V(\infty)$ the steady state voltage and RC the time constant. After simple modification, the expression is rewritten as

$$V(t) = V(0) + [V(\infty) - V(0)]\,(1 - 2^{-t/\Delta t}) \tag{3}$$

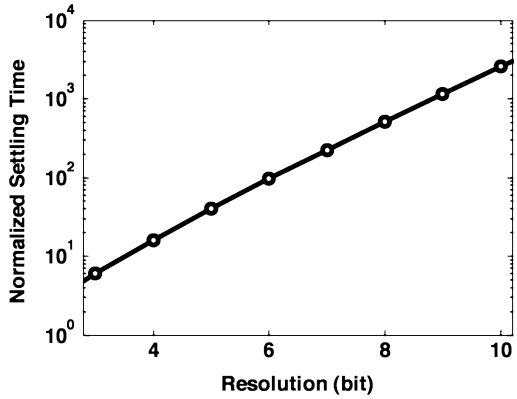

Fig. 12. Normalized settling time versus resolution.

where $\Delta t = \ln 2 \times \mathrm{RC}$ and Δt is the settling time for 1-bit accuracy. For an N-bit ADC, at least N times Δt is necessary to achieve enough accuracy. Therefore, the worst RC settling time is expressed as

$$T_{\mathrm{RC,worst}} = N \times \ln 2 \times R_{\max} C_{\max} \cong N \times \ln 2 \times \left(\frac{R_{\mathrm{total}}}{4} + R_{\mathrm{sw,on}} \right) 2^{N-2} C_{\mathrm{sw}}. \quad (4)$$

The estimation of the settling time is accurate because the reference network in this work is similar to a one-pole RC system. On the contrary, the estimation of the comparison time is more difficult. Although estimation based on the small-signal model is available in [5], the model is inaccurate when the input signal is large. Transistor level simulation is the most accurate way to extract the actual comparison time. The comparison time of a latch-based comparator is signal dependent. If the difference between the input signal and reference is large, the comparison time will be short. The shortest comparison time occurs when the difference is full scale. Note the shortest comparison time and worst settling time do not always occur simultaneously. However, the condition imposes a tight constraint on this ADC to ensure correct function. Take a 5-bit case as an example. If the simulated comparison time for a large input is 0.05 ns and C_{sw} is 5 fF, the total resistance must be smaller than 360 Ω according to (4). If the on-resistance of a reference switch is 200 Ω, then the resistance of the reference ladder should be less than 640 Ω. Equation (4) is mainly used to evaluate the ladder resistance since the ladder is the only building block consuming static power dissipation.

Fig. 12 illustrates the normalized settling time versus resolution, which shows an exponential dependence of the settling time to resolution. This trend indicates the difficulty of switching network design in high-resolution versions. Brutally reducing the RC time constant may result in the waste of static power dissipation. Incomplete settling or error tolerance techniques can be introduced to reduce the requirement of long settling time [5], [8].

V. Experimental Results

This prototype is fabricated in a 1P6M 65-nm CMOS process with metal-oxide-metal (MOM) capacitor. Fig. 13 shows the die

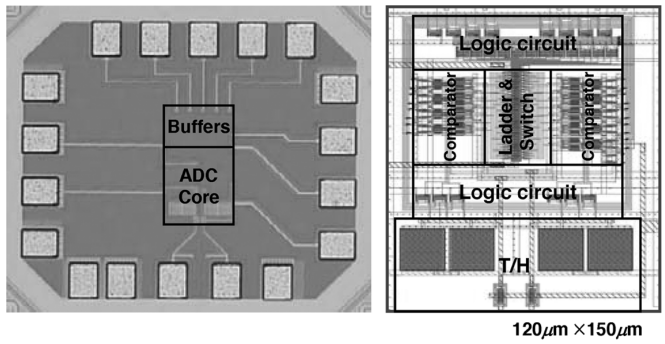

Fig. 13. Micrograph and ADC core layout.

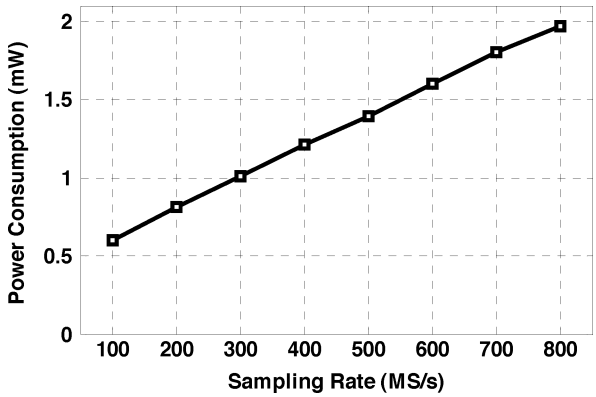

Fig. 14. Power consumption versus sampling rate.

micrograph and zoomed layout view of the ADC core which only occupies an active area of $150 \times 120\ \mu\mathrm{m}^2$. To stabilize the amplitude of input signals, an on-chip 100-Ω resistor is placed between the differential input ports to match the 50-Ω resistance of signal sources. The sampling capacitance of the passive T/H circuit is 1 pF. The nominal resistance of the reference ladder is 240 Ω for fast reference voltage settling. The reference voltages are externally applied. Since the clock signal is only applied to the sampling switches, first comparator and synchronous flip-flops, the small capacitive loading avoids on-chip clock buffers. To drive the probes of the logic analyzer, large inverter-based buffers serve as output driving circuits for the ADC.

The bare die is directly mounted on a PCB, and the pads of the die are connected to the traces of the PCB through bonding wires. To avoid the transmission loss of input and clock signals, the lengths of the PCB traces and bonding wires are minimized to reduce parasitic inductance. A pattern generator Agilent 81250 provides differential clocks for the ADC and a synchronous clock for the logic analyzer. At 800 MS/s, 20% of the period is sufficient for input signal sampling. The rest of the period is for the 5 comparisons. An RF signal generator Agilent E4438C produces single-ended sinusoidal signals which are then converted into differential form by an RF transformer. Two bias-tees provide the differential signals with the designated input common-mode voltage, 0.8 V. A logic analyzer captures the output data. Limited by the bandwidth of the data probes, the output data must be sampled at a lower frequency, 1/4 sampling frequency.

Excluding the output buffers, the active circuits and reference ladder totally consume 1.39 mW at 500 MS/s and 1.97

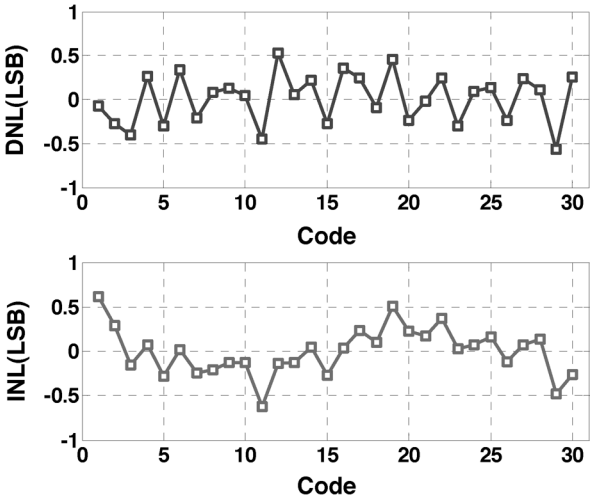

Fig. 15. DNL and INL at 800 MS/s.

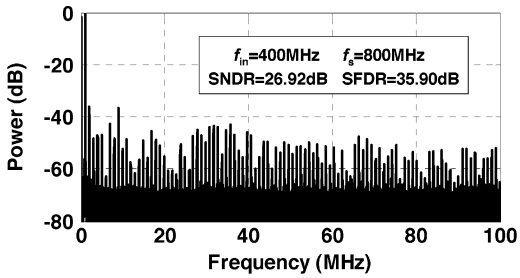

Fig. 16. Power spectrum at 400-MHz input and 800-MHz sampling.

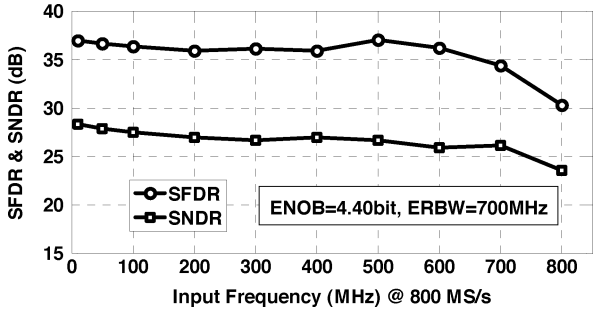

Fig. 17. SFDR and SNDR versus input frequency at 800 MS/s.

TABLE II
SPECIFICATION SUMMARY

Specification (Unit)	Experimental Result	
Supply Voltage (V)	1	
Input CM Voltage (V)	0.8	
Input Range (V_{pp})	0.6	
Sampling Capacitance (pF)	1	
Active Area (mm^2)	0.018	
Peak DNL / INL (LSB)	-0.56 +0.53 / -0.62 +0.61	
Sampling Rate (MS/s)	500	800
Power (mW)	1.39	1.97
ENOB (bit)	4.52	4.40
ERBW (MHz)	500	700
FOM (fJ/conv.-step)	121	116

mW at 800 MS/s. Fig. 14 displays the measured power consumption versus sampling rate. The relation between the power consumption and sampling rate is quite linear. Due to the resistor ladder, this ADC has static power consumption around 0.375 mW. Fig. 15 illustrates the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at 800 MS/s. The peak DNL is 0.56 LSB and the peak INL is 0.62 LSB. When the input frequency is around 400 MHz, the Nyquist frequency, this ADC achieves 26.92-dB signal to noise and distortion ratio (SNDR) and 35.90-dB spurious free dynamic range (SFDR) as shown in Fig. 16. Fig. 17 depicts the plot of the measured SNDR and SFDR versus input frequency. The drop of the SNDR from 10–700 MHz is only 2.17 dB, resulting in an effective resolution bandwidth (ERBW) over the Nyquist frequency. The effective number of bits (ENOB) is 4.40 bit and ERBW is 700 MHz at 800 MS/s. To evaluate the overall performance of the ADC, we use a well-known figure-of-merit (FOM) equation defined as

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times \min\{2 \times \mathrm{ERBW},\ f_s\}}. \tag{5}$$

The FOM at 800 MS/s is 116 fJ/conversion-step. When the sampling rate increases to 1 GS/s, the ENOB decreases to 4.2 bit because the comparison time left for the last stage is insufficient. At 500 MS/s, the ENOB is 4.52 bit and the ERBW is 500 MHz, yielding an FOM of 121 fJ/conversion-step. Table II shows the specification summary at 500 and 800 MS/s where the nominal input range is 600 mV. When the input range extends to 800 mV, the ENOB becomes 4.60 bit at 800 MS/s. However, the power consumption of the resistor ladder becomes larger when the input range extends.

Table III lists the comparison of this work to other state-of-the-art high-speed power-efficient 5-bit to 7-bit ADCs [4]–[6], [9]–[12]. The table shows the SAR architecture is the most popular solution for high-speed power-efficient analog-to-digital conversion [4], [5], [11]. These time-interleaved SAR ADCs have at least two channels for high operation speed, where one of them even has 36 channels [11]. The disadvantages of the time interleaved structure are the offset, gain, linearity, and timing mismatches between channels [13]. To alleviate these mismatches requires additional hardware or external trimming. For single-channel architecture, flash and folding ADCs are still taking the leading place [9], [10]. According to this table, this prototype occupies a very small die area and achieves good power efficiency [12]. For the same power consumption limit and technology, the proposed architecture shows higher speed potential than the SAR type ones.

VI. CONCLUSION

The proposed binary-search ADC overcomes the disadvantage of the original binary-search ADC: the exponential growth of comparators with resolution. The design difficulty is shifted from the analog circuit design (comparator) to digital one (reference switching network). The low capacitive loading of the

TABLE III
COMPARISON TO STATE-OF-THE-ART LOW-RESOLUTION HIGH-SPEED ADCS

Specification (Unit)	Chen *ISSCC'06*	Vebruggen *VLSI'08*	Vebruggen *ISSCC'08*	Cao *ISSCC'08*	Ginsburg *ISSCC'08*	Van der Plas *ISSCC'08*	This Work *ISSCC'09*
Supply Voltage (V)	1.2	1	1	1.2	0.8	1	1
Power (mW)	5.3	7.6	2.2	32	1.2	0.133	1.97
Sampling (GS/s)	0.6	1.75	1.75	1.25	0.25	0.15	0.8
ENOB (bit)	5.36	4.85	4.67	5.52	4.60	6.40	4.40
ERBW (MHz)	4000	2000	878	400	125	270	700
FOM (fJ/conv.-step)	220	150	50	871	197	10.4	116
Architecture	SAR	Flash	Folding	SAR	SAR	Two-Step	BS
Channel No.	2	1	1	2	36	1	1
Resolution (bit)	6	5	5	6	5	7	5
Area (mm^2)	0.06	0.031	0.017	0.09	2.8	0.055	0.018
Technology	0.13 μm	90 nm	90 nm	0.13 μm	65 nm	90 nm	65 nm

proposed work also alleviates the design difficulty of the sampling circuit. Compared to the flash ADC, the proposed architecture has lower hardware overhead and better power efficiency. The binary-search ADC also shows higher speed potential than a SAR ADC. Thus, this work is a balanced structure between flash and SAR ADCs. The fabricated prototype demonstrates the power efficiency (around 100 fJ/conversion-step) and high-speed potential (up to 800 MS/s) of an asynchronous binary-search ADC with reference range predication. Moreover, this ADC can serve as the core slice of a time-interleaved architecture. Small area and low power at nearly 1-GS/s could enable higher throughput of the same resolution at low power.

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