A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique

Jin-Fu Lin, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*, Chun-Cheng Liu, *Student Member, IEEE*, and Chih-Hao Huang

***Abstract*—In this brief, a split-capacitor correlated double sampling (SC-CDS) technique is proposed to improve the performance of CDS. Using the proposed technique, low-gain operational amplifiers (op-amps) can be employed to implement a low-power pipelined analog-to-digital converter (ADC). A power-efficient class-AB pseudodifferential op-amp and its corresponding integrator-based common-mode stabilization (IB-CMS) method are developed to further reduce the power consumption of the ADC. The proposed pipelined ADC fabricated in a pure digital 0.18-μm 1P5M CMOS process consumes 18 mW at 60 MS/s from a 1.8-V power supply. The active die area is 0.84 mm^2.**

***Index Terms*—Class AB, correlated double sampling (CDS), pipelined analog-to-digital converter (ADC), pseudodifferential.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) have low input capacitance, high-speed concurrent operation, and hardware complexity that linearly increases with resolution. Accordingly, among various ADC structures, the pipelined ADC is a popular architecture, because it achieves high speed and resolution while maintaining area efficiency and low power consumption. As a result, it is a suitable architecture for implementing ADCs for video and communication applications.

A conventional pipelined ADC requires power-hungry high-gain operational amplifiers (op-amps) to accomplish accurate analog signal processing, making it unsuitable for low-power designs. Correlated double sampling (CDS) is an analog op-amp gain error correction technique [1]. Using CDS, low-gain amplifiers can be employed to implement a high-accuracy low-power pipelined ADC. However, the conventional CDS technique has two problems, i.e., the double-loading problem and the requirement of three operating phases. These two problems have been resolved in the time-shifted CDS technique [2], which, however, has other problems, such as an additional signal-dependent offset and the requirement of a half-rate sample-and-hold amplifier (SHA). In [3], a time-aligned CDS technique was proposed to partially solve these problems. Correlated level shifting [4] was proposed to deal with the problems of existing CDS techniques, but it cannot reduce the dc offset and flicker noise of applied circuits. In this brief, a split-capacitor CDS technique is proposed to overcome the problems of the aforementioned CDS techniques.

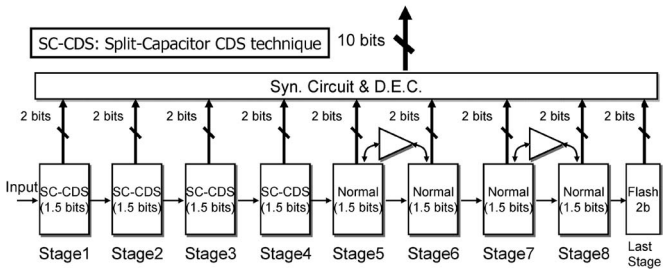

Fig. 1. Architecture of the proposed pipelined ADC.

A low-gain class-AB pseudodifferential op-amp architecture is also proposed to further reduce the power consumption of the proposed pipelined ADC. In order to stabilize the output common-mode (CM) voltage of the pseudodifferential architecture, an integrator-based CM stabilization (IB-CMS) technique is developed. Only one low-gain amplifier is required for the integrator. The proposed method is simpler than Chiu's method in [5].

The rest of this brief is organized as follows. Section II introduces the architecture of the proposed pipelined ADC. Section III briefly reviews existing CDS techniques and then describes the proposed split-capacitor CDS technique in detail. Potential problems and their solutions for the SHA-less architecture are addressed in Section IV. The low-gain class-AB pseudodifferential op-amp and its corresponding IB-CMS technique are described in Section V. Section VI shows the measurement results of the proposed pipelined ADC. Finally, the conclusion is given in Section VII.

II. Architecture of the Proposed Pipelined ADC

Fig. 1 shows the architecture of the proposed pipelined ADC. A 1.5-b/stage architecture is adopted for high-speed low-complexity operation. The front-end SHA is eliminated to reduce the power consumption of a pipelined ADC. Because the required accuracy of the latter pipelined stages is gradually relaxed, the proposed split-capacitor CDS technique can only be applied for the first four stages. For further reducing

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power consumption, the op-amp-sharing technique is employed in the latter stages to reduce the number of required op-amps [6]. Only low-gain amplifiers are used in the proposed pipelined ADC.

III. Split-Capacitor CDS Technique

The conventional switched-capacitor multiplying digital-to-analog converter (SC-MDAC) requires a high-gain op-amp to perform the high-accuracy charge transfer process. To avoid using high-gain amplifiers, the conventional CDS technique is employed to correct the finite op-amp gain error of low-gain amplifiers [1]. This technique needs three phases, i.e., sampling, predictive amplification, and main amplification phases, to perform its function. In the predictive amplification phase, the finite op-amp gain error is predicted and stored with additional capacitor. During the main amplification phase, the error-compensated output is performed with the help of the capacitor stored gain error. To correctly predict the op-amp gain error, the main and predictive capacitors need to sample the input signal at the same time, causing double loading in the preceding stage. Therefore, these problems, including the double-loading problem and the requirement of three operating phases, slow down the circuit operation and increase power consumption.

The time-shifted CDS technique, which rearranges the timing scheme, has been proposed to overcome these problems [2]. However, the main and predictive capacitors sample the main amplifying output $V_{\rm in}$ and the predictive amplifying output $V_{\rm in\_p}$ of the preceding stage in different sampling phases, respectively. The difference between $V_{\rm in}$ and $V_{\rm in\_p}$ is gradually accumulated in the latter pipelined stages, which not only degrades the gain error correction ability of the time-shifted CDS technique but also induces an additional signal-dependent offset. Furthermore, when the time-shifted CDS technique is applied in the first pipelined stage, a half-rate SHA is required to provide the same input for the predictive and main amplifying paths of the first stage. This SHA increases the total noise and power consumption of a pipelined ADC.

To overcome the problems of the time-shifted CDS technique, the time-aligned CDS technique is proposed, as shown in Fig. 2 [3]. The main architecture of this technique is the same as that of the conventional CDS technique. The time-interleaved operation is adopted to equivalently increase the operation speed. C_{s_p} and C_{f_p} are shared between two channels. An additional empty phase is inserted to simplify the timing arrangement. Due to the time-interleaved operation, the error-compensated output $(V_{o,a1}/V_{o,a2})$ is performed every two clock phases. Because the main and predictive capacitors both sample the main amplifying output, i.e., the error-compensated output, of the previous stage, all the aforementioned problems of the time-shifted CDS technique are overcome, except for the double-loading problem.

In this brief, a split-capacitor CDS technique is proposed to overcome the double-loading problem of the time-aligned CDS technique. The split-capacitor CDS has the same timing arrangement as that of the time-aligned CDS. Fig. 3 shows the configuration of the successive three pipelined stages with split-capacitor CDS in phases 1 and 2. In phase 1, $C_{f1,i-1}$ and

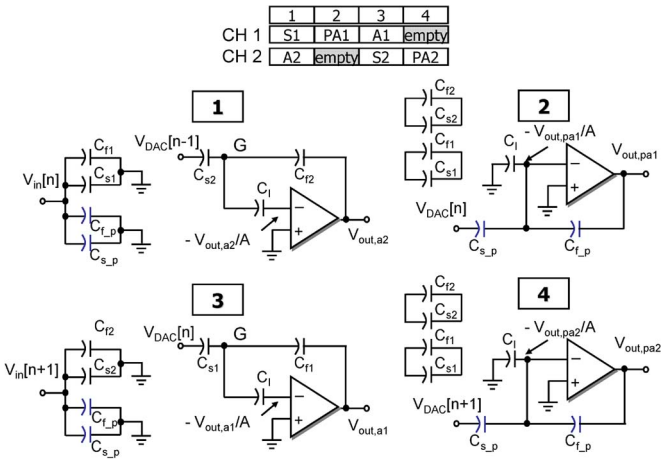

Fig. 2. Block diagram of the MDAC with the time-aligned CDS technique [3].

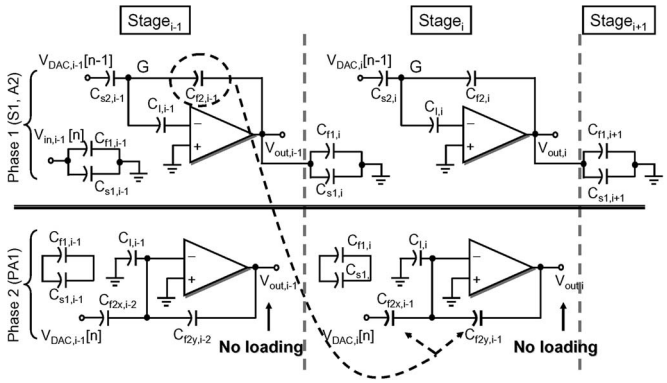

Fig. 3. Block diagram of the MDAC with the proposed split-capacitor CDS technique.

$C_{s1,i-1}$ sample the main amplifying output of its previous stage $V_{{\rm in},i-1}[n]$, and $C_{f2,i-1}$, $C_{s2,i-1}$, and $C_{I,i-1}$ act as the main amplifying outputs corresponding to $V_{{\rm in},i-1}[n-1]$. $C_{f2,i-1}$ also acts as a sampling capacitor for the next stage. Therefore, it is used to sample $V_{{\rm out},i-1}$, replacing the role of C_{f_p} and C_{s_p} shown in Fig. 2. This implementation is similar to that in [7]. Therefore, only $C_{f1,i}$ and $C_{s1,i}$ are required to sample $V_{{\rm out},i-1}$ in $stage_i$. In phase 2, $C_{f2,i-1}$ is split into $C_{f2x,i-1}$ and $C_{f2y,i-1}$, and configured to perform the predictive amplifying operation in $stage_i$. As a result, the internal pipelined stages, except for the first stage, do not suffer double loading in the proposed split-capacitor CDS. The capacitor value must be scaled down by 2 in the successive stages with split-capacitor CDS. However, due to the physical limitations and matching requirement of the capacitor, it cannot continuously be scaled down. For this reason, the proposed technique is only applied in the first four stages.

It is noteworthy that the first stage requires dedicated capacitors (C_{f_p} and C_{s_p}) to perform the predictive amplifying operation. This seems to cause double loading in the previous circuit of the first stage. However, compared with the time-shifted CDS technique, a dedicated half-rate SHA is not required in the proposed technique. A SHA-less architecture is adopted, which reduces the total noise and required capacitor values. Assume that all pipelined stages use the same capacitor

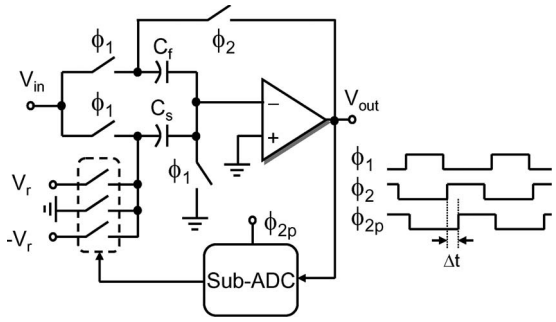

Fig. 4. Block diagram of the MDAC circuit with the embedded SHA technique [9].

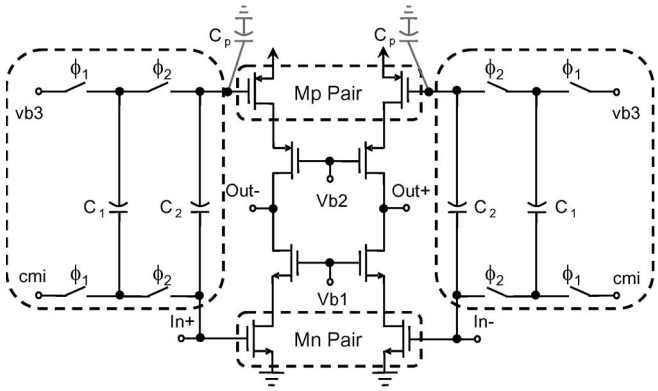

Fig. 5. Pseudodifferential class-AB telescopic cascoded op-amp.

value and that the total noise of the first three stages and SHA dominates that of the whole ADC. Only KT/C noise is considered here to simplify analysis. Based on a fixed noise budget, the relationship between the required unit capacitor values of the 1.5-b/stage MDAC in the time-shifted CDS $C_{\rm TS}$ and those used in the proposed technique $C_{\rm split}$ can be derived as

$$C_{\rm TS} = \frac{21}{5} C_{\rm split}. \tag{1}$$

A larger $C_{\rm TS}$ is required in the time-shifted CDS technique when the same input capacitance is assumed for the two pipelined ADCs. Moreover, when the op-amp noise is considered, the $C_{\rm TS}$ would even be larger due to the additional op-amp noise of the SHA. As a result, the proposed technique is more power efficient than the time-shifted CDS, even though the double input capacitance of stage 1 still exists. It should be noted that, when the preceding circuit of a pipelined ADC, such as an anti-aliasing filter or programmable gain amplifier, is implemented with the switched-capacitor topology, the dedicated predictive amplifying capacitors of the first stage can be implemented with the feedback capacitor of preceding circuit of a pipelined ADC, as is the case in Fig. 3.

IV. Design Issues of SHA-Less Architecture

Because the main and predictive capacitors in the proposed split-capacitor CDS technique sample the input signal at the same time, a half-rate front-end SHA is not required, which significantly reduces the power consumption of an ADC. However, a SHA-less architecture induces an additional signal-dependent offset [8]. The embedded SHA technique is adopted to overcome this problem, as shown in Fig. 4 [9]. The input of sub-ADC is connected to the output of the MDAC. When ϕ_1 is high, the input signal is sampled by C_s and C_f. When ϕ_2 is high and ϕ_{2p} is low, C_f is connected to the output of the MDAC, and sub-ADC is not activated. In the meantime, the left side of C_s keeps floating, and no charge on C_s is transferred to C_f. As a result, the MDAC becomes a SHA topology. When ϕ_{2p} is high, the sub-ADC processes the MDAC output, which is the held signal of the input signal. When the sub-ADC accomplishes the conversion, the voltage on the left side of C_s is decided, and the MDAC returns to normal operation. With the help of the embedded SHA, no additional signal-dependent offset is induced. Compared with a standalone SHA, no additional noise is induced in this technique.

However, the SHA period Δt reduces the settling time of the MDAC output, which significantly increases the power consumption of a pipelined ADC. When this technique is applied in the MDAC with split-capacitor CDS, this problem is insignificant, because the following phase of the sampling phase is the predictive amplifying phase in split-capacitor CDS. The MDAC in the predictive amplifying phase has no additional sampling capacitor from the successive stage, and its loading thus becomes very small. The transconductance of the single-stage op-amp is proportional to $C_L/t_{\rm settling}$, where C_L is the output loading and $t_{\rm settling}$ is the settling time. In this brief, the ratio of total loadings in the predictive and main amplification phases for stage 1 is about one third when the capacitors of stage 2 are scaled by 2 and op-amp parasitic capacitors are not considered. This indicates that the settling time of the MDAC in the predictive amplification phase is only one-third times that of the MDAC in the main amplification phase. Because Δt is 2 ns in this work, the residual settling time for the predictive amplification of the MDAC is sufficient for the maximum sampling rate of 60 MS/s. A large timing budget is preserved for higher operating speed. As a result, although the SHA period Δt reduces the settling time of the predictive amplification output, the resulting additional settling error of the predictive amplification is small, compared with that of the conventional implementation shown in Fig. 4.

V. Pseudodifferential OP-AMP Architecture

Using the proposed split-capacitor CDS, low-gain amplifiers are employed to implement a low-power pipelined ADC. A single-stage pseudodifferential telescopic cascoded amplifier is adopted because of its high power-efficiency and large signal swing. The circuit architecture is shown in Fig. 5. Additional class-AB capacitors C_1 and C_2 are employed to further enhance the dc gain and bandwidth of the amplifier. The equivalent transconductance Gm of the amplifier is

$$Gm = gm_N + \left(\frac{C_1 + C_2}{C_p + C_1 + C_2}\right) gm_P \tag{2}$$

where gm_N and gm_P are the transconductances of Mn and Mp, respectively. The equivalent transconductance is proportional to the ratio of the parasitic capacitor of PMOS C_p and the class-AB capacitor $(C_1 + C_2)$.

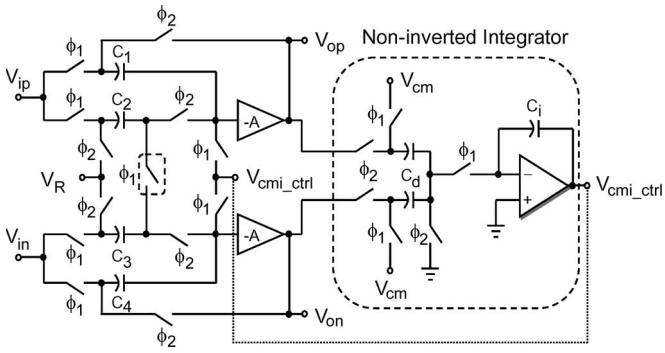

Fig. 6. Block diagram of the proposed integrator-based CM stabilization method.

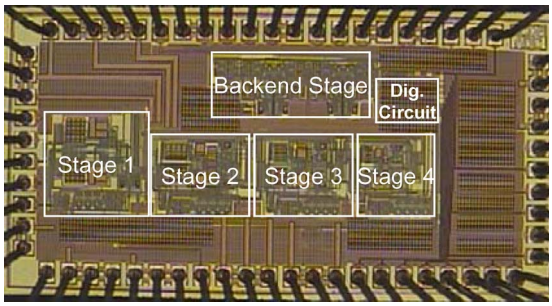

Fig. 7. Die photograph.

The output common voltage of the pseudodifferential amplifier without a tail current source is sensitive to CM disturbance. In this brief, an IB-CMS method is proposed to stabilize the output CM voltage of the pseudodifferential circuit. Fig. 6 shows the conventional pseudodifferential MDAC topology with the proposed IB-CMS method (the split-capacitor CDS topology is not shown in Fig. 7 for clarity). The floating sampling scheme is adopted to reduce the CM gain of the MDAC [2]. Because the right sides of C_2 and C_3 are connected with one floating switch (surrounded by the dashed line) in the sampling phase ϕ_1, the CM gain of the MDAC is unity. Any input CM disturbance of the MDAC is directly transferred to the output without amplification. To further regulate the output CM voltage, an additional noninverted integrator is used. In the amplifying phase ϕ_2, sampling capacitors C_d of the integrator sample the output CM voltage of the MDAC. In the sampling phase ϕ_1, the variation of the output CM voltage is updated into the integrated capacitor C_i. $V_{\rm cm}$ is the ideal output CM voltage. The resulting integrator output ($V_{\rm cmi\_ctrl}$) are sampled by C_1 and C_4 in ϕ_1. As a result, a CM regulated feedback loop is performed to stabilize the MDAC output CM voltage level. The transfer function of the CM regulated feedback loop can be derived as

$$H_{\rm cm}(z) = \frac{C_i - C_i z^{-1}}{C_i + (C_d - C_i)z^{-1}}. \quad (3)$$

The CM gains for the dc and Nyquist-rate CM variations are 0 and $2C_i/(2C_i - C_d)$, respectively. The dc CM variation can fully be suppressed, and the high-frequency CM variation is directly transferred to the following stages without amplification when C_i is much larger than C_d. This implementation

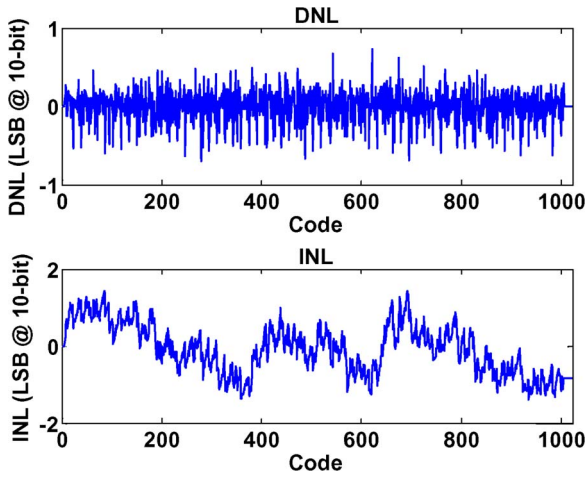

Fig. 8. Measured DNL and INL.

also ensures a stable response, because the pole is located within the unit circle in the z-transform analysis. Because the finite gain error and settling error of the integrator only reflect minor variation on the output CM voltage, a low-gain (25 dB) low-bandwidth (one-tenth op-amp bandwidth) amplifier is employed in the regulated integrator. As a result, the integrator does not consume much power.

VI. Measurement Results

The prototype, which was a 10-bit 60-MS/s pipelined ADC, was fabricated in a 0.18-μm 1P5M pure digital CMOS process. All capacitors were of metal–oxide–metal type to reduce fabrication cost. Fig. 7 shows a photograph of the die. The active die area occupies 0.84 mm^2. The power consumption is 18 mW from a 1.8-V power supply at 60 MS/s. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 8. The absolute peak DNL and INL are 0.73 LSB and 1.44 LSB, respectively. From the INL profile, the positive gain error caused by capacitor mismatch in stage 1 is the dominant error source of the ADC performance degradation. The dynamic performance versus input frequency at 60 MS/s is shown in Fig. 9. The signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) at a 20-MHz input frequency are 53.6 and 64.8 dB, respectively. The effective number of bits (ENOB) is 8.61 bits. At a 50-MHz input frequency, the ADC performance is degraded due to the sampling timing mismatch of the two channels in stage 1. Fig. 10 shows the SNDR/SFDR versus the input CM voltage plot. Even under large input CM variation, the proposed pipelined ADC maintains stable performance. This result demonstrates the effectiveness of the proposed IB-CMS method.

A performance summary of the proposed pipelined ADC is given in Table I. Table II shows the performance comparison of the proposed ADC and published 10-bit pipelined ADCs fabricated in the 0.18-μm process. The proposed ADC has high power efficiency, compared with those of other works, i.e.,

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot F_s}. \quad (4)$$

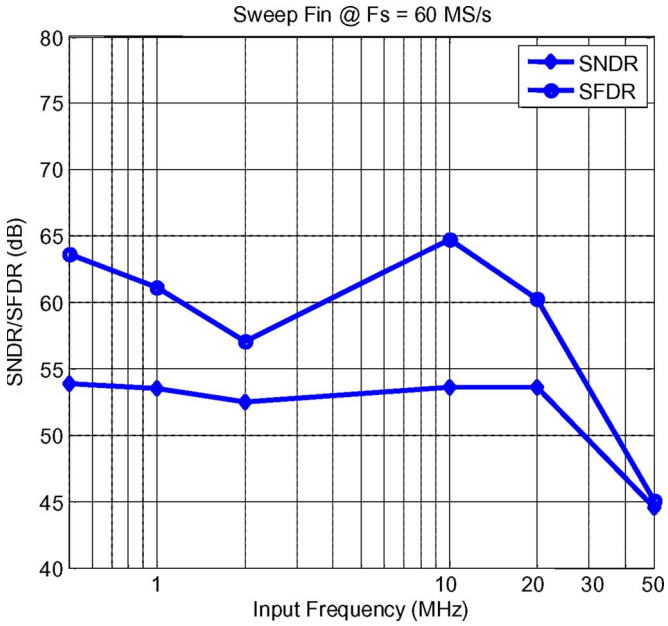

Fig. 9. Measured THD, SFDR, and SNDR versus input frequency (at Fs = 60 MS/s).

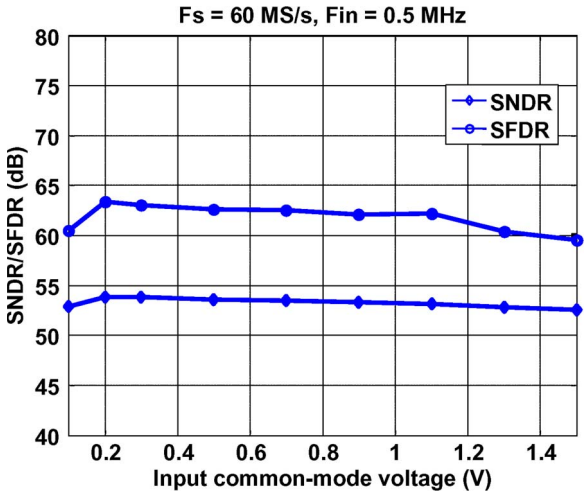

Fig. 10. Measured performance versus input CM voltage.

TABLE I
PERFORMANCE SUMMARY

Resolution	10 bits
Conversion Rate	60 MS/s
Maximum DNL/INL	0.73 LSB/ 1.44 LSB
Input Range	1.6 V_{pp} differential
SFDR @ fin=20 MHz	64.8 dB
SNDR @ fin=20 MHz	53.6 dB
Power Consumption	Analog: 13 mW Digital: 5 mW
Power Supply	1.8 V
Technology	0.18 μm CMOS 1P5M Process
Active Die Area	1.4 mm*0.6 mm

VII. CONCLUSION

The split-capacitor CDS technique has been proposed to overcome the double loading and additional operating phase problems of prior CDS techniques. A power-efficient class-AB pseudodifferential telescopic cascoded op-amp and its corresponding CM stabilization method have also been developed to further reduce the power consumption of the ADC. In the advanced CMOS process, two-stage op-amp topology would be used to achieve enough output signal swing at a low supply voltage. The class-AB capacitors can also be employed to enhance the bandwidth and dc gain of this op-amp with minor modification. By using short-channel high-speed devices, the pipelined ADC with the proposed techniques can achieve better FOM.

TABLE II
PERFORMANCE COMPARISON

10-bit pipelined ADC @ 0.18 μm Process					
Vdd (V)	Fs (MS/s)	Power (mW)	Active Area (mm^2)	FOM (pJ/step)	Ref.
1.8	30	22	0.7	1.26	[9]
1.8	150	123	2.2	2.46	[10]
1.8	50	18	1.43	0.61	[11]
1.8	100	67	2.5	1.64	[2]
1.8	100	50	2.2	1.95	[3]
1.8	60	18	0.84	0.77	This work

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