Low-Power and Wide-Bandwidth Cyclic ADC With Capacitor and Opamp Reuse Techniques for CMOS Image Sensor Application

Jin-Fu Lin, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*, Chin-Fong Chiu, Hann-Huei Tsai, and Jiann-Jong Wang

***Abstract*—In this paper, a power-efficient programmable gain amplifier (PGA) and a cyclic analog-to-digital converter (ADC) are developed for a satellite CMOS image sensor system. The cyclic ADC employs capacitor and opamp reuse techniques to reduce power consumption and occupied silicon area. Moreover, a power-efficient and wide-bandwidth telescopic cascode gain boosting amplifier with capacitive level shifters is adopted to decrease its power consumption further. According to the system specification, a 10-bit, 14-MS/s cyclic ADC with the front-end PGA circuit is implemented in the TSMC 0.18-μm triple-well 1P3M CMOS image sensor (CIS) process. The proposed cyclic ADC achieves a spurious free dynamic range (SFDR) of 65.1 dB and a signal-to-noise distortion ratio (SNDR) of 52.44 dB with 5-MHz input frequency at 14 MS/s. The power consumption of the cyclic ADC and PGA from a 3.3 V supply are 15.84 mW and 5.78 mW, respectively. The total core area is 0.381 mm^2.**

***Index Terms*—Analog-to-digital converter (ADC), CMOS image sensor, cyclic ADC, data converter, low power, programmable gain amplifier (PGA).**

I. Introduction

IMAGE sensors play an important role in today's satellite remote sensing applications, such as environment monitoring, disaster area evaluations, etc. Traditionally, the charge-coupled device (CCD) image sensor is a popular choice to serve as the image capture device due to its better dynamic range and uniformity. However, with the development of CMOS process, the performance of the CMOS sensor is improved significantly. Moreover, due to its low-power and easy-integration advantages, CMOS image sensors become a major competitor of the CCD technology. Since the satellite sensing system is powered by the solar cells, larger system power consumption must call for larger solar cells which increase the size and fabrication cost of a satellite. As a result, the low-power CMOS image sensor is preferred.

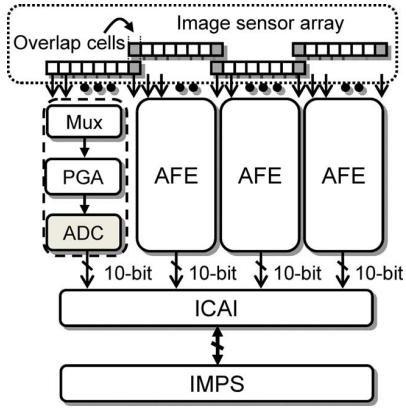

Fig. 1. Block diagram of the high-speed CMOS image sensor for the satellite application.

Fig. 1 shows the block diagram of the developed Formosa satellite image system,[1] which consists of a one-dimensional CMOS image sensor array including its analog front-end circuitry, an image combiner and acquisition interfaces (ICAI), and a system-on-chip image processing (IMPS). The one-dimensional line sensor array architecture, rather than a two-dimensional image sensor, is adopted in this system. Since a satellite rotates around the Earth at high speed, a two-dimension Earth image can be continuously fulfilled by employing the motion of the satellite, like a typical scanner operation. However, the long sensor array architecture imposes difficulties on semiconductor fabrication and package. To deal with these problems, the long sensor array is divided into four short strips. These image sensor strips are arranged in an interleaved form to avoid the spatial discontinuity. Some image sensors are overlapped to explicitly define assembling edges among substrips and conveniently calibrate the image assembling error with the ICAI.

For each short sensor strip, an analog front-end circuit is composed of an analog multiplexer (MUX), a programmable gain amplifier (PGA), and an analog-to-digital converter (ADC). The

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[1]The goal of this project is to develop the satellite image system and the corresponding critical techniques by integrating the research power of the academic and industry in Taiwan.

ADC is employed to convert the sensed signal to digital representation for further digital signal processing. Finally, the digital back-end ICAI circuit combines and calibrates the digitized image signal.

In this paper, low-power PGA and ADC are developed for reducing the loading of the satellite power system. In the developed system, each strip is comprised of 700 pixels CMOS sensor array and the frame rate is 8000 frame/s. The dynamic range needs to be higher than 50 dB. Accordingly, a 10-bit 8-MS/s ADC is at least required to meet the system specification. For the ADC integrated in the line sensor array system, there are two possible schemes: pixel-level ADC and single-channel ADC. The pixel-level ADC can achieve low-power operation [1]. However, this architecture usually suffers from large silicon area and fixed pattern noise (FPN). On the other hand, the single-channel ADC has opposite pros and cons compared with the pixel-level ADC. The pixel size of the architecture with the pixel-level ADC would be large for the high-speed operation within sufficient accuracy. As a result, to satisfy the requirement of the high frame rate and reduce pixel size in the developed system, a medium-speed single-channel ADC is preferred.

Among many popular ADC architectures, successive approximation (SA) ADCs [2], [3], cyclic ADCs [4], and pipelined ADCs [5] are possible candidates. The SA ADC consists of one comparator, passive capacitive DAC, and digital circuit and has low-power potential. However, a high-resolution SA ADC has disadvantages of the low operating speed and large input capacitance. The cyclic ADC has advantages of small die area and input capacitance, but its speed is as low as that of an SA ADC. The pipelined ADC can achieve high-speed operation, but occupy large die area. In this work, the cyclic ADC is selected because of its advantages of low input capacitance and small die area at the medium sampling rate.

To reduce the pixel size, gain-amplification and level-shifter functions are realized with a high-speed standalone PGA. A switched-capacitor (SC) PGA with eight gain modes (X1 to X8) is implemented by using a single operational amplifier (opamp). By increasing the sampling time of the cyclic ADC, the settling time of the PGA, therefore, is increased only at expense of minor additional capacitors. Moreover, the capacitor and opamp reuse techniques are proposed to reduce die area and power consumption of the cyclic ADC.

The rest of this paper is organized as follows. Section II describes the architecture of the proposed cyclic ADC. Section III introduces circuit implementations of other components. Finally, experimental results are discussed in Section IV, and conclusion is made in Section V.

II. Architecture of the Proposed Cyclic ADC

A. Conventional Architecture

Fig. 2 is the circuit diagram of a conventional cyclic ADC with the 1.5-bit/stage architecture. The ADC consists of two cascaded stages and the output of the second stage is fed back to the first one. These two stages convert signals from the output of each other until completing N-bit data conversions. In the first cycle, the first stage performs the dedicated sample-and-hold operation to provide a held signal for the second stage. Coarse

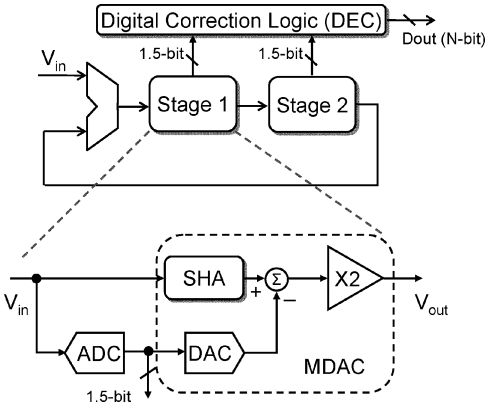

Fig. 2. Circuit diagram of an N-bit conventional cyclic ADC with a 1.5-bit/stage architecture.

quantization and residue amplification of the held signal are accomplished in the second stage. Then, the residue signal is passed to the first stage to do further quantization and amplification. Since it needs several algorithmic cycles to finish one complete conversion process for a given analog input signal, the throughput of a cyclic ADC is usually slow. However, the overall circuitry of a cyclic ADC is quite simple, and the occupied silicon area is small.

B. Review of Previous Loading-Free Technique [6]

In general, the power consumption of switched-capacitor (SC) circuits is proportional to the output capacitive loading. In [6], a loading-free technique has been proposed to reduce power consumption of a pipelined ADC. The basic idea behind this technique is that the feedback capacitor of the SC circuit in the present stage is served as the sampling capacitor of that in the next stage. As a result, the output loading of the present stage is only the equivalent capacitor of the feedback path, which significantly reduces the output loading of the present stage and power consumption.

Fig. 3 shows the circuit diagram of the loading-free technique in a switched-opamp pipelined ADC. With the help of the loading-free technique, no additional sampling capacitor for stage 2 is required to sample the output of stage 1. As a result, the loading of stage 1 can be expressed as

$$C_{L,1} \approx C_{f,1} || (2C_{LS,1} + C_{s,1}). \tag{1}$$

Because the output loading of a conventional SC circuit includes the sampling capacitor $C_{s,2}$ of stage 2 (not shown in Fig. 3), the output loading of the stage with loading-free technique is reduced significantly.

Since $C_{f,1}$ is flipped over to accomplish the MDAC operation of the stage 2 in $\phi 1$, it can not serve as the sampling capacitor of stage 1 at the same time, as the same operation of the conventional flip-around MDAC operation [7]. Therefore, only $C_{s,1}$ samples input signal, and the ratio of $C_{s,1}$ to $C_{f,1}$ is 2:1 to achieve X2 stage gain. The feedback factor (1/3) would be lower than that of the conventional flip-around MDAC (1/2). Moreover, due to the low-voltage operation, the DAC and level shifter capacitors (C_{LS}) are also required. As a result, the feedback factor of the circuits shown in Fig. 3 is lower (1/4). The low

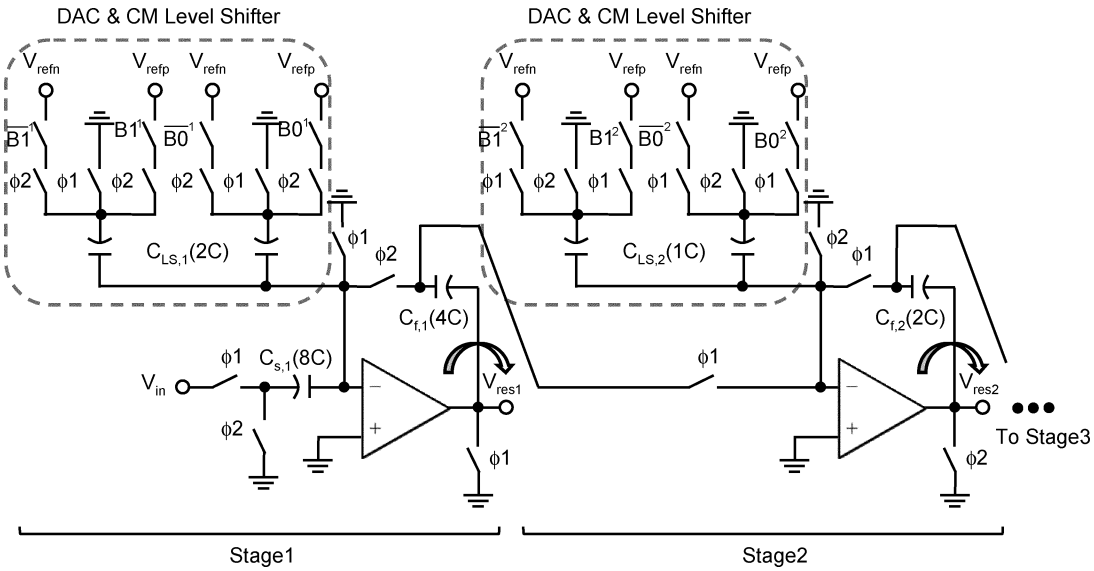

Fig. 3. Circuit diagram of the loading-free technique in a switched-opamp architecture.

feedback factor represents the low power efficiency. Because of this disadvantage, the low-power potential of the loading-free technique becomes unapparent.

In addition, right side of $C_{f,1}$ is directly connected to the output of stage 1. The opamp of stage 1 must be turned off in $\phi 1$ to avoid disturbing the MDAC operation of stage 2. For a low supply voltage operation, the switched-opamp technique could be employed to accomplish such a function. However, this architecture has slow operating speed limited by the slow wake-up operation. In the normal supply voltage, an additional switch can be inserted between the output of stage 1 and $C_{f,1}$ to overcome this problem. This solution can achieve high-speed operation compared with the switched-opamp architecture. However, additional switches in the signal path would still affect the settling behavior of an MDAC.

C. MDAC Architecture

An MDAC is the most critical component in a cyclic ADC. Fig. 4 shows two 1.5-bit/stage MDAC implementations. They have different input sampling schemes. In the sampling phase $(\phi 1)$, C_s and C_f sample input signal, and the opamp is configured as unity gain buffer in Fig. 4(a). Input signal, dc offset and low-frequency noise, such as flicker noise, are stored on the C_s and C_f. Therefore, the dc offset and flicker noise are cancelled in the amplifying phase $(\phi 2)$. The ideal MDAC transfer function is as follows:

$$V_{\text{out}} = \frac{C_s + C_f}{C_f} V_{\text{in}} + \frac{C_s}{C_f} V_r, \quad \{V_r : 0 \text{ and } \pm V_{\text{ref}}\} \quad (2)$$

where V_{in} is the input signal, and V_{ref} is the reference voltage of the ADC. The DAC value (V_r) depends on conversion results of the sub-ADC.

The digital error correction (DEC) technique is frequently used to relax the offset requirements of comparator and opamp [7]. With the help of the DEC technique, large offsets of opamps and sub-ADCs can both be tolerated. Therefore, if the opamp offset is within the tolerable range of the DEC technique, it just causes ADC system offset and does not cause any nonlinearity. As a result, the MDAC without the input offset storage technique, as shown in Fig. 4(b), can be implemented. The input and output of the opamp in Fig. 4(b) are only connected to common mode voltages in the sampling phase $(\phi 1)$. Advantages of the architecture in Fig. 4(b), compared with that in Fig. 4(a), are listed in the following.

1) The input and output common mode voltages can be different, which increases the flexibility in designing opamp.
2) The bandwidth of the sampling network is only determined by the turn-on resistance of switches and capacitors, which is independent of the opamp bandwidth. This feature can improve input bandwidth.
3) The opamp is idle in the sampling phase. As a result, power-efficient techniques such as opamp sharing and double sampling can be applied, [8], [9].

Based on the above-mentioned advantages, the MDAC shown in Fig. 4(b) is adopted in the proposed architecture. Moreover,

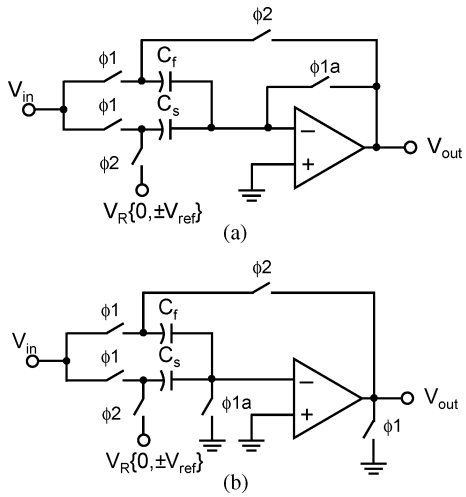

Fig. 4. (a) Circuit diagram of an MDAC *with* the input offset storage technique. (b) Circuit diagram of an MDAC *without* the input offset storage technique.

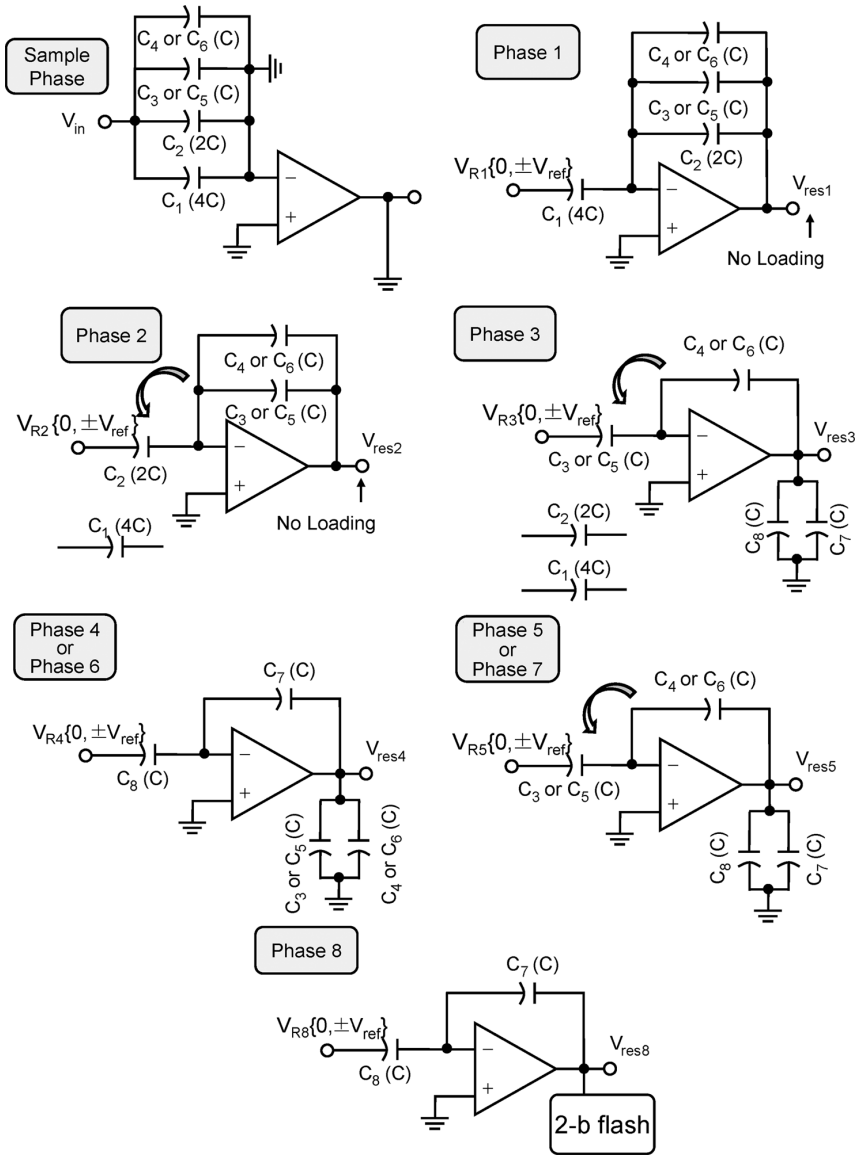

Fig. 5. Circuit diagram of the proposed 10-bit, 1.5-bit/stage cyclic ADC with the capacitor and opamp reuse techniques.

two stages can thus share a single opamp to significantly reduce power consumption and die area.

D. Proposed Capacitor Reuse Technique

In order to overcome disadvantages and enhance power efficiency of the previous loading-free technique, the capacitor reuse technique is proposed. The circuit diagram of the proposed technique is shown in Fig. 5. The ratio of C_1, C_2, C_3, and C_4 are 4:2:1:1. In the sample phase, all capacitors are used to sample the input signal. In phase 1, C_2, C_3, and C_4 become feedback capacitors connected to the output, and C_1 is connected to the DAC value (V_{R1}). Meanwhile, the feedback capacitors (C_2, C_3, and C_4) can act as sampling capacitors in the next cycle to sample output, and thus no additional sampling capacitor becomes the loading of amplifier. In phase 2, C_3 and C_4 still act as feedback capacitors, and C_2 is flipped over to connect the next DAC value (V_{R2}). V_{res2} can be sampled by C_3 and C_4, so no additional sampling capacitor in phase 2 is required. Based on

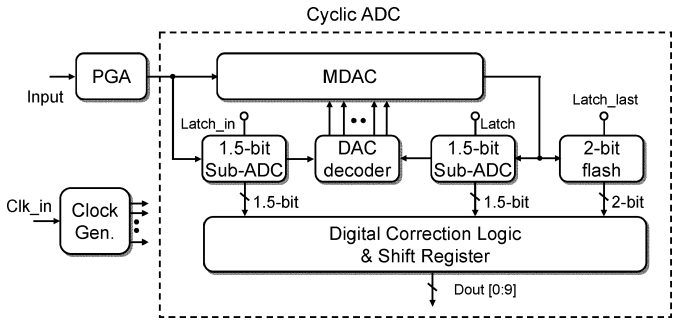

Fig. 6. Circuit diagram of the proposed cyclic ADC.

the same procedure, the feedback capacitor in the present cycle can be continuously served as the sampling capacitor in the following cycles. However, in order to achieve X2 stage gain of a 1.5-bit/stage architecture, the feedback and DAC capacitors must be continually scaled down by 2 in the following cycles.

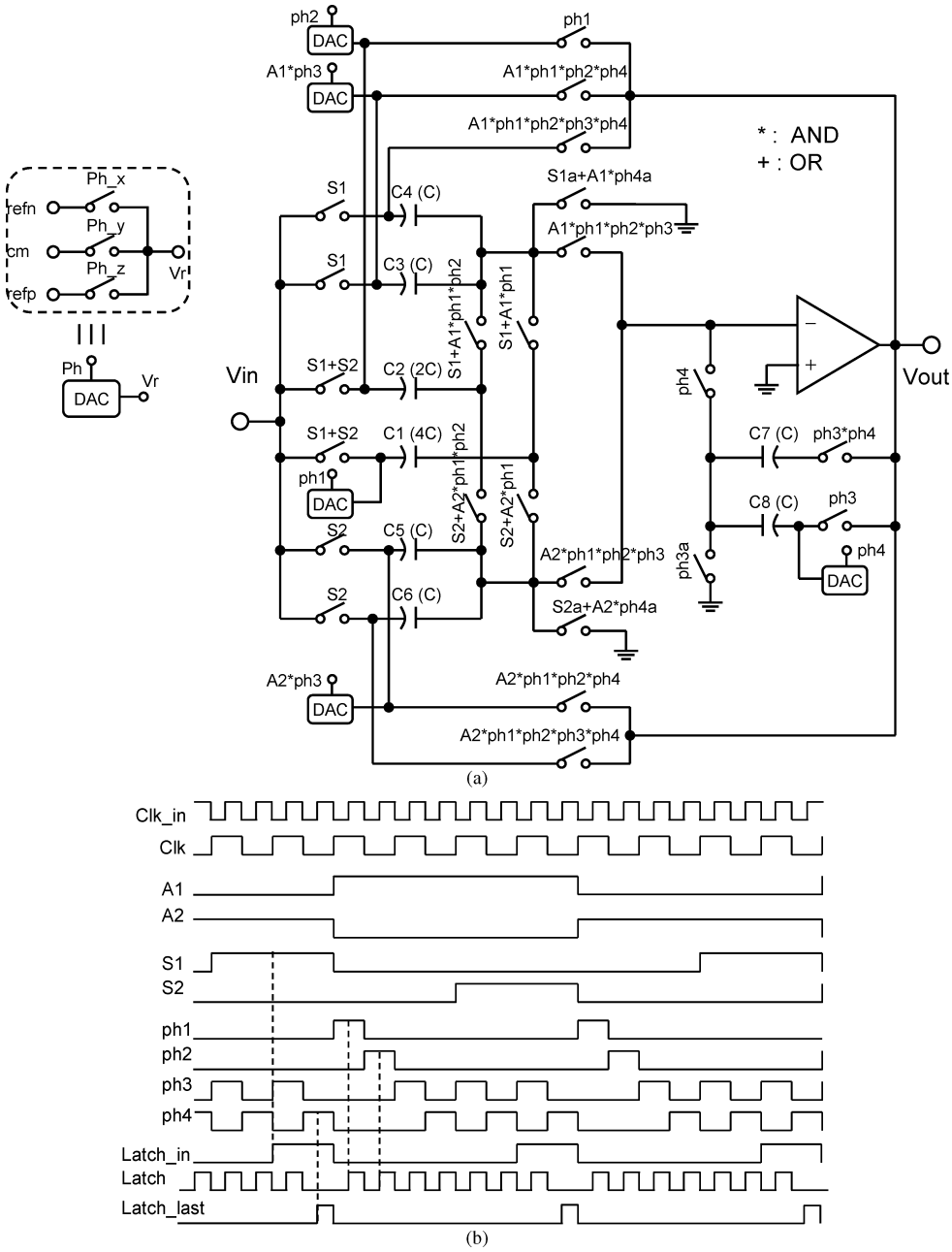

Fig. 7. (a) Detail schematic of the MDAC circuit. (b) Timing diagram of the proposed cyclic ADC.

The noise consideration and physical limitation would limit the minimum allowable capacitor. For this reason, the number of cycles using the capacitor reuse technique is limited.

In the proposed cyclic ADC, only phase 1 and phase 2 employ the capacitor reuse technique. In phase 3, additional capacitors (C_7 and C_8) are required to sample output voltage V_{res3} for the next cycle operation. In the following phases, the (C_7, C_8) and (C_3, C_4) are alternately configured as the sampling and MDAC operations. In phase 8, the last 2-bit flash ADC samples the V_{res8} and produces its corresponding coarse digital codes. One complete data conversion requires nine phases including one sampling phase and eight amplifying phases. Additional C_5 and C_6 are employed to extend the sampling period of the proposed cyclic ADC. They perform time-interleaved operation with C_3 and C_4.

It is noteworthy that the feedback capacitor samples not only output signal but also the dc offset and opamp finite gain error. The dc offset can be stored, like the offset cancellation shown in Fig. 4(a). In other words, the capacitor reuse technique has an inherent dc offset cancellation feature. Moreover, because the finite opamp gain error affects the sampling voltage in the feedback capacitor, the higher opamp DC gain is required to reduce the gain error.

The capacitor reuse technique applied for the proposed cyclic ADC has the following advantages compared with the previous loading technique [6].

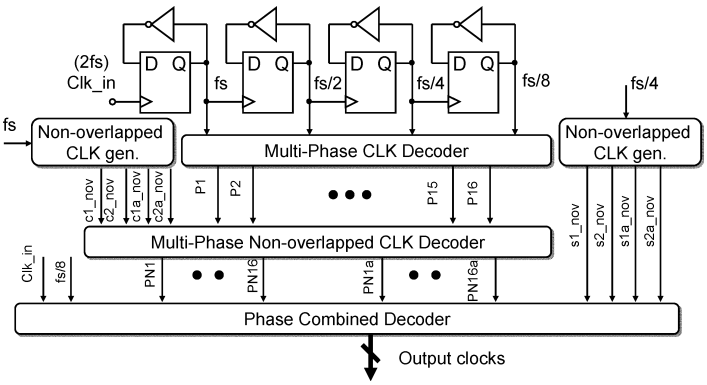

Fig. 8. Circuit diagram of the clock generator.

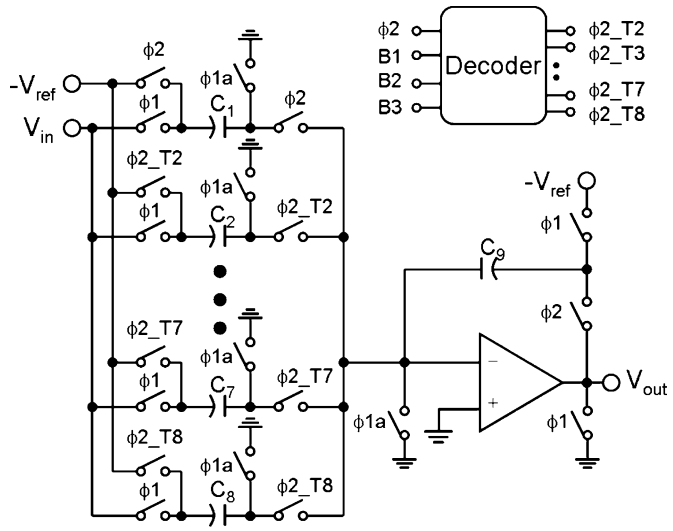

Fig. 9. Circuit diagram of the PGA.

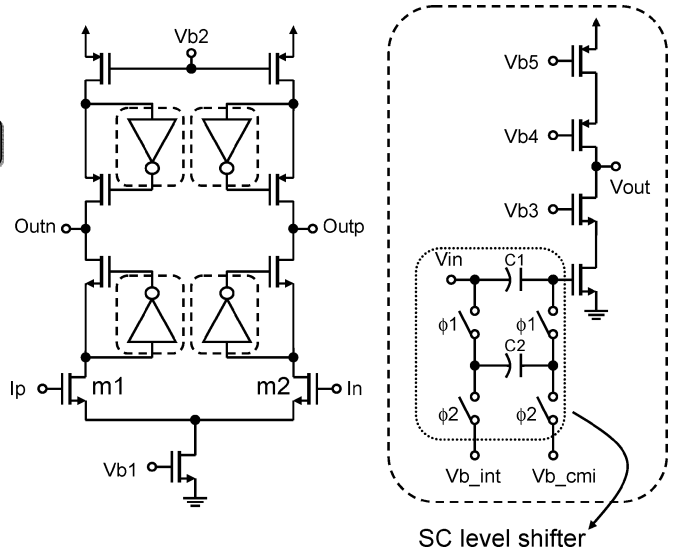

Fig. 10. Schematic of the high-gain and wide-bandwidth operational amplifier.

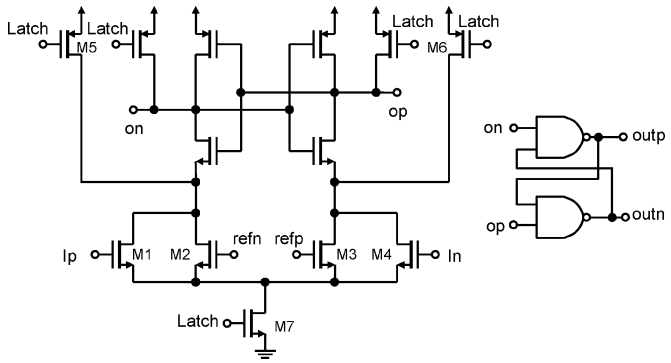

Fig. 11. Schematic of a dynamic comparator.

1) The feedback factor of the proposed circuit is 1/2, which is larger than that of the previous loading-free technique (1/4).
2) The feedback capacitors are flipped at the pivot of the opamp input, rather than the opamp output. Therefore, the opamp output does not disturb the operation at the previous cycle.

E. Circuit Diagram of the Proposed Circuit

The circuit diagram of the proposed circuit including the PGA and cyclic ADC is shown in Fig. 6. The input signal is level shifted and amplified by the PGA. The analog output of the PGA is converted to digital signal by the backend cyclic ADC. The PGA is implemented with a switched-capacitor circuit. The detailed implementation is described in the next section. The PGA can be served as the front-end sample-and-hold circuit to provide wide-bandwidth performance. The cyclic ADC only requires one MDAC circuit contained only one opamp, two 1.5-bit sub-ADCs, 2-bit flash ADC and digital circuits for the DAC decoder, DEC, and clock generator.

For clear explanation, the single-ended circuit diagram of the MDAC circuit in the proposed cyclic ADC is shown in Fig. 7(a). The practical implementation is a fully differential topology for better noise immunity. The required control signals corresponding to switches in Fig. 7(a) can be derived from clock phases in Fig. 7(b) by simple logical AND ($*$ symbol) and OR ($+$ symbol) operations. The CLK is the master clock, which four times the throughput rate of the cyclic ADC. The circuit operation follows nine phases shown in Fig. 5. To relax the settling time of the PGA, the period of sample phase of the cyclic ADC ($S1$ or $S2$) is extended. With the help of the capacitor-reuse technique, large part of capacitors can be reused. Only additional C_5 (C) and C_6 (C) are required. Die area overhead is quiet slight. (C_3, C_4) and (C_5, C_6) are employed for time-interleaved operation.

The circuit diagram of the clock generator is shown in Fig. 8. One clock input (clk_in) with double frequency of the system clock (CLK) is applied. The signals including fs, $fs/2$, $fs/4$, and $fs/8$ are generated by the cascaded frequency dividers and the clk_in. Sixteen phases clocks $(\mathrm{P1} \sim \mathrm{P16})$ are generated from these four signals with simple logic gates, then the multiphase nonoverlapped clock decoder is employed to produce nonoverlapped behavior for these 16 multiphase clocks. All control signals in the cyclic ADC are generated with the phase combined decoder and multiple nonoverlapped clock phases.

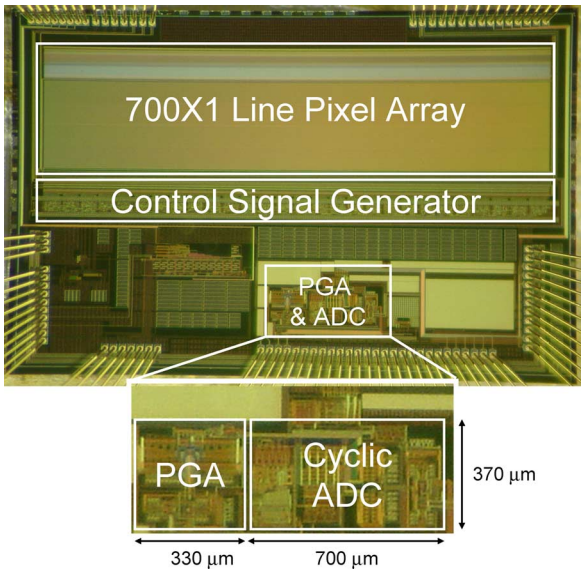

Fig. 12. Die photograph of the proposed PGA and cyclic ADC.

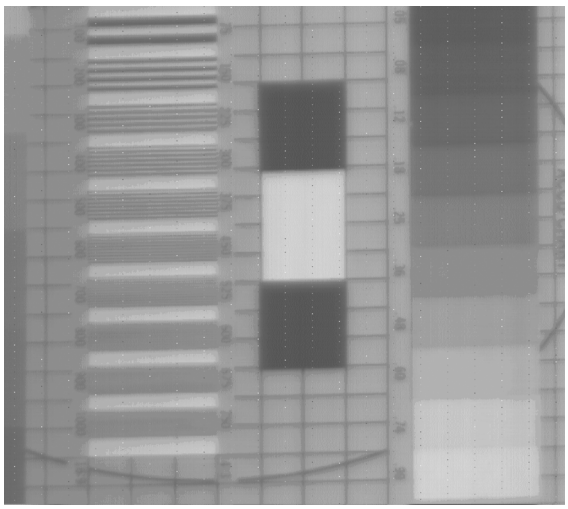

Fig. 13. Image captured with the column ADC.

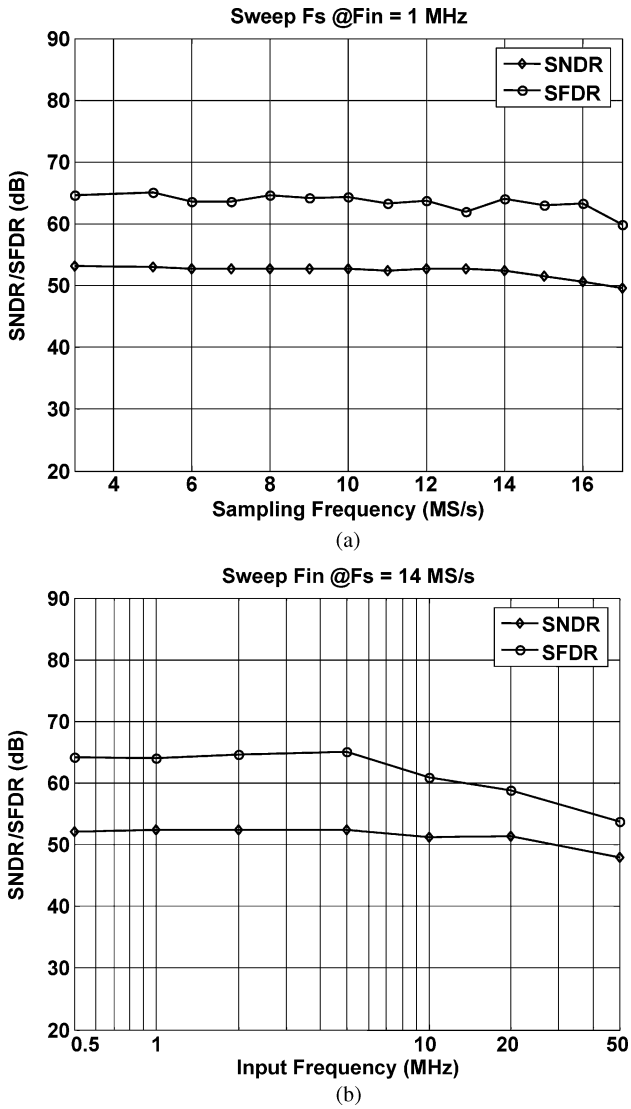

Fig. 14. Measured THD, SFDR, and SNDR versus (a) sampling rate ($@\mathrm{Fin} = 1\ \mathrm{MHz}$) (b) input frequency ($@\mathrm{Fs} = 14\ \mathrm{MS/s}$).

III. Circuit Implementations

A. Programmable Gain Amplifier (PGA)

To reduce the complexity of pixel analog readout circuits, functions of the gain amplification and the level shifter are accomplished by the standalone PGA circuit. The transfer function of the PGA is

$$V_{\mathrm{out}} = G(V_{\mathrm{in}} + V_{\mathrm{ref}}) - V_{\mathrm{ref}} \tag{3}$$

where V_{in} and V_{out} is the input and output of the PGA, respectively. V_{ref} is the reference voltage of the cyclic ADC. The programmable gain of the PGA (G) is designed as eight modes (X1 to X8) and controlled by 3 binary bits $(\mathrm{B1} \sim \mathrm{B3})$ according to the strength of the light source.

Fig. 9 shows the circuit diagram of the PGA. In $\phi 1/\phi 1a$ phase, to ensure constant input capacitance, which avoids influencing the settling behavior of the previous circuit, $C_1 \sim C_8$ are all used to sample input signal. Meanwhile, C_9 is precharged to $-V_{\mathrm{ref}}$, and the opamp is reset. In $\phi 2$, among sampling capacitors $(C_1 \sim C_8)$, specific capacitors would be selected to form feedback network and connected to $-V_{\mathrm{ref}}$ according to thermometer gain control bits. The unselected capacitors are floating. Through this implementation, only one active opamp is required to accomplish gain amplification and level shifter at the same time. When $\phi 2\_T2$ to $\phi 2\_T8$ are all low, the PGA becomes SHA configuration which has the highest feedback factor (1/2). On the other hand, when $\phi 2\_T2 \sim \phi 2\_T8$ are all high, the PGA has X8 of gain amplification, but has the lowest feedback factor (1/9). In order to cover the worst case, the bandwidth of the opamp must be designed according to the $G = 8$ configuration.

B. Operational Amplifier

Two opamps are required for the PGA and MDAC. The settling time of the MDAC is 1/4 of the PGA; however, the feedback factor of the MDAC is 9/2 of the PGA with the X8 mode. Hence, the opamps for the PGA and MDAC have similar

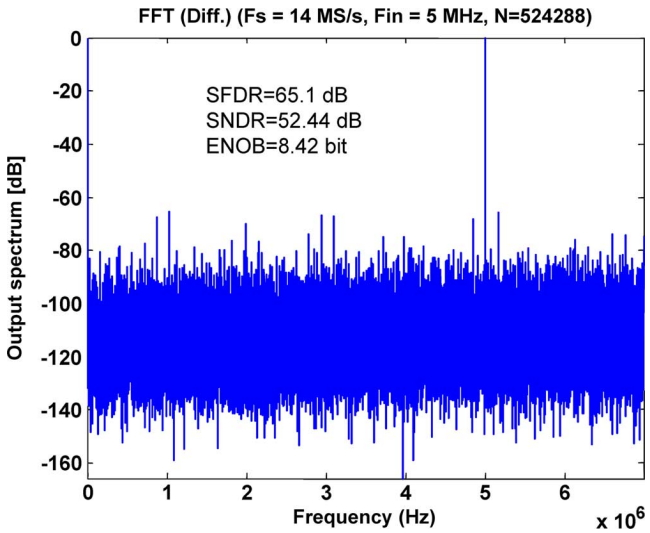

Fig. 15. The measured spectrum with 5-MHz input signal and at 14 MS/s.

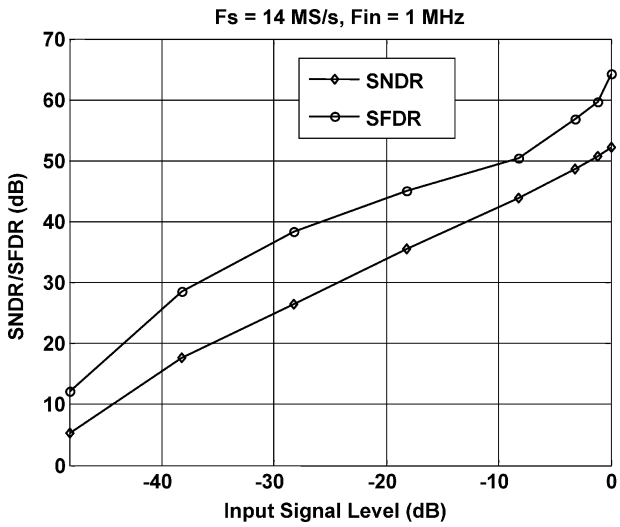

Fig. 17. SFDR and SNDR versus input signal level at 1-MHz input frequency and 14 MS/s.

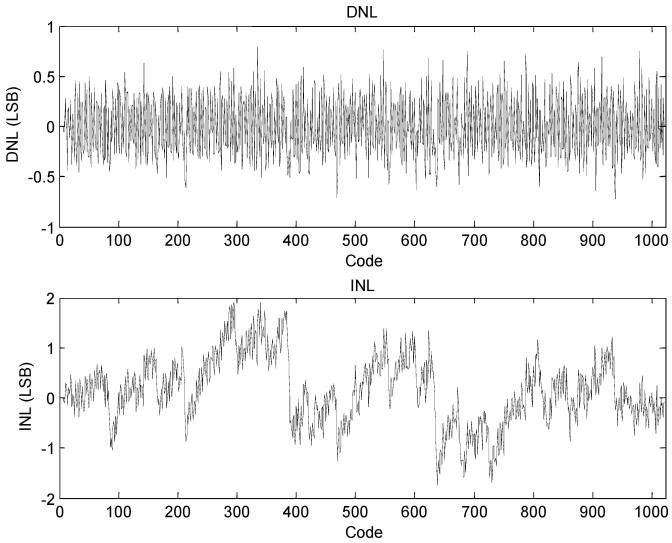

Fig. 16. The measured DNL and INL at 1 MHz input signal and 14 MS/s.

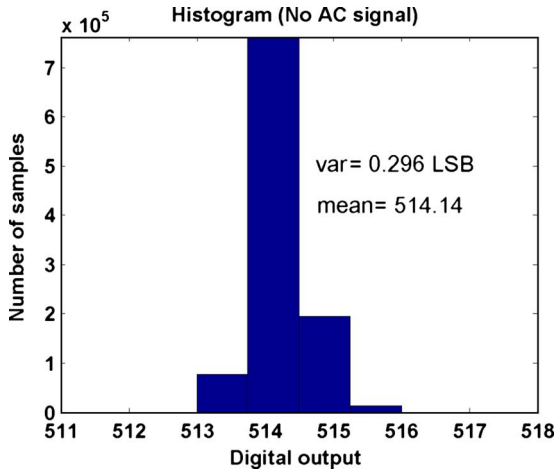

Fig. 18. Histogram of the digital output with zero input.

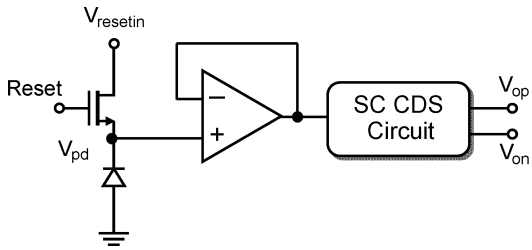

Fig. 19. Schematic of an active pixel senor.

specification and can be designed as the same one to reduce design effort. The circuit diagram of the opamp is shown in Fig. 10. Since the MDAC and PGA adopt the sampling scheme shown in Fig. 4(b), the input and output common mode voltages can be different. As a result, the power-efficient telescopic cascoded amplifier with narrow input common mode range (ICMR) can be used as the main amplifier. At the 3.3 V supply voltage, the 2.4 V_{pp} differential signal swing can still be achieved. The switched capacitor common mode feedback (SC-CMFB) is used to stabilize the output common mode of opamps [10]. Furthermore, the gain boosting amplifier is employed to increase the dc gain. The bias condition of the boosting amplifier is independent of that of the main amplifier due to the use of SC level shifter. Accordingly, all gain-boosted amplifiers can adopt wide bandwidth n-type cascoded amplifier [9]. The dominant pole of the opamp is at the output node, and no low-frequency second pole exists. Therefore, the phase margin of the opamp is high enough for the different feedback factor operations of the PGA. The $M1$ and $M2$ input transistors are the 1.8-V device to reduce the opamp input parasitic capacitors and speed up the circuit operation. This opamp has advantages of wide bandwidth and power efficiency. To suppress the memory effect of the opamp sharing architecture [9] and enhance the linearity of the MDAC, a high open-loop gain of the opamp is designed (100 dB).

C. Sub-ADC

Large comparator offset can be tolerated in a 1.5-bit/stage pipelined/cyclic ADC. The maximum tolerable offset is

TABLE I
PERFORMANCE SUMMARY OF CMOS IMAGE SENSOR

CMOS Image Sensor Specification		
Technology	TSMC triple-well 1P3M 0.18 μm CMOS image sensor (CIS) process	
Line Sensor Array Size	16 blocks	700 pixel/block
Pixel Pitch	6.5 μm	
Sensitivity	3.64 V/lux.s	
Fixed Pattern Noise	+2.73%/-2.7%	
Saturation Exposure	0.3604 V/lux.s	
Saturation Output Voltage	1.312 V	
Frame Rate	8000 frame/s	
Integration Time	120 µs	
Dynamic Range	> 50 dB	

$\pm 1/4\ V_{\rm ref}$ (300 mV) in the proposed circuit. Therefore, low-power, but possibly large-offset, dynamic comparator can be employed to implement sub-ADCs and the last 2-bit flash ADC. The circuit diagram of the dynamic comparator is shown in Fig. 11. The main architecture is a dynamic latch followed by an SR-latch. Its behavior is like an edge-triggered flip-flop. The input signal is sampled and amplified during the positive rising edge of the latch signal. Because of no dc biased pre-amp, large kickback noise would disturb the input signal during the positive rising edge of the latch signal. As a result, the rising edges of control signals for all sub-ADCs (*Latch_in* and *Latch*) and 2-bit flash ADC (*Latch_last*) are allocated at the middle point of the amplified phases of previous circuits, as shown in Fig. 7(b). Through this kind of timing arrangement, longer time is preserved to absorb the disturbance caused by the comparator kickback noise. The threshold voltage of the dynamic comparator is defined by the ratio of $M1 \sim M4$ transistor sizes as follows:

$$V_{\rm th} = \pm \frac{W_{\rm ref}}{W_{\rm in}} (V_{\rm refp} - V_{\rm refn}) \tag{4}$$

where $V_{\rm refp}$ and $V_{\rm refn}$ are the positive and negative reference voltages of the cyclic ADC. $W_{\rm ref}$ and $W_{\rm in}$ represent the input $(W1 = W4)$ and reference $(W2 = W3)$ transistor sizes, respectively. The threshold voltage $(V_{\rm th})$ is very sensitive to the process variation. Resetting transistors ($M5$ and $M6$) are added to ensure the $M1 \sim M4$ operated in the saturation region at the beginning of the rising edge of the latch signal. As a result, this refinement increases the transconductance of $M1 \sim M4$ and reduces the comparator offset [11].

IV. EXPERIMENTAL RESULTS

The proposed cyclic ADC has been fabricated in the TSMC 0.18-μm triple-well 1P3M CMOS image sensor (CIS) process. In order to reduce the light reflection and interference, only three metal layers are used in the whole chip. The die photograph is shown in Fig. 12. The core die area including the PGA and cyclic ADC occupies 0.381 mm^2. The power consumption of the cyclic ADC and PGA from a 3.3 V power supply at 14 MS/s are 15.84 mW and 5.78 mW, respectively. Fig. 13 shows the image captured with the developed CMOS image system.

The dynamic specifications, including signal-to-noise distortion ratio (SNDR) and spurious free dynamic range (SFDR), were analyzed by fast Fourier transform (FFT) with the MATLAB CAD tool. Specifications of the static linearity, including integral nonlinearity (INL) and differential nonlinearity (DNL), were measured based on the sinewave code density testing method [12]. Since the proposed PGA has the function of the embedded level shifter, the PGA must be configured as unity-gain SHA topology for the dynamic performance measurement of the proposed cyclic ADC. Fig. 14(a) shows the dynamic performance versus sampling frequency at 1-MHz input frequency. The performance of the cyclic ADC starts to degrade at higher than 14 MS/s. Fig. 14(b) shows the dynamic performance versus input frequency at 14-MS/s sampling rate. The FFT spectrum with 5-MHz input frequency and at 14 MS/s is shown in Fig. 15. The SNDR and SFDR with 5-MHz input frequency are 52.44 and 65.1 dB, respectively. The effective number of bit (ENOB) is 8.42 bit. Even at a 20-MHz input frequency, the ENOB of the cyclic ADC is still 8.23 bit. This result manifests the wide-bandwidth performance of the proposed PGA.

The measured DNL and INL at 14 MS/s is shown in Fig. 16. The peak DNL and INL at 14 MS/s are within ± 0.79 LSB and ± 1.89 LSB. The dynamic performance versus input signal level is shown in Fig. 17. The peak SFDR is 64.2 dB. The dynamic range of the ADC is about 60 dB. Fig. 18 shows the histogram of digital outputs with zero input signal at 14 MS/s. The variation between the middle code (512) and the mean value of the histogram represents the dc offset of the ADC, which is 2.14 LSB. The variance of this histogram means the rms noise value, which is 0.296 LSB. With the help of inherent offset cancellation of the proposed capacitor reuse technique, the total offset of the cyclic ADC is significantly reduced.

Fig. 19 shows the schematic of an active sensor pixel. Each pixel is comprised of an image sensor and readout circuits. The image sensor includes a photodiode, a reset transistor and one single-ended opamp. In this work, the source follower is replaced with the opamp to achieve higher linearity. The readout

TABLE II
PERFORMANCE SUMMARY OF PROPOSED ADC

ADC Specification					
Resolution	10 bits				
Sampling Rate	14 MS/s				
Power Supply	3.3 V				
Input Range (diff.)	2.4 V				
SNDR @ f_{in} = 5 MHz	52.44 dB				
SFDR @ f_{in} = 5 MHz	65.1 dB				
DNL	-0.53 LSB~0.42 LSB (@8 MS/s)		-0.72 LSB~0.79 LSB (@ 14 MS/s)		
INL	-1.49 LSB~1.74 LSB (@ 8 MS/s)		-1.72 LSB~1.89 LSB (@ 14 MS/s)		
Offset	5.02 mV				
Noise (r.m.s.)	0.69 mV				
Analog Power for Cyclic ADC	5.78 mW	Analog Power for PGA	5.78 mW	Digital Power	10.06 mW
Total Power	21.62 mW				
Core Area	0.381 mm^2				

TABLE III
COMPARISON WITH PRIOR COLUMN-LEVEL 10-bit ADCs FOR CMOS IMAGE SENSORS

Reference	[13]	[14]	This work
Resolution	10 bits	10 bits	10 bits
Conversion Time	16 μs	4 μs	0.071 μs
DNL	N/A	+0.53/-0.78 LSB	+0.72/-0.79 LSB
INL	+1.4/-1.0 LSB	+1.42/-1.61 LSB	+1.73/-1.89 LSB
Power Supply	2.5 V	2.8 V	3.3 V
Power Consumption	52 mW	36 mW	15.8 mW
Technology	0.25 μm CMOS	0.35 μm CMOS	0.18 μm CMOS

circuit is implemented with passive switched-capacitor network. This circuit performs the function of correlated double sampling (CDS) to reduce the FPN and produces fully differential outputs to the backend ADC for the better noise immunity and signal-to-noise ratio (SNR). The measured results of sensors and the proposed circuit are summarized in Tables I and II, respectively. Table III shows the comparison with prior column-level 10-bit ADCs for CMOS image sensor applications. From this comparison, it reveals that the proposed cyclic ADC can achieve higher conversion rate while consuming less power.

V. CONCLUSION

A low-power PGA and a cyclic ADC are proposed for the satellite CMOS image sensing system. A low-power PGA with constant input capacitance, gain amplification and level shifter is implemented with a single opamp. The proposed capacitor reuse technique reduces the power consumption, die area and offset of the cyclic ADC. Moreover, the single power-efficient opamp is shared in multiple algorithmic cycles to reduce the power consumption of the cyclic ADC. The proposed wide-bandwidth cyclic ADC can be even applied for the subsampling applications [15].

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