A Histogram-Based Testing Method for Estimating A/D Converter Performance

Hsin-Wen Ting, *Student Member, IEEE*, Bin-Da Liu, *Fellow, IEEE*, and Soon-Jyh Chang, *Member, IEEE*

***Abstract*—A sine-wave histogram-testing structure for analog-to-digital converters (ADCs) is proposed. The ADC static parameters, i.e., offset error, gain error, and nonlinearity errors, are directly obtained from the sine-wave histogram test. Then, the obtained static parameters are related to the estimation of the degraded signal-to-noise ratio (SNR) value. Therefore, the relationships among these parameters are analyzed, and a single sine-wave histogram test can be performed to evaluate the ADC. With the appropriate approximations in the reference sine-wave histograms and the estimations of the ADC parameters, the realization of an ADC output analyzer circuit could be a simple task. An ADC output analyzer circuit is therefore developed and synthesized using a 0.18-μm technique to analyze the outputs of an 8-bit ADC and estimate its performances using the proposed method.**

***Index Terms*—Analog-to-digital converters (ADCs), degraded signal-to-noise ratio (SNR) value, gain error, nonlinearity error, offset error, sine-wave histogram test.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) have a wide application in modern electronic devices and systems. Therefore, characterizing the performance of ADCs is an important concern. The ADCs are commonly tested using a specification-oriented method to determine the parameters of interest, such as offset error, gain error, nonlinearity error, signal-to-noise ratio (SNR), and effective number of bits (ENOB). Thus, the tolerance and confidence levels of the testing method that is used to characterize the ADC must be appropriate [1], [2].

The histogram method is one of the popular techniques for ADC testing [1]–[6]. Conventionally, the histogram test reveals the offset error, gain error, and nonlinearity error, i.e., differential nonlinearity (DNL) and integral nonlinearity (INL), by comparing the measured histograms to the reference ones. Performing one test to obtain the ADC dynamic and static parameters is a promising strategy for test procedure simplification and ADC test cost reduction. Studies that relate the relationship between the test results of the histogram method and the ENOB value have been reported [7]–[10]. Therefore, one objective of this paper is to relate the commonly obtained static parameters, i.e., offset error, gain error, and nonlinearity error, to the degradation in SNR value.

To realize a complete system on a single chip, the ADCs are often integrated with other circuits. Testing these ADC circuits is a challenging task because of the limited controllability and observability. To resolve the problem, one promising strategy is to estimate the ADC performance on chip [5], [6]. In general, the straightforward realization of the on-chip histogram test method requires hardware resources of memory for storing both the experimental and the reference histograms and computing capabilities for evaluating the ADC parameters. Either a linear ramp or a sine wave can be used as an input stimulus to establish the histograms. The linear histogram technique presents a very interesting feature that concerns memory saving for storing the reference histograms. In addition, another advantage that is derived from the intrinsic property of a linear ramp input is the reduced circuitry of the ADC output analyzer circuit [5], [6]. However, the linear ramp input slowly changes, and the linear tests are consequently considered to be static tests [4]. The dynamic nonlinearities of the ADC worsen with increasing input slew rate. In applying a higher frequency signal to the ADC, the worse nonlinearities result in a larger harmonic distortion and degrade the ADC's performance. At higher frequencies, a sine wave is easier to generate than a linear signal, and a sine-wave input signal is usually used to determine the dynamic characterization [4], [11]. However, the characterization of the ADC performance with a sine-wave input is more complicated than that for the linear ramp input due to the nonuniform distribution of the code counts. Then, a large amount of additional circuitry is required to extract the nonuniform distribution. An interesting test technique for resolving this difficulty has been reported [6]. However, the assumption of a symmetric reference histogram to save on hardware costs generates a testing error. Therefore, another objective of this paper is to investigate the appropriate approximations, which are easy to implement on chip, of the original complex expressions in the ADC sine-wave histogram test. Then, an ADC output analyzer circuit is realized according to these approximations in the ADC sine-wave histogram test.

This paper is organized as follows: The basic histogram-testing background is introduced in Section II. The proposed single sine-wave histogram test that determines the ADC parameters is described in Section III, along with an analysis and discussion. The simulation and experimental results that validate the proposed testing architecture are given in Section IV. Finally, conclusions are drawn in Section V.

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II. BACKGROUND

The histogram or the output code density is the number of times every individual code has occurred [3]. The sine-wave histogram-testing technique applies an analog sine-wave signal that is slightly larger than the full scale of the ADC to ensure that all the valid codes are exercised. Then, the code count numbers of the converter output are recorded to establish the histograms.

The size of each ADC quantization level is the least significant bit (LSB). The number of hits at the upper and lower codes can be used to find the offset (V_o) and amplitude (A) of the input sine wave in LSBs, i.e.,

$$V_o = \frac{\cos\left[\pi H(0)/N_t\right] - \cos\left[\pi H(2^N-1)/N_t\right]}{\cos\left[\pi H(0)/N_t\right] + \cos\left[\pi H(2^N-1)/N_t\right]}(2^{N-1}-1) \quad (1)$$

$$A = \frac{2^{N-1} - 1 - V_o}{\cos\left[\pi H(2^N-1)/N_t\right]}. \quad (2)$$

This fitted sine wave is the input as seen through the "eyes" of the ADC device under test (DUT) [4], [11].

When the offset and amplitude of the sine-wave input are determined, the reference sine-wave distribution of code counts, which is denoted as $H_{\text{ref}}(i)$, can be obtained. The expression of the ith code count for an N-bit ADC is therefore

$$H_{\text{ref}}(i) = \frac{N_t}{\pi}\left[\sin^{-1}\left(\frac{i+1-2^{N-1}-V_o}{A}\right) - \sin^{-1}\left(\frac{i-2^{N-1}-V_o}{A}\right)\right] \quad (3)$$

where N_t is total number of samples.

The offset error should be zero for an ideal ADC. Therefore, the offset error Offset_Error of an N-bit ADC can be expressed in LSBs as

$$\text{Offset\_Error} = (2^N/V)V_o \quad (4)$$

where V is the reduced full-scale range of the ADC.

The nominal value of the slope of the ADC transfer curve G is unity, and the gain error Gain_Error of an N-bit ADC can be expressed in LSBs as

$$\text{Gain\_Error} = 2^N(G-1). \quad (5)$$

Let $H(i)$ be the number of samples presented in code i. One can therefore subtract one LSB from the ith codeword width to obtain the DNL errors in LSBs, i.e.,

$$\text{DNL}(i) = \frac{H(i)}{H_{\text{ideal}}(i)} - 1, \qquad i = 1, 2, \ldots, 2^N - 2. \quad (6)$$

Then, the DNL values can be integrated to obtain the cumulative sum and to calculate the INL errors. The corresponding INL error expression in LSB units can be described as

$$\text{INL}(i) = \sum_{k=1}^{i} \text{DNL}(k), \qquad i = 1, 2, \ldots, 2^N - 2. \quad (7)$$

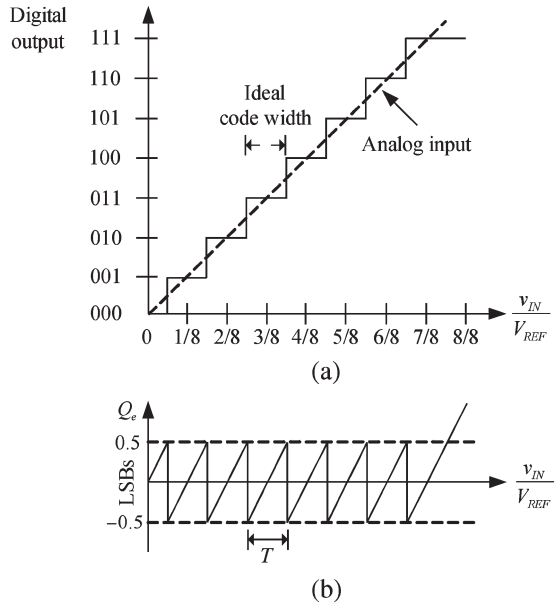

Fig. 1. (a) Transfer curve for an ideal 3-bit ADC. (b) Quantization error for an ideal 3-bit ADC.

III. ADC SINE-WAVE HISTOGRAM-TESTING STRUCTURE

This section is divided into three parts. The relationships between the estimated degradation of the SNR value and the test results, which are obtained by using the sine-wave histogram method, are analyzed. Therefore, a single sine-wave histogram test can be used to obtain the ADC static performance and an estimation of the dynamic one. Then, the considerations of employing a sine-wave histogram test method are summarized. In addition, an ADC output analyzer circuit, together with the appropriate approximations needed to determine the ADC parameters, is then developed without using extra memory to store the reference histograms.

A. Relationships Among ADC Performances

The error waveform is generated in the process of quantization. The nominal size of each quantization level is the LSB. An N-bit ADC with a full-scale analog input range of FS has a corresponding LSB step size of

$$V_{\text{LSB}} = \frac{FS}{2^N - 1}. \quad (8)$$

Ideally, the quantization error is uniformly distributed, and the root mean square (rms) value of the ideal quantization error is given by

$$v_{e,\text{rms}} = \frac{V_{\text{LSB}}}{\sqrt{12}}. \quad (9)$$

The transfer curve and the quantization error of a 3-bit ideal ADC are shown in Fig. 1, where the periodicity of the sawtooth is designated as T.

For a full-scale sine-wave input having a peak value of 2^{N-1} LSB, the best achievable SNR value $\text{SNR}_{\text{ideal}}$ at the output of the ADC is given in units of decibel as

$$\text{SNR}_{\text{ideal}} = 6.02N + 1.76. \quad (10)$$

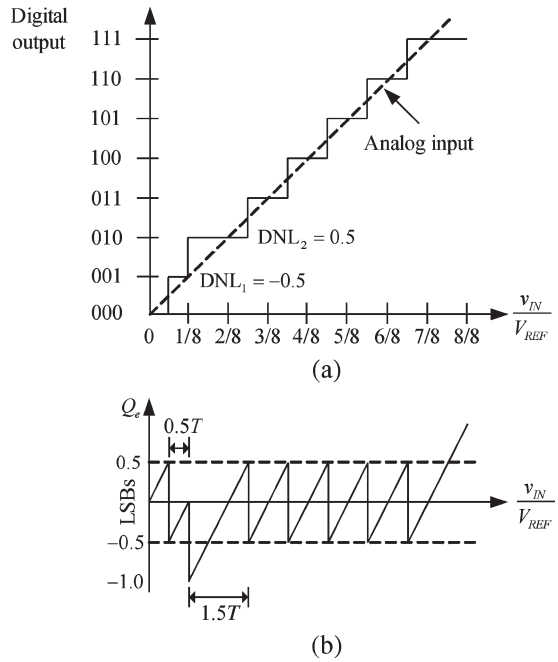

Fig. 2. Example with $\mathrm{DNL}_1 = -0.5$ LSB and $\mathrm{DNL}_2 = 0.5$ LSB for a practical 3-bit ADC.

In a practical N-bit ADC, the corresponding rms uncertainty of the quantization error is the rms amplitude of this sawtooth, and the rms value will deviate from the ideal value expressed in (9). To develop the rms quantization noise in a practical ADC, the relationships between the DNL and the rms quantization errors are discussed. The DNL errors can be obtained from (6), and the DNL will change the code widths to be longer $(\mathrm{DNL} > 0)$ or shorter $(\mathrm{DNL} < 0)$; an example is illustrated in Fig. 2. The DNL error of code 1 is -0.5 LSB because the code width is shorter than one quantization level. On the other hand, the DNL error of code 2 is 0.5 LSB because the code width is longer than one quantization level.

The general equation of a squared error for a quantization level i with a DNL error of $\mathrm{DNL}_{i,\mathrm{act}}$ and an ideal periodicity of T is described as

$$v_{e,i}^2 = \frac{1}{T(1+\mathrm{DNL}_{i,\mathrm{act}})} \int_{-0.5T(1+\mathrm{DNL}_{i,\mathrm{act}})}^{0.5T(1+\mathrm{DNL}_{i,\mathrm{act}})} \left(\frac{V_{\mathrm{LSB}}}{T}t\right)^2 dt = \frac{V_{\mathrm{LSB}}^2}{12}(1+\mathrm{DNL}_{i,\mathrm{act}})^2. \quad (11)$$

There will be an excess squared error due to the ADC nonlinearities. The absolute deviated squared error, which is different from the ideal one in (9), is considered because it represents the excess squared error with nonlinearity errors. Consequently, the absolute value is used when $\mathrm{DNL}_{i,\mathrm{act}}$ is a negative value, and the absolute deviated squared error for a code i with a DNL error of $\mathrm{DNL}_{i,\mathrm{act}}$ is expressed as

$$v_{\mathrm{de},i}^2 = \frac{V_{\mathrm{LSB}}^2}{12}\left(1 + \left|\mathrm{DNL}_{i,\mathrm{act}}^2 + 2\mathrm{DNL}_{i,\mathrm{act}}\right|\right). \quad (12)$$

The gain and offset are the parameters of a straight-line fit to the kth transition level $T[k]$ versus k. The transfer characteristic can be represented to define the gain (G) and offset (V_{os}) as

$$T[k] = \frac{(k-1) + T[1] + V_{\mathrm{os}} + \varepsilon[k]}{G} \quad (13)$$

where the transition levels are all in LSB units, and the ideal code bin width is 1 LSB.

Given these values of G and V_{os}, the term $\varepsilon[k]$ is the INL error, which represents the difference between the actual and ideal characteristics computed from G and V_{os} for code k [1], [2].

The gain is the slope of a practical ADC transfer function and can be approximated as

$$G = \frac{2^N - 2}{T[2^N - 1] - T[1]} \approx 1 - \frac{1}{2^N - 2}\sum_{i=2}^{2^N-2} \mathrm{DNL}_i. \quad (14)$$

The nominal value of G is unity, and the gain error Gain_Error of an N-bit ADC can be obtained in LSB units from (5). If the gain error is x LSB, the value of gain G should be $1 + x \cdot 2^{-N}$ from (5), which is typically close to unity.

For any particular value of the gain and offset, the actual DNL error $\mathrm{DNL}_{i,\mathrm{act}}$ is defined from (13) in units of LSB as

$$\mathrm{DNL}_{i,\mathrm{act}} = G\left(T[i+1] - T[i]\right) - 1 \quad (15)$$

when the ideal code bin width is 1 LSB. The DNL error DNL_i for code i is expressed as

$$\mathrm{DNL}_i = \left(T[i+1] - T[i]\right) - 1 \quad (16)$$

if there is no gain error $(G = 1)$ and offset error $(V_{\mathrm{os}} = 0)$. It is obvious that the offset error will be cancelled out because of the subtraction between the two transition levels in (16). Then, the deviated squared error for a code i in (12) can be expressed as

$$v_{\mathrm{de},i}^2 = \frac{V_{\mathrm{LSB}}^2}{12}\left[1 + \left|G^2\left(\mathrm{DNL}_i^2 + 2\mathrm{DNL}_i\right) + \left(G^2 - 1\right)\right|\right] \quad (17)$$

when the offset and gain are considered. The nominal value of G is unity; therefore, the term $(G^2 - 1)$ in (17) is neglected, and (17) is approximated as

$$v_{\mathrm{de},i}^2 \approx \frac{V_{\mathrm{LSB}}^2}{12}\left[1 + \left|G^2\left(\mathrm{DNL}_i^2 + 2\mathrm{DNL}_i\right)\right|\right]. \quad (18)$$

Then, the deviated rms error (rmse) v_{de} that is introduced by the nonlinearity errors, offset error, and gain error for an N-bit ADC will therefore be expressed as

$$v_{\mathrm{de}} = \frac{V_{\mathrm{LSB}}}{\sqrt{12}} \cdot \sqrt{\frac{\sum_{i=1}^{2^N-2}\left[1 + \left|G^2\left(\mathrm{DNL}_i^2 + 2\mathrm{DNL}_i\right)\right|\right]}{2^N - 2}}. \quad (19)$$

The degradation in the SNR value SNR_d concerning the deviated rmse v_{de} for an N-bit ADC is then expressed as

$$\mathrm{SNR}_d = -10 \cdot \log\frac{\sum_{i=1}^{2^N-2}\left[1 + \left|G^2\left(\mathrm{DNL}_i^2 + 2\mathrm{DNL}_i\right)\right|\right]}{(2^N - 2)} \quad (20)$$

when taking (19) into account.

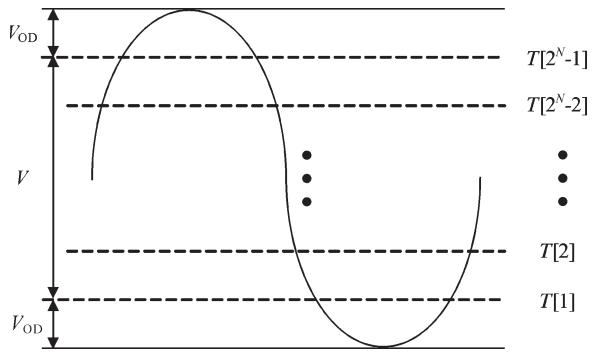

Fig. 3. Sine-wave histogram-testing parameter for an N-bit ADC.

B. Considerations of the Sine-Wave Histogram Test Parameters

The estimation of the uncertainty affecting the INL (code transition level) or DNL (code bin width) measurement is discussed. The uncertainty is classified into a random effect and a systematic one. The general concerned random effects are additive noise, jitter, and sampling uncertainty [1], [2], [13]. The systematic error mainly arises from the distortion of the input signal [1], [2], [12], [13] and the input signal probability density function (pdf) deviating from the ideal one [1], [2], [13]. It is preferable to provide an expanded combined uncertainty that includes estimation errors and to define an interval where the value of the measurement is believed to lie within a certain confidence [1], [2], [13].

Combining the random effects, the number of records R required for a given test uncertainty B in the INL and DNL is given by

$$R = D\cdot\left(\frac{2^{N-1}K_u}{B}\right)^2\cdot\left(\frac{\alpha\pi}{M}\right)\cdot\left[0.25\frac{\alpha\pi}{M}+1.13\left(\frac{\sigma}{V}+0.5\sigma_\phi\right)\right] \tag{21}$$

where $K_u = Z_{0.5u}$ is the normalized Gaussian random variable with a given confidence $1-u$.

D is equal to 1 or 2 for the INL or DNL, respectively, and M is the number of record lengths. The parameters σ_ϕ and σ are variances of the phase jitter and random noise, respectively. The reduced full-scale range V and the overdrive $V_{\rm OD}$ are illustrated in Fig. 3, and α is defined as [1], [2]

$$\alpha = 1 + (2V_{\rm OD}/V). \tag{22}$$

Therefore, the total number of samples N_t is equal to RM.

In general, the random effect can be effectively reduced by increasing the record length M with consideration of the finite resolution of the synthesizers [1], [2], [13]. The number of cycles per record J and a record length M should be selected such that J is an integer that is mutually prime to M. The coherent condition is $r \equiv f_i/f_s = J/M$, where f_i and f_s are the input and the sampling frequency, respectively. If (23) is satisfied, even if a frequency ratio error Δr is present, then the counting variance is bounded in the same way as for the perfectly coherent sampling case [13]–[16]

$$\frac{\Delta r}{r} \le \frac{1}{2JM}. \tag{23}$$

The systematic contributions of $E_{\rm INL,pdf}$ and $E_{\rm DNL,pdf}$ that result from the deviation of the input signal pdf can be neglected when a suitable overdrive region $(V_{\rm OD})$ is used [13], i.e.,

$$V_{\rm OD} \ge \left[\max\left(2\sigma_n, \frac{0.32\sigma_n^2}{E_{\rm INL,pdf}\cdot Q}\right) \text{ or } \max\left(3\sigma_n, \sigma_n\sqrt{\frac{3}{8E_{\rm DNL,pdf}}}\right)\right] \tag{24}$$

where Q is the ideal code bin width in input units.

The systematic error $\varepsilon_{\rm dist}$ is arising from the distortion of the input sine wave [12]. $\varepsilon_{\rm dist}$ has an upper bound, which is given by [13]

$$\varepsilon_{\rm dist} \le \left[E_{\rm INL,dist}\cdot Q \text{ or } \frac{\sqrt{A}(E_{\rm DNL,dist}\cdot Q)}{\sqrt{2Q}\left(\sqrt{1+V_{\rm OD}/Q}-\sqrt{V_{\rm OD}/Q}\right)}\right] \tag{25}$$

where A is the signal amplitude, $V_{\rm OD}$ is the overdrive region, Q is the ideal code bin width in input units, and $E_{\rm INL,dist}$ and $E_{\rm DNL,dist}$ are the maximum admitted errors for the DNL and INL measurements, respectively.

The systematic contributions of $E_{\rm INL,pdf}$ and $E_{\rm DNL,pdf}$ can be easily reduced by increasing the overdrive $(V_{\rm OD})$ but with negligible costs. Therefore, $E_{\rm INL,pdf}$ and $E_{\rm DNL,pdf}$ are always regarded to be small and are safely assumed not to affect the confidence of the results. The errors $E_{\rm INL,dist}$ and $E_{\rm DNL,dist}$ can be improved by instrument hardware. A source distortion smaller than -62 and -44 dBc (when $V_{\rm OD}=0$) is required to evaluate an 8-bit ADC with an admitted systematic error of 0.1 LSB in transition level (INL) and code bin width (DNL), respectively [13].

C. ADC Output Analyzer

As mentioned in Section II, the offset and amplitude of the sine-wave input have to be determined to represent the correct input signal information before the sine-wave histogram test is performed. However, the direct computation of the cosine functions in (1) and (2) requires a large silicon area cost. In addition, the calculations of the reference histogram $H_{\rm ref}$ in (3) are complex, and the required area is huge because the inverse sine functions are necessary for all codes. Therefore, the appropriate approximations in determining the input sine-wave characterization and reference histograms are necessary to realize an ADC output analyzer circuit with reduced overhead.

The hitting number at the upper and lower codes $[H(2^N-1)$ and $H(0)]$ for an N-bit ADC can be used to calculate the input signal's offset and amplitude from (1) and (2). The trigonometric function $f(x)=\cos x$ can be well approximated as $1-x^2/(2!)$ by using the Maclaurin series when the variable x

is smaller or equal to one eighth. The counting numbers of both upper and lower codes $H(\text{End\_Code})$ can be approximated by

$$H(\text{End\_Code}) = \left[H(0), H(2^N-1)\right] \approx \frac{N_t}{\pi} \cdot (2)^{\frac{2-N}{2}} \quad (26)$$

when the offset is small, and the total number of samples is N_t. Therefore, the variable $x = [\pi H(\text{End\_Code})/N_t]$ is smaller or equal to one eighth when the ADC resolution is larger or equal to 8 bits from (26). Then, the offset calculation in (1) can be simplified as

$$V_o \approx \frac{\pi^2}{N_t^2}\left[H(2^N-1)+H(0)\right]\left[H(2^N-1)-H(0)\right]2^{N-3} \quad (27)$$

when the resolution of the ADC DUT is larger or equal to 8 bits. The simplified offset expression will not involve cosine function calculations and will thus reduce the computing hardware and cost in very large scale integration (VLSI) realization. In addition, the hardware for offset calculation can be further reduced if the total number of samples N_t is a power of 2. The calculated absolute offset value will be large if the difference between the upper and lower code counts $H(2^N-1)-H(0)$ is larger.

Similarly, the amplitude calculation in (2) can be approximated from (26) as

$$A \approx \frac{2^{N-1}-1-V_o}{1-2^{1-N}} + V_{\text{OD}} \approx (2^{N-1}-1-V_o)(1+2^{1-N}) + V_{\text{OD}} \quad (28)$$

when the ADC resolution is larger or equal to 8 bits and an overdrive region of V_{OD} is selected.

The simplified amplitude expression will not involve cosine function calculations and will thus reduce the computing hardware and cost in VLSI realization. First, the estimated offset value in (27) is calculated. Then, the estimated amplitude value in (28) is given. Concerning the computing hardware, the estimations of both V_o and A are available in (27) and (28) using basic operative units.

The estimated values of the offset and amplitude in (27) and (28) (to reduce the computing hardware) will be substituted into (3) to provide the reference histogram H_{ref}. However, the operation of the inverse sine function in (3) cannot be efficiently evaluated with simple arithmetic operation units. The COordinate Rotation DIgital Computer (CORDIC) technique is an iterative computing algorithm that can efficiently evaluate many elementary functions using a unified shift-and-add approach. By varying a few simple parameters, the same CORDIC hardware is capable of iteratively evaluating the required functions. This regular unified formulation makes the CORDIC-based architecture an alternative arithmetic-computing algorithm in modern VLSI systems [17]–[19]. Concerning the computing hardware, the estimations of H_{ref} will be available using the basic operative units of the CORDIC technique without a huge amount of extra memory.

The estimated $H_{\text{ref}}(i)$ for each code i is then compared to the actual captured code-counting number $H(i)$ for the corresponding code i to calculate the DNL and INL errors from (6) and (7).

The reduced full-scale range V can be expressed as (2^N-1) LSB. The offset error Offset_Error for an N-bit ADC can be expressed in LSBs using (4) as

$$\text{Offset\_Error} \approx (1+2^{1-N})V_o. \quad (29)$$

The gain error Gain_Error for an N-bit ADC can be expressed in LSBs using (14) as

$$\text{Gain\_Error} \approx -\frac{2^N}{2^N-2}\sum_{i=2}^{2^N-2}\text{DNL}_i \quad (30)$$

because the summation of the DNL error is much smaller than 2^N-1 when N is larger or equal to 8 in most conditions.

Then, the degraded SNR value SNR_d estimated by (20) is related to

$$\text{Error} = (2^N-2)^{-1}\sum_{i=1}^{2^N-2}\left[1+\left|G^2\left(\text{DNL}_i^2+2\text{DNL}_i\right)\right|\right]. \quad (31)$$

A small look-up table is used to estimate SNR_d according to the calculated value of Error. Therefore, the realization for the logarithm function in (20) is not necessary. If an Error is calculated to be 1.25, then a degraded SNR value SNR_d will be estimated as -0.97 dB from (20) and (31). If the estimated gain error from (30) is x LSB, where x is a small real value in most conditions, then the value of gain G should be $1+x\cdot 2^{-N}$ from (5). The effect of G on Error and SNR_d is almost negligible when $0.99 \le G \le 1.01$. If the gain error of ADC DUT is small, the term G in (31) can be further ignored to reduce the hardware cost.

The schematic of the proposed ADC output analyzer is shown in Fig. 4. The testing procedure is based on the comparisons between the experimental and reference sine-wave histograms. The counting numbers of both end codes $H(2^N-1)$ and $H(0)$ were recorded to estimate the offset and amplitude values by (27) and (28). Then, the estimated offset and amplitude values are fed to the CORDIC-based $H_{\text{ref}}(i)$ calculator to calculate the correct reference histograms. The code i, which is captured and analyzed, is indicated by the first counter C_1. The corresponding experimental counting number $H(i)$ for this code i is computed by the second count C_2. Likewise, the counter C_1 also instructs the CORDIC-based $H_{\text{ref}}(i)$ calculator as to which reference histogram $H_{\text{ref}}(i)$ will be estimated. In addition, the ADC parameters are obtained in (6), (7), (15), (29)–(31) by the using basic operative units for the considered computing hardware.

IV. Simulation and Experimental Result

The estimated SNR_d value is related to the nonlinearity, which is affected by the measurement uncertainty. Consequently, the effects of the measurement uncertainty on the degraded SNR value were simulated. Depending on the level of specified DNL errors, the simulations were divided into three classes. The simulation uses an 8-bit ADC model. For example, a specified DNL error of ± 0.5 LSB in this ADC model indicates that the DNL errors are within ± 0.5 LSB with a probability of

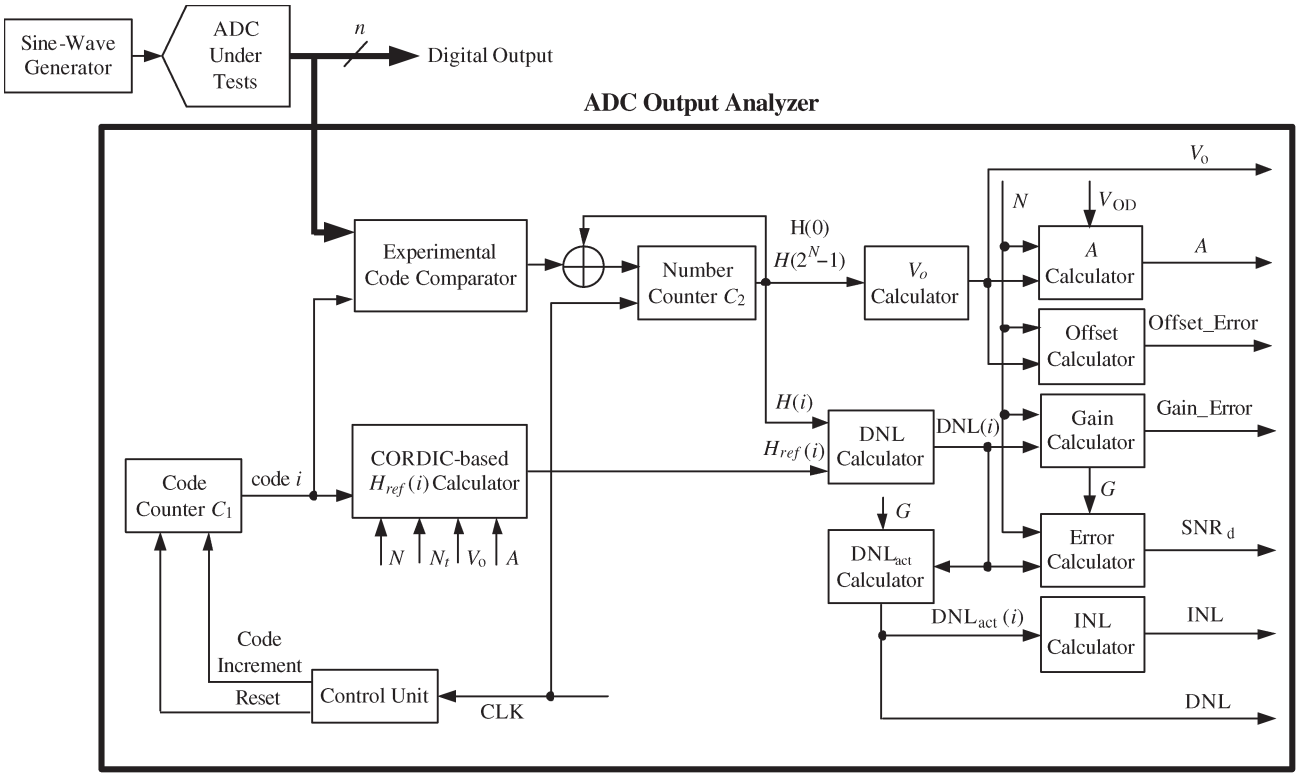

Fig. 4. Schematic of the proposed ADC output analyzer.

TABLE I
SIMULATIONS OF THE COMPARISONS BETWEEN $SNR_{d,unc}$ AND SNR_{d0} FOR AN 8-bit ADC WITH DIFFERENT DNL LEVELS

DNL (LSB)	measurement uncertainty	SNR_{d0} (dB)	$SNR_{d,unc}$ (dB)	$\lvert Difference \rvert_{max}$ (dB)
±0.25	0.1	–0.915	–0.837 ~ –1.002	0.087
±0.5	0.1	–2.352	–2.141 ~ –2.560	0.211
±1	0.1	–4.265	–3.912 ~ –4.606	0.353

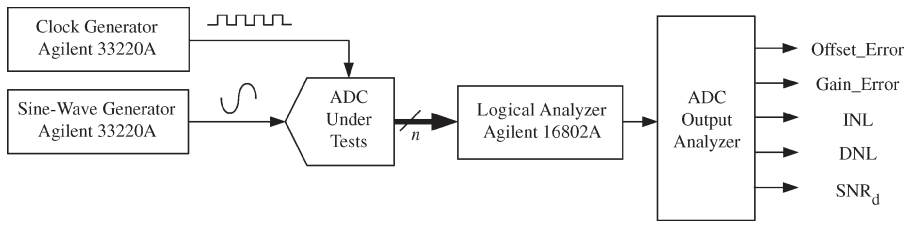

Fig. 5. Experimental setup.

99.7%. SNR_{d0} is defined as the estimated SNR_d value when there is no measurement uncertainty in the transition level (INL) and code bin width (DNL). Assume that the measurement uncertainties for the transition level and the code bin width are both 0.1 LSB. Then, the estimated SNR_d values $SNR_{d,unc}$ were compared with SNR_{d0}. From Table I, the absolute difference between $SNR_{d,unc}$ and SNR_{d0} was small in the three levels of the DNL errors when 1000 trials were used. Therefore, a measurement uncertainty of 0.1 LSB in the transition level and code bin width is applicable in estimating the degraded SNR value.

Measurements were performed to validate the proposed test architecture, which was applied to a commercial 8-bit ADC AD7822 from Analog Devices. The measured ADC output vectors were stored by a logic analyzer and then analyzed by the proposed ADC output analyzer circuit to validate the circuit performance and computation accuracy. The measurement setup for this 8-bit ADC used the Agilent 33220A to produce both the analog sine-wave input and the clock signal. In this measurement, the signal frequency was about 18.554 kHz, and the clock frequency was 2 MHz. The Agilent 16802A was used to store the ADC outputs. An illustration of the experimental setup is shown in Fig. 5. The harmonic distortion of the Agilent 33220A is -70 dBc (dc $\sim$ 20 kHz), which is suitable in the DNL and INL measurements for an admitted systematic error of 0.1 LSB, as mentioned in Section III-B. The sample numbers per record M were selected to be 2048. To guarantee a test

TABLE II
ESTIMATIONS OF THE ADC PARAMETERS AND THE SYNTHESIZED RESULTS OF THE PROPOSED ADC OUTPUT ANALYZER

Estimations of ADC parameters	
Specification	Value
Offset_Error	–0.24 LSB
Gain_Error	–0.26 LSB
DNL	±0.40 LSB
INL	±0.40 LSB
SNR_d	–1.24 dB
Synthesized results of the proposed output analyzer	
Specification	Value
Technology	0.18 μm
Clock frequency	50 MHz
Gate count	15171

uncertainty B of 0.1 and a given confidence of 0.95 in INL and DNL, the numbers of records R calculated from (21) were 8 and 15 for INL and DNL, respectively. The total number of samples $N_t = RM$ was therefore 30 720. Concerning the hardware complexity, N_t was adjusted to a power of 2, as mentioned in Section III-C. Consequently, the number of N_t was selected to be 32 768.

Then, the ADC output codes were applied to the proposed ADC output analyzer circuit. The estimated DNL, INL, and SNR_d were ±0.40 LSB, ±0.40 LSB, and −1.24 dB, respectively. The total synthesized results of the proposed output analyzer circuit are listed in Table II.

V. CONCLUSION

This paper has analyzed the relationships between the estimated degradation of the SNR value and the test results obtained by using the sine-wave histogram method. Therefore, a single sine-wave histogram test can be used to characterize an ADC. Furthermore, the considerations of the sine-wave histogram test are summarized. The random effect in estimation uncertainty can be effectively reduced by increasing the record length with consideration of the finite resolution of the synthesizers. The systematic contributions in the estimation uncertainty can be reduced by increasing the overdrive and improving the instrument hardware. In addition, an ADC output analyzer circuit for determining the ADC parameters is also introduced. This architecture involves calculation of the ADC parameters using appropriate approximations to reduce hardware complexity. An ADC output analyzer circuit is therefore developed and synthesized by using a 0.18-μm technique to validate the performance of the proposed ADC output analyzer circuit.

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