A Digitally Calibrated CMOS Transconductor With a 100-MHz Bandwidth and 75-dB SFDR

Soon-Jyh Chang, *Member, IEEE*, Ying-Zu Lin, *Student Member, IEEE*, and Yen-Ting Liu

***Abstract*—This paper proposes a high-speed CMOS transconductor with its linearity enhanced by current–voltage negative feedback. This voltage-to-current converter is mainly composed of two parts: an operational transconductance amplifier and a pair of feedback resistors. The measured spurious-free dynamic range of the transconductor achieves 72.6 dB when the input frequency is 100 MHz. To compensate for common-mode deviation due to process and temperature variation, digital calibration circuits are added. With the proposed calibration scheme, the common-mode voltage deviation is eliminated within 24 clock cycles. Fabricated in TSMC 0.13-μm CMOS process, the transconductor occupies 220×160 μm^2 active area and consumes 6 mW from a 1.2-V supply where the calibration circuits only consume 16% of the overall power consumption.**

***Index Terms*—High-linearity amplifier, operational transconductance amplifier (OTA), transconductor, voltage-to-current converter.**

I. Introduction

TRANSCONDUCTOR is a basic building block of mixed-signal circuits, which provides voltage-to-current conversion for subsequent current-mode circuits. Scaling down of supply voltage in advanced CMOS processes has made it difficult to design high-performance voltage-mode mixed-signal circuits. Without cascoded gain stage, the gain of voltage-mode amplifiers decreases. On the other hand, multistage structures increase the gain but limit the bandwidth. Current-mode circuits have many advantages over their voltage-mode counterparts, including intrinsic low-supply voltage requirement and high-speed potential [1]. Transconductors are often employed in continuous-time filters, data converters, voltage-controlled oscillators (VCOs), and other interface circuits [2].

Wide bandwidth, high linearity, and large dynamic range are the main design targets of a transconductor. Most of high-performance transconductors nowadays are designed based on a simple differential pair [3], [4]. Numerous techniques have been proposed to enhance the linearity of the differential pair. Most of them are variants of the classic source-degeneration technique [5], in which the degeneration resistor and differential pair form a local feedback network. The linear output range of this degenerated transconductor is extended, but the linearity of its transconductance is commonly limited below 60 dB. A state-of-the-art transconductor with an input frequency range up to 10 MHz and a spurious-free dynamic range (SFDR) of 80 dB is published in [6]. Based on [6], we propose an improved transconductor [7]. The proposed transconductor has a larger transconductance, roughly two times larger than that of the conventional one, and lower power consumption because the power hungry common-mode feedback (CMFB) circuit is replaced by a power-efficient digital calibration circuit.

The subsequent sections are organized as follows. Section II describes the design flow and analysis of the proposed transconductance core and digital calibration circuits. Section III discusses the nonidealities of this transconductor. The experimental results and comparison with other published state-of-the-art works are presented in Section IV. Finally, we draw a conclusion in Section V.

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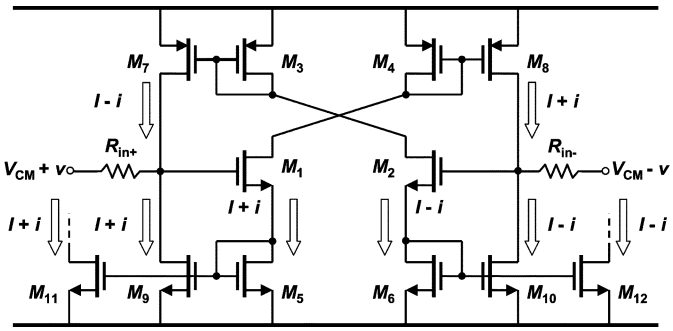

Fig. 1. Proposed transconductance core.

II. Proposed Digitally Calibrated Current–Voltage Feedback Transconductor

A. Current–Voltage Feedback Transconductance Core

The schematic of the proposed transconductance core is depicted in Fig. 1, where I stands for the dc bias current and i for ac signal current. Transistors M_{1-6} constitute a feedforward operational transconductance amplifier (OTA). Two feedback resistors, $R_{\text{in}+}$ and $R_{\text{in}-}$, are connected between the transconductor inputs and OTA inputs. When a positive voltage change is applied to the gate of M_1, a corresponding additive drain current flowing through M_1 is generated. The current also flows through M_4 and M_5. Current mirror pairs $M_4 - M_8$ and $M_5 - M_9$ replicate the currents of M_4 and M_5 to M_8 and M_9, respectively. At the same time, a negative voltage change is applied to the gate of M_2, and a corresponding subtractive current through M_2 is produced. Similarly, the subtractive current flows through M_3 and M_6, and M_7 and M_{10} get the replicated currents of M_3 and M_6, respectively. If $M_{7,8}$ and $M_{9,10}$ have the same current driving capability, the dc bias currents sink through $M_7 - M_9(M_8 - M_{10})$ path, and the ac signal currents of $M_7(M_8)$ and $M_9(M_{10})$

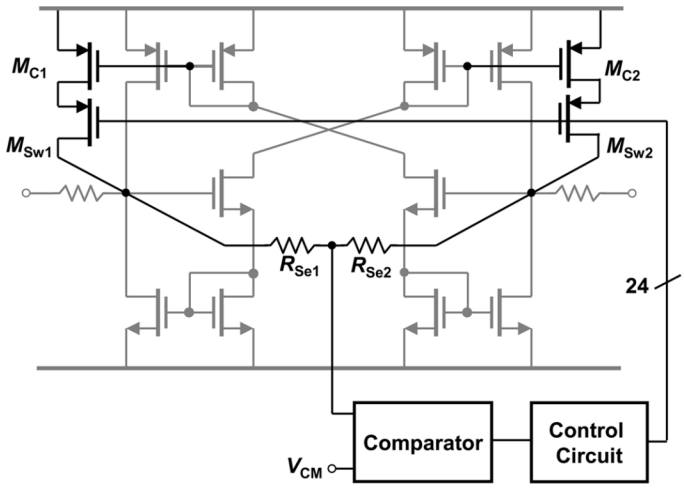

Fig. 2. Proposed digital calibration circuits.

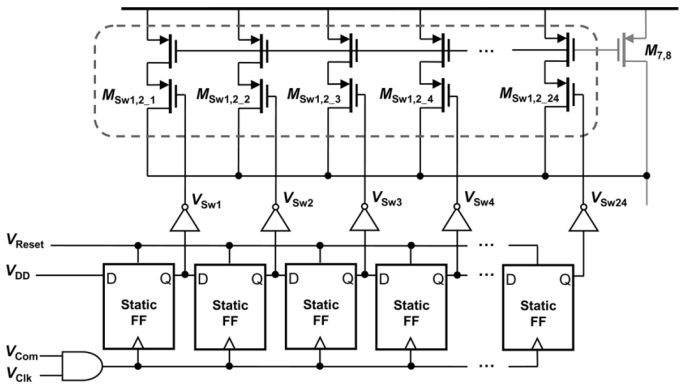

Fig. 3. Compensation transistors and control circuits.

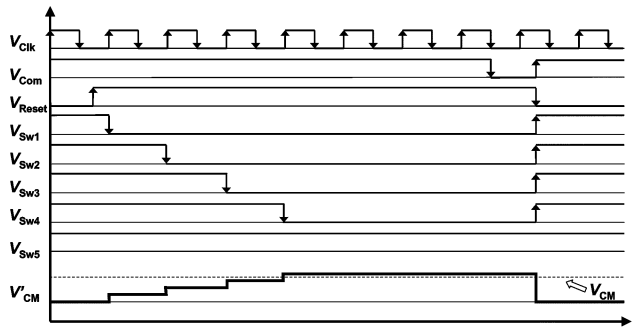

Fig. 4. Timing diagram of the calibration scheme.

flow into resistor $R_{\text{in}+}$ ($R_{\text{in}-}$) to perform voltage mixing at the OTA input. Thus far, a complete signal feedback path is formed. M_{11} and M_{12} are added to deliver output currents.

With $R_{\text{in}+}$ and $R_{\text{in}-}$, signal amplitudes are degenerated at the OTA inputs. The "gate-degeneration" resistors play the same role as the resistor in a source-degenerated differential pair. Small voltage variations at the OTA inputs make the input transistors (M_1 and M_2) operate around the predetermined bias point, and therefore the input swing is extended. Owing to the modification of the OTA structure, doubled signal currents flow into the feedback resistors. The closed-loop gain of this transconductor is described as

$$g_{\text{m\_close}} = \frac{g_{\text{m\_open}}}{1 + g_{\text{m\_open}} \cdot R} \tag{1}$$

where $g_{\text{m\_open}}$ is the transconductance of the OTA and R is the resistance of the feedback resistors. The transconductance of the OTA is derived as

$$g_{\text{m\_open}} = \left(\frac{\frac{g_{\text{m9}}}{g_{\text{m5}}} + \frac{g_{\text{m7}}}{g_{\text{m3}}}}{1 + \frac{g_{\text{m1}}}{g_{\text{m5}}}} \right). \tag{2}$$

When the loop gain is large, the transconductance approximates to $1/R$. In comparison with the conventional architecture, the transconductance of the proposed OTA is roughly two times larger. Therefore, the proposed voltage-to-current converter achieves higher linearity due to the larger loop gain.

Another advantage of this transconductor is that it is easily modified to have multiple outputs by simply adding output transistors, either n-type or p-type ones. These output transistors can be scaled for any desired ratio of output currents.

B. Calibration Circuit

Due to process variation, the current driving capability of $M_{7,8}$ and $M_{9,10}$ may be different from the expected quantity. This difference usually results in common-mode voltage deviation. In order to adjust this deviation, a CMFB circuit is often necessary. In the proposed circuit, power efficient calibration circuits are used to alleviate common-mode voltage deviation. As depicted in Fig. 2, R_{Se1} and R_{Se2} sense the OTA input common-mode voltage. The succeeding comparator compares the sensed voltage with the predetermined common-mode voltage, and the resultant output is applied to the control circuit. Each of the switches M_{Sw1} and M_{Sw2} is composed of 24 identical transistors, and similarly, the compensation transistors M_{C1} and M_{C2} consist of 24 identical transistors each, as depicted in Fig. 3. Before calibration, transistors $M_{\text{Sw1,2}}$ are off and the input common-mode voltage is designed to be lower than the reference voltage. When the comparator output is high, these static flip-flops are activated. The switches turn on successively until the comparator changes its output polarity. After calibration, the common-mode voltage is slightly higher than the desired value. The difference between the calibrated input common-mode voltage and the reference voltage depends on the transistor number and size of $M_{\text{C1,2}}$. In this design, the step is less than 10 mV. Fig. 4 shows the timing diagram of a simplified example where V'_{CM} is the actual input common-mode voltage of the transconductor. The simulated OTA input common-mode voltages with and without calibration are shown in Fig. 5(a) and (b), respectively. The two figures show the typical (TT), fast-NMOS and slow-PMOS (FS), and slow-NMOS and fast-PMOS (SF) cases since FS and SF are the extreme cases where maximal difference of mobility between PMOS and NMOS transistors occurs. For clarity, Fig. 5 does not exhibit the fast-NMOS and fast-PMOS (FF) and slow-NMOS and slow-PMOS (SS) cases. Fig. 5(b) shows calibration procedures of the common-mode voltage in different process corners. Even in the most critical condition, FS, the input common-mode voltage can be correctly adjusted. When the transconductor is in normal operation mode, the comparator is turned off to reduce power consumption. These static flip-flops hold the calibration data until they are reset.

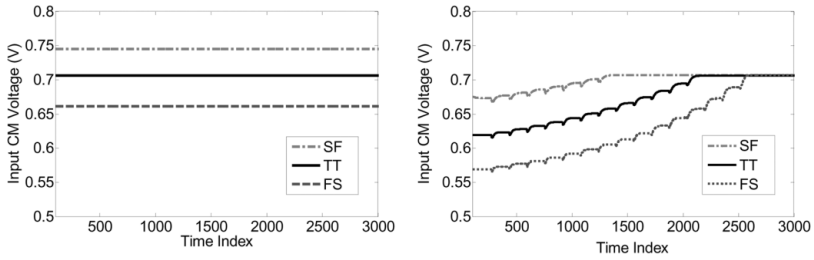

Fig. 5. (a) The input common-mode voltage without calibration. (b) The input common-mode voltage with calibration.

III. Nonidealities Analysis

A. Distortion

Because a MOS transistor is not a linear element, distortion occurs in voltage-to-current conversion. Hence, the linearity of this transconductor is limited by the distortion of the input transistors since other transistors only bypass or perform current-to-current amplifying. Considering velocity saturation effect in advanced CMOS processes, the current equation of a MOS transistor is [8]

$$I = \beta_1 \frac{(V_{\rm GS} - V_{\rm TH})^2}{1 + P_{\rm sat}(V_{\rm GS} - V_{\rm TH})}$$
$$\text{where } \beta_1 = \frac{1}{2}\mu_0 C_{\rm ox}\frac{W}{L} \text{ and } P_{\rm sat} = \frac{\mu_0}{2\upsilon_{\rm sat}L} + \theta. \quad (3)$$

In (3), $\upsilon_{\rm sat}$ is the saturation carrier drift velocity and θ is a fitting parameter to model the effect of the transversal electric field. A fully differential circuit exhibits no even order harmonic distortions. Therefore, low order odd harmonics dominate, and we can get a quantitative result as follows:

$$\frac{A_{\rm HD3}}{A_{\rm F}} \simeq \frac{1}{4}\frac{\alpha_3}{\alpha_1}\left(\frac{1}{1+\beta\alpha_1}\right)^3 V_{\rm m}^2$$
$$\text{where } \alpha_1 = \frac{\beta_1 P_{\rm sat} V_{\rm OV}(2 + P_{\rm sat}V_{\rm OV})}{(P_{\rm sat} + \beta_1 R_5)(1 + P_{\rm sat}V_{\rm OV})^2},$$
$$\alpha_3 = \frac{\beta_1 P_{\rm sat}^2}{(P_{\rm sat} + \beta_1 R_5)(1 + P_{\rm sat}V_{\rm OV})^4}$$
$$\text{and } V_{\rm OV} = V_{\rm CM} - V_{\rm TH1}. \quad (4)$$

β is the feedback factor, $V_{\rm CM}$ is the input common-mode voltage of the transconductor, $V_{\rm TH1}$ is the threshold voltage of M_1, and R_5 is the resistance of M_5 which can be simplified as $1/g_{\rm m5}$. Equation (4) shows the amplitude ratio of the third-order harmonic $(A_{\rm HD3})$ to the fundamental tone $(A_{\rm F})$ of this transconductor. In general, if a large input signal swing is desired, we have to deal with a critical third-order harmonic tone. Nevertheless, due to negative feedback, the voltage variation at the OTA inputs is very small and odd-order harmonics are greatly suppressed in the proposed design. Experimental results show the transconductor still maintains sufficient linearity when the input swing is two times larger than the supply voltage.

B. Mismatch

Mismatches between any pair of the transistors and/or input resistors result in even-order harmonics. When the mismatch between any pair of the devices is up to 0.1%, the second-order harmonic becomes very critical since it is larger than the third-order one. To overcome the nonideality, emphasis is put on the floorplan and circuit layout. The devices are carefully laid out using the common-centroid geometry technique. Guard rings and deep N-wells prevent substrate noise coupling. Furthermore, the use of minimum length transistors is avoided. Large devices are employed in this circuit to alleviate performance degradation owing to component mismatches and flicker noises. In order to obtain better linearity, poly-silicon resistors are used.

C. Thermal Noise

Thermal noise is an intrinsic performance limit of mixed-signal circuits. If circuits cannot tell signals from noises, they fail to function. Since the circuit is symmetrical, we only analyze the noise effects of a half-circuit for simplicity. Then, the scalar 2 is added in front of (6) to present the thermal noise effects of the whole circuit. In the proposed transconductor, if the feedback resistor $(R_{\rm in+})$ is removed, the gain of the half-circuit can be expressed as

$$A_{\rm V} = g_{\rm m\_open} r_{\rm out} = \left(\frac{\frac{g_{\rm m9}}{g_{\rm m5}} + \frac{g_{\rm m7}}{g_{\rm m3}}}{1 + \frac{g_{\rm m1}}{g_{\rm m5}}}\right) g_{\rm m1}(r_{\rm o7} // r_{\rm o9}). \quad (5)$$

We derive the input-referred thermal noise power of the transconductor as (6), shown at the bottom of the page, where $\gamma_{\rm n}$ and $\gamma_{\rm p}$ are the thermal noise coefficients of the NMOS and

$$\overline{V_{\rm n,in}^2} = 2\left[4kT\left(R + \frac{\gamma_{\rm n}}{g_{\rm m1}}\right) + \frac{1}{A_{\rm V}^2}\left(\overline{V_{\rm n,out}^2}\Big|_{\rm M_3} + \overline{V_{\rm n,out}^2}\Big|_{\rm M_5} + \overline{V_{\rm n,out}^2}\Big|_{\rm M_7} + \overline{V_{\rm n,out}^2}\Big|_{\rm M_9}\right)\right]$$
$$= 2 \times 4kT\left[R + \gamma_{\rm n}\frac{1}{g_{\rm m1}} + \frac{1}{g_{\rm m\_open}^2}\left(\gamma_{\rm p}\frac{g_{\rm m7}^2}{g_{\rm m3}} + \gamma_{\rm n}\frac{g_{\rm m9}^2}{g_{\rm m5}} + \gamma_{\rm p}g_{\rm m7} + \gamma_{\rm n}g_{\rm m9}\right)\right] \quad (6)$$

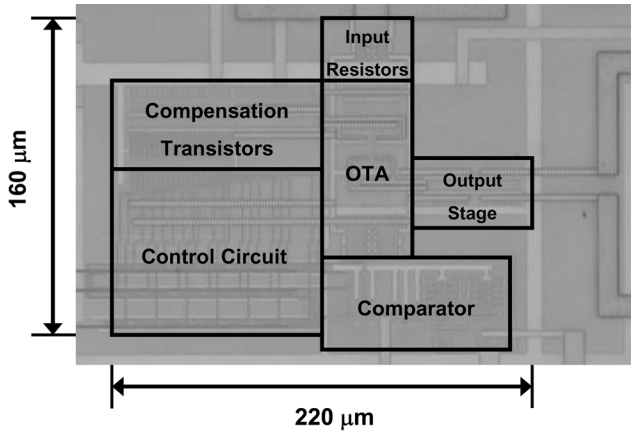

Fig. 6. Chip photograph.

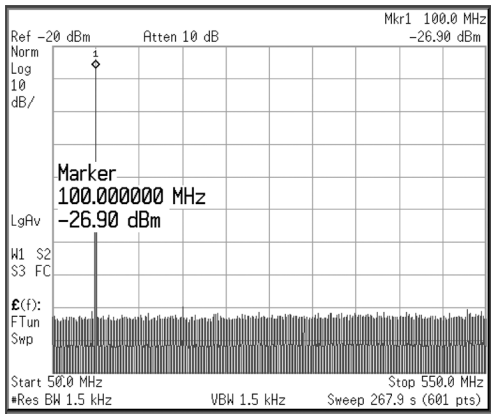

Fig. 8. Measured output spectrum when fin $= 100$ MHz.

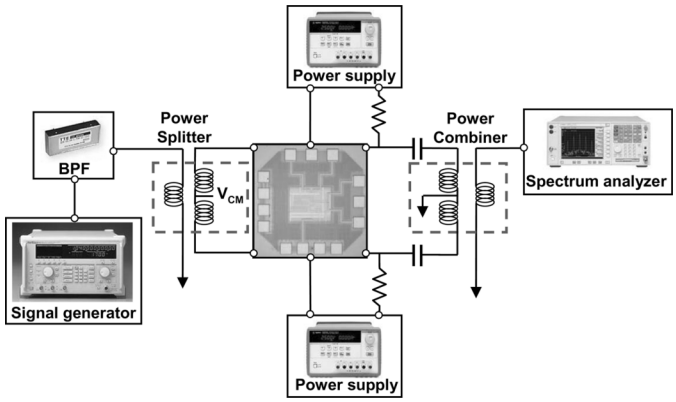

Fig. 7. Measurement setup.

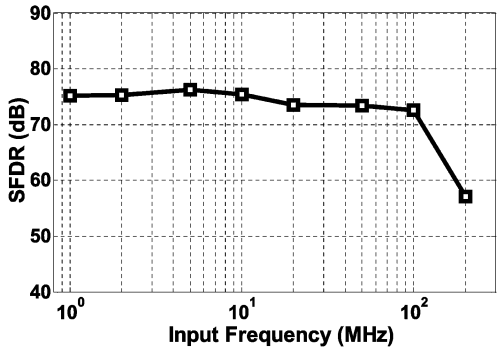

Fig. 9. Measured SFDR versus input frequency.

TABLE I
COMPARISON WITH STATE-OF-THE-ART TRANSCONDUCTORS

	SFDR (dB / MHz)	THD (dB / MHz)	Process (μm)	Supply (V)	Input Swing (V)	Power (mW)	FOM (10^{-18} J/V)
Kachare [9]	N/A	−54 @ 0.1	0.5 CMOS	2	0.3	0.96	19109
Ouzounov [10]	75 @ 10	< −70 @ 10	0.18 CMOS	1.8	0.4	0.36	2
Lopez- Martin [11]	68 @ 0.1	−66.5 @ 0.1	0.5 CMOS	±1.3	3	1.70	1464
Chilakapati [6]	80 @ 10 65 @ 20	−77 @ 10 −61 @ 20	0.35 CMOS	3.3	3.6	10.56 (52.80)	6.38 (31.9)
This work	72.6 @ 100 57.5 @ 200	−71.8 @ 100 −56.4 @ 200	0.13 CMOS	1.2	4	5.04 (6.00)	2.77 (3.3)

PMOS transistors, respectively. To suppress the thermal noises, we can increase the transconductance of $M_{1,2}$ or decrease the resistance of the feedback resistors. However, decreasing the feedback resistance reduces the loop gain.

There is a tradeoff between the output signal amplitude and linearity. If high input resistance is selected, the performance may be degraded by noises due to the small output amplitude. On the other hand, if relatively low resistance is used, the harmonics dominate the output signal linearity.

IV. MEASUREMENT RESULTS

The proposed transconductor is fabricated in TSMC 0.13-μ m CMOS 1P8M process. For higher transistor mobility, low threshold-voltage devices are used. The transconductor occupies 220 μ m$\times$ 160 μm active die area, and its photograph is shown in Fig. 6. Fig. 7 shows the measurement setup. The differential peak-to-peak input range is larger than 4 V and the input common-mode voltage is 0.7 V. For fair comparison, the output amplitude is designed close to that of the conventional work [6]. The combination of Anritsu MG3642A synthesized signal generator and TTE KC7T bandpass filters provides signals with SFDRs around 90 dB. Two 250-Ω resistors are added externally to convert output current into voltage. Fig. 8 shows the measured output spectrum when the input frequency is 100 MHz. The measured SFDR is 72.6 dB, and the total harmonic distortion (THD) is -71.8 dB. Experimental results show the linearity is dominant by the 2nd-order harmonic which is mainly caused by the mismatch between the two external resistors. The power levels of the odd harmonics are very close to the noise floor. Fig. 9 depicts the measured SFDR versus input frequency where the peak SFDR value is around 75 dB and the -3-dB bandwidth is 100 MHz. The comparison among the proposed transconductor and other state-of-the-art works is summarized in Table I. An FOM equation is used to evaluate the overall performance of a transconductor. The FOM is defined as

$$\mathrm{FOM} = \frac{\mathrm{Power}}{10^{|\mathrm{THD}|/10} \times f_{\mathrm{BW}} \times V_{\mathrm{DD}}} \tag{7}$$

where f_{BW} is the bandwidth and V_{DD} is the supply voltage. The proposed work achieves the widest input bandwidth from the lowest supply voltage. The improvement of performance mainly comes from an advanced process, large transconductance of the OTA, and little loading induced by the calibration circuits. Besides the input bandwidth, another advantage of the proposed work and [6] over the other works is the large input swing. When

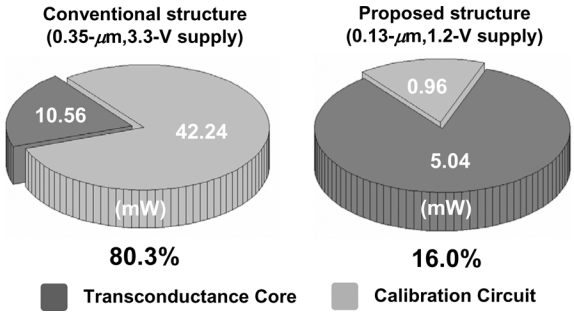

Fig. 10. Comparison of power consumption to the conventional work.

the other works increase input swings, their input transistors experience large transition and may deviate from the desired operation regions. Nonetheless, the proposed transconductor does not suffer from this problem. Fig. 10 shows the comparison of power consumption of the proposed transconductor to the conventional one [6]. Compared with the CMFB circuit in the conventional work, the calibration circuits in the proposed work only take a small part of the overall power consumption.

V. Conclusion

A transconductor for high-speed operation with an SFDR of around 75 dB is presented. An OTA and a pair of resistors connected in negative feedback constitute this voltage-to-current converter. Owing to the large loop gain, nonlinear effects are greatly suppressed, and voltage amplitudes in the signal paths are quite small. As a result, the linearity and speed of the transconductor are both augmented. Moreover, compared to the conventional CMFB solution, digital calibration circuits greatly reduce the power overhead for common-mode voltage adjustment. A transconductor is an important building block of $G_{\rm m} - C$ filters. Generally, the accuracy of $G_{\rm m} - C$ filters is worse than that of the switched capacitor (SC) type ones. Nonetheless, since the proposed transconductor is suitable for high accuracy applications, this transconductor improves the disadvantage of $G_{\rm m} - C$ filters.

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