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Low-Power Circuit Techniques for Low-Voltage Pipelined ADCs Based on Switched-Opamp Architecture

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SUMMARY This paper proposes useful circuit structures for achieving a low-voltage/low-power pipelined ADC based on switched-opamp architecture. First, a novel unity-feedback-factor sample-and-hold which manipulates the features of switched-opamp technique is presented. Second, opamp-sharing is merged into switched-opamp structure with a proposed dual-output opamp configuration. A 0.8-V, 9-bit, 10-Msample/s pipelined ADC is designed to verify the proposed circuit. Simulation results using a 0.18-μm CMOS 1P6M process demonstrate the figure-of-merit of this pipelined ADC is only 0.71 pJ/step.

key words: *low-voltage, switched-opamp, sample-and-hold, opamp-sharing, pipelined ADC*

1. Introduction

Serving as a crucial component in many communication-related products, analog-to-digital converters (ADCs) with high performance while dissipating low power are highly preferred. Pipelined ADC proves to be a popular architecture since it employs concurrent operation to achieve high throughput in a power-efficient manner. However, as process technology scales, the design of pipelined ADC becomes much more complicated when low-voltage is also a significant concern. Lower supply voltage inherently translates into lower power in digital domain while this is not the case considering analog circuit [1], [2]. In order to maintain the required dynamic range and speed performance with reduced voltage supply, extra power is needed to suppress the noise floor as well as boosting the opamp bandwidth. As a result, for a given signal-to-noise ratio (SNR) specification, the total power consumption will inversely increase with reduced supply. Insufficient switch overdrive voltage is another critical problem for low-voltage circuit which may lead to higher distortion and longer settling. Limited opamp structure choices which often fail to provide enough gain and bandwidth even deteriorate the situation.

Many approaches have been proposed to deal with insufficient switch conduction at low voltage [2]–[4]. Switched-opamp (SO) architecture removes the critical switch and replaces it with a switchable opamp [3]. It is fully compatible with deep-submicron technology and allows for extensive applications with low supply voltage such as switched-capacitor (SC) filters [5], [6], sigma-delta modulator [7], and pipelined ADCs [8]–[13].

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For a switched-opamp based pipelined ADC, since lower supply voltage does not promise lower power, the power minimization issue can be tackled from two aspects by examining the power distribution phenomenon. In the architectural level, sample-and-hold (S/H) is the dominant power contributor since it processes the full resolution and bandwidth of an ADC [14]. In the circuit level, opamps generally consume more than 80% of an overall ADC power and therefore opamp-sharing are widely used in pipelined ADCs [15]–[18]. This work proposes power saving design techniques for switched-opamp based ADCs following these two guidelines. A novel S/H architecture is introduced to relax the power and noise contribution of traditional SO-based S/H [9], [13]. Furthermore, a power-efficient ADC architecture by incorporating the opamp-sharing technique into switched-opamp configuration is presented [10]. A 0.8-V 9-bit 10-MS/s ADC is designed to demonstrate the proposed ideas.

This paper is organized as follows: Sect. 2 presents the architecture of the proposed ADC. A novel S/H as well as the SO-based opamp-sharing architecture which altogether constitute the low-voltage/low-power pipelined ADC are described and clarified. Low-voltage building blocks such as opamp and comparator are discussed in Sect. 3. Simulation results of the developed ADC using 0.18-μm CMOS 1P6M device models are demonstrated and analyzed in Sect. 4.

2. Design Issues of Proposed Pipelined ADC

2.1 ADC Architecture

Figure 1 shows the architecture of the overall pipelined ADC based on switched-opamp technique. It consists of a dedicated sample-and-hold, seven 1.5-bit/stage pipelined

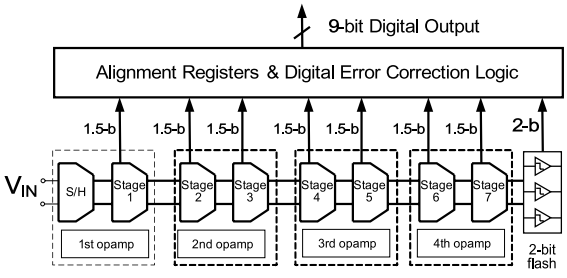

Fig. 1 ADC architecture with opamp-sharing allocation.

stages [19] and a final 2-bit flash ADC. A total of 16 bits are collected and processed by the digital error correction unit to remove the redundancy and retrieve the effective 9-bit digital output. The front-end S/H is realized with a novel SO-based technique which allows itself to operate in unity-feedback configuration. In addition, opamp-sharing is applied along the pipeline stages. Total four opamps are used, in which S/H and first multiplying-digital-to-analog-converter (MDAC) share a common opamp and then the following six MDACs share the other three opamps. The opamp sharing allocation is illustrated as the dashed blocks in Fig. 1. The proposed S/H and opamp-sharing scheme are described in detail in the following sub-sections.

2.2 Proposed SO-Based Sample-and-Hold

Figure 2(a) shows the conventional flip-around architecture of a sample-and-hold circuit which is widely used in pipelined ADCs [2]. High speed performance and power efficiency can be achieved since its feedback factor is ideally equal to 1. Besides, there is no capacitor mismatch issue because one single capacitor plays both roles of sampling and feedback capacitor. However, such type of S/H cannot be used in low-voltage circuits owing to the critical switch connected to output nodes. If the S/H in Fig. 2(a) is operated with insufficient supply, S_1 and S_2 can only be poorly conducted during their respective on-phase because they are connected to either input or output nodes whose DC levels are set around $V_{DD}/2$. Therefore, flip-around S/H cannot be directly applied in low-voltage application. Several published work concerning low-voltage sampling circuits have been proposed [8], [9], [20]. Figure 2(b) depicts a common implementation of charge-redistribution type S/H which is adaptive to SO structure [9], [13]. During ϕ_1, the opamp is turned off and C_S samples the input while C_F is reset. During ϕ_2, the opamp is activated and the differential input charge is transferred from C_S to C_F to produce the corresponding V_{OUT}. In this architecture, two bootstrapped switches [2] are used to interface the input signal for high linearity. All other switches are connected to either V_{DD} or ground and hence no critical switches exist. A major drawback of this SO-based S/H is the reduced feedback factor compared to the traditional flip-around architecture. A reduced feedback factor β directly degrades the speed and noise performance since the closed-loop bandwidth ω_u and output-referred noise $\overline{v_o^2}$ can be approximated by [14]

$$\omega_u = \beta \frac{g_m}{C_L} \tag{1}$$

$$\overline{v_o^2} = \frac{kT}{\beta C_F} \tag{2}$$

where g_m and C_L represent the opamp's input transconductance and output loading respectively, and kT is the thermal energy.

We propose a novel SO-based sample-and-hold to solve this issue. The concept is based on the features of the switched-opamp architecture in two aspects: (a) the bottom plate of feedback capacitor is forced to permanently connect to the output nodes of opamp. (b) The opamp is turned-off in one of the two non-overlapped phases, during which the output stage can be pulled to V_{DD} or ground using additional switch. Thus the sampling behavior can be realized by directly attaching the sampling capacitors onto the output nodes of the opamp rather than connecting them to ground using additional switches. The proposed fully-differential S/H architecture is shown in Fig. 3. C_{S1} and C_{S2} sample the input signal respect to V_{DD} at ϕ_1 since the opamp is currently turned-off and the output nodes are pulled to V_{DD}. During ϕ_2, the input signal path is terminated by turning off the bootstrapped switches, while the top plates of C_{S1} and C_{S2} are connected to the opamp input terminals, resulting in unity feedback and $V_{OUT} = V_{IN}$. Such configuration exploits the features of switched-opamp architecture and turns the drawbacks into benefits. It has the following advantages: The settling speed is potentially doubled compared to the S/H in Fig. 2(b) since the feedback factor is now ideally equal to 1 rather than 1/2. The improvement in feedback factor also implies the output-referred noise of the S/H is reduced by half according to Eq. (2). In a pipelined ADC, S/H usually dominates the overall noise performance

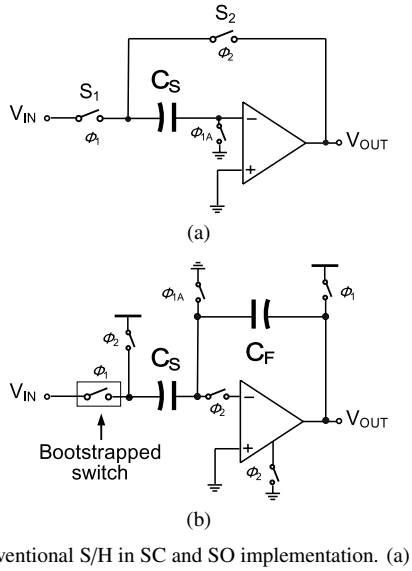

Fig. 2 Conventional S/H in SC and SO implementation. (a) Flip-around architecture [2], (b) SO based S/H [9], [13].

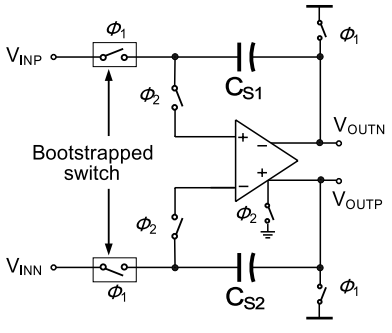

Fig. 3 Proposed switched-opamp based S/H with unity feedback factor.

because it locates at the front-end while the following stages attenuate their resulting noise through the interstage gain accumulated along the pipeline [14]. Reduced noise also indicates smaller loading capacitance and hence higher speed and lower power consumption can be achieved. Furthermore, slew-rate requirements are also relaxed because the opamp has to charge only the output node but not the feedback capacitor.

Charge injection and clock feedthrough errors in S/H circuits can be treated as DC offset by turning off the switch connected to ground with an advanced clock phase shown in Fig. 2. In the proposed scheme, advanced clock phase is not required because the bootstrapped switch always ensures a constant overdrive voltage. The channel charge stored in bootstrapped switch is independent of the input signal, and the resulting injection during turn-off can be viewed as DC offset which can be eliminated by fully-differential structure. The threshold voltage variation due to body effect which contributes to high-order distortion can be alleviated by properly minimizing the bootstrapped switch size as long as the settling requirement is satisfied. Simulation results demonstrate that the proposed S/H achieves more than 10 bit linearity at 10 MS/s, consuming only 0.3 mW at 0.8 V supply.

2.3 Merging of Opamp-Sharing and Switched Opamp Techniques [10]

Opamp-sharing technique is based on the principle that opamps operate only in the residue amplification phase but idle in sampling phase. However, two architectural limitations prevent opamp-sharing technique from straightforward application into switched-opamp configuration. First, opamp-sharing demands the opamp to be used in both clock phases for sharing while switched-opamp turns off the opamp in one of the two phases in order to mimic the behavior of a switch. Second, capacitors which are connected to the output nodes of the opamp in switched-opamp implementation are not detachable. Therefore, the opamp shared by one pipelined stage cannot be directly reused by the other without circuit modification. We have proposed a solution to solve this problem [10]. By adding one more output stage to the conventional two-stage opamp, switched-opamp configuration can be merged with opamp-sharing technique. The input stage is kept active in both phases for opamp-sharing while the dual output stages switch on/off in turn. When output stage 1 is turned-off, it provides the high impedance required for SO structure. At this moment, output stage 2 is turned on and used for opamp-sharing together with the input stage. Output stages 1 and 2 exchange their roles in the opposite clock phase and always operate complementarily.

In this pipelined ADC, two types of opamp-shared stages are used as shown in Fig. 1. The first is a dedicated S/H with its opamp shared with the first MDAC. The other is opamp-shared stages between adjacent MDACs. Figure 4 shows the detailed circuit illustrating the opamp-sharing architecture between S/H and MDAC1. The following MDACs reuse opamps in a similar manner. As shown in Fig. 4, bootstrapped switches are used to interface the system input for minimizing the distortion and reducing the switch resistance. The opamp composes of two output stages in order to be shared with the following MDAC. During ϕ_1, the system input directly charges the sampling capacitors C_{SH1} and C_{SH2} respect to the output nodes of V_{O2} since V_{O2} is turned-off and can be pulled up to V_{DD}. The opamp's input stage V_I as well as the first output stage V_{O1} is currently used by MDAC1 to produce the residue for MDAC2. Next, in ϕ_2, the top plates of the sampling capacitors are connected to opamp's inputs, and the sampled input now appears on V_{O2} for MDAC1 to sample. The right part of

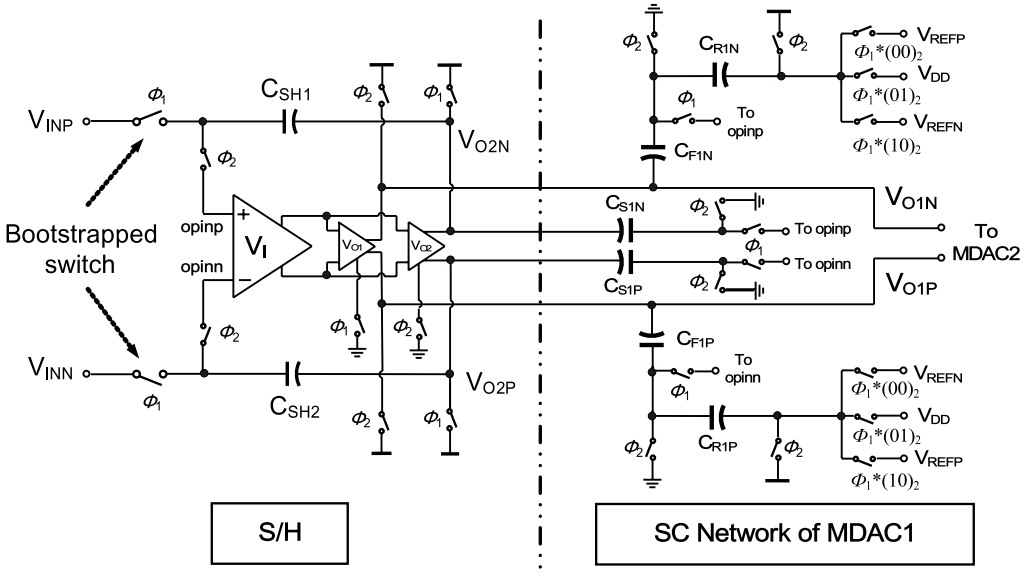

Fig. 4 Opamp-sharing between S/H and MDAC1.

Table 1 Power comparison for a 9-bit SO-based pipelined ADC w/ and w/o opamp-sharing.

	9-bit Pipelined ADC in SO structure	
# of Circuit blocks	Without Opamp-Sharing	Opamp-Sharing with Dual-Output Opamp
Opamp	8	4
I/P Stage	8	4
O/P Stage	8	4
CMFB Amp.	8	4
Estimated Power	100%	75%

the dashed line in Fig. 4 shows the SC network of MDAC1 [8]. C_S, C_F, and C_R denote the sampling capacitor, feedback capacitor and reference capacitor respectively. Capacitor values are arranged as $C_S = 2C_F = 2C_R$. C_S is chosen as two times the value of C_F in order to provide an interstage gain of two. Since for switched-opamp configuration, the capacitors connected to the opamp output are no longer switchable, the commonly used flip-around MDAC [2] cannot be applied and the maximum achievable feedback factor is only 1/4, which is only half of traditional circuit. Normally an opamp is difficult to optimize when it is shared between a S/H and a MDAC because the closed-loop bandwidth in two phases are unequal. The proposed S/H which has unity feedback factor even complicates this power and speed tradeoff compared to original SO-based S/H with β = 1/2. However, in the proposed design, the dual output stages of a shared-opamp can provide a degree of freedom to be independently optimized for S/H and MDAC to solve this issue.

2.4 Power Analysis

In the proposed SO-based opamp-sharing technique, an opamp with dual output stages is required. The addition of one more output stage seems to increase the power consumption. However since the dual output stages turns on/off alternatively in one of the two nonoverlapped clock phases, the proposed opamp consumes only equal power as a normal opamp operated at both phases. Furthermore, from a systematic perspective, the proposed dual-output opamp is shared between adjacent pipelined stages; therefore approximately half of the power is saved. Table 1 provides a detailed comparison for a switched-opamp based pipelined ADC with/without using the proposed opamp-sharing architecture. For a 1.5-b/stage, 9-bit pipelined ADC with a dedicated S/H, total 8 opamps are required without opamp sharing. The power of common-mode feedback (CMFB) amplifier is also taken into consideration since it is necessary to provide common-mode signal inversion for low-voltage opamp [8], [13]. The current consumptions of input stage, output stage, and CMFB amplifier are assumed to be 1:2:1, respectively. Bias circuit is neglected for simplicity. As shown in Table 1, 25% power is saved by using the proposed architecture. In combination with the proposed S/H, more power can be saved.

3. Circuit Design

3.1 Opamp Design

A nonideal opamp deteriorates the overall pipelined ADC linearity in mainly two ways: (1) linear but finite opamp gain and (2) nonlinear gain due to limited output swing. The latter may contribute more error due to reduced available swing in low-voltage applications. In the proposed design, sufficient gain is required to suppress the opamp-induced nonlinearity as well as the memory effect due to opamp-sharing [17].

Figure 5(a) shows the fully differential switched opamp with dual output stages adopted in this pipelined ADC [6]. As aforementioned, the merging of switched-opamp and opamp-sharing demand an opamp with dual output stages. Therefore a conventional Miller-compensated two-stage structure with dual switchable common-source output stages is used. Only one of the two output stages is turned on in each clock phase while the input stage is kept active in both phases so as to minimize the wake-up time. With input common-mode set to ground, a folded input stage with PMOS input pair is employed. The output stages apply simple common-source structure for rail-to-rail output swing. Zero-nulling resistors are used for compensation rather than MOS in order to prevent distortion caused by great impedance variation at low voltage. The output stages as well as their corresponding RC compensation networks can be separately optimized to meet the speed/power constraint set by different pipelined stages. The dynamic SC CMFB circuit as shown in Fig. 5(b) is used to provide proper output common-mode level control. Two sets of SC branches are required for dual output stages in both phases. The amplifier A_1 is used to provide the correct polarity for CMFB control signal, and the circuit is simply the same as the input stage of the main opamp.

In this paper, a 0.8-V, 9-bit, 10-MS/s pipelined ADC was designed to verify the proposed low-voltage power-saving circuit techniques. The gain and bandwidth requirements of the opamps in S/H and first MDAC are of significant concern. Normally for an N-bit ADC, an opamp gain of 2^{N+1} is required to assure finite gain induced error within $\pm 1/2$ LSB. Considering the fundamental nonideal effects such as process, temperature and supply variations, the minimum gain should be increased accordingly. In addition, in low voltage design, opamp experiences severe gain drift due to limited output range. Therefore an extra gain is further demanded. As for the bandwidth requirement, opamp must settle within $\pm 1/2$ LSB in half of the sampling period. The relationship between the unity gain frequency of opamp and the ADC resolution can be expressed as follows [14]:

$$\beta \cdot f_T > \frac{N \cdot \ln 2}{\pi} \cdot f_S \tag{3}$$

where β is the feedback factor, f_T denotes the unity gain frequency and f_S the sampling rate. For a 9-bit ADC, and when

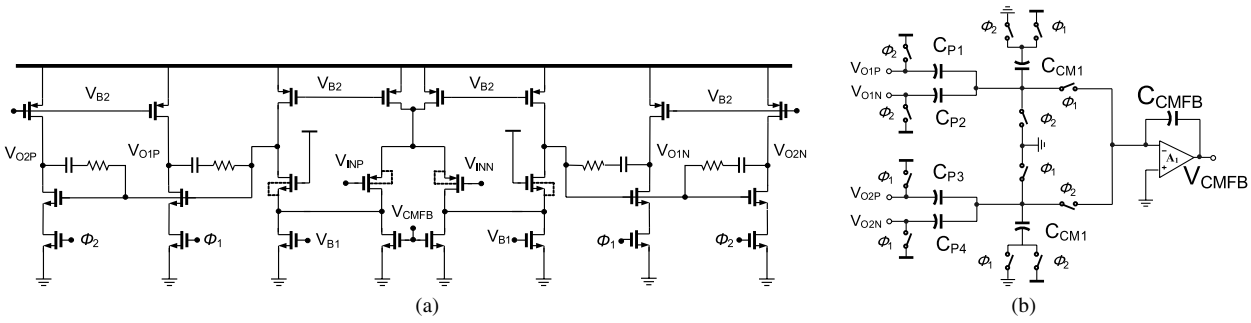

Fig. 5 Switched-opamp for opamp-sharing. (a) Opamp with dual output stages and, (b) Dynamic CMFB circuit.

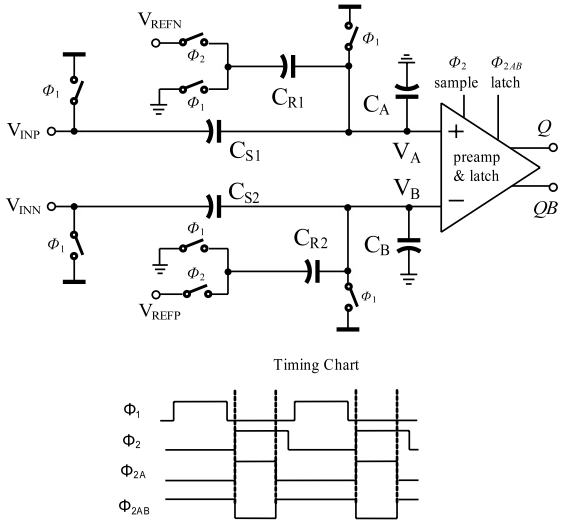

Fig. 6 Low voltage SC comparator.

the opamp in the 1st MDAC is operated at 10 MS/s sampling rate with $\beta = 1/4$, an unity gain frequency of 80 MHz is required. Simulation results show that the designed opamp for the first MDAC achieves 76-dB gain with 73° phase margin, and the unity-gain frequency is 92 MHz.

3.2 Low-Voltage Comparator Design

Although the 1.5-b/stage architecture greatly relaxes the offset tolerance of the comparators, for low voltage comparator where the available swing shrinks, careful design is required to guarantee the offset within acceptable range. Figure 6 shows the modified SC comparator from [2] to adapt SO structure. It consists of an SC network and a preamplifier followed by dynamic latch. Due to SO configuration, the input capacitors C_{S1} and C_{S2} should be permanently connected to the outputs of the previous stage. Therefore the reference voltage can only be provided by using separated capacitor branches. The comparator threshold voltages are determined by the ratio between input capacitor and reference capacitor. The capacitor ratios of C_S/C_R are 4:1 and 2:1 in the 1.5-b/stage and 2-b flash for $\pm(V_{REF}/4)$ and $\pm(V_{REF}/2)$ thresholds, respectively. Two additional capacitors C_A and C_B are placed at the input terminals of the preamplifier. This is because spikes during phase transitions may push V_A and V_B nodes to swing over V_{DD}, causing the adjacent PMOS switches to be forward biased [5]. The addition of these two capacitors can attenuate the instantaneous glitch and alleviate the possible charge loss.

4. Simulation Results

A 0.8-V 9-bit 10-MS/s pipelined ADC was designed employing the proposed S/H architecture as well as the merged switched-opamp and opamp-sharing technique. A 0.18-μm CMOS 1P6M process is used where the threshold voltage of NMOS and PMOS are both around 0.45 V. The supply voltage of the proposed ADC is specified as 0.8 V which is lower than the summation of V_{THN} and V_{THP}, i.e. 0.9 V, in order to exploit the advantage of switched-opamp architecture.

Since the latter stages in a pipelined ADC contribute to less input-referred noise and linearity error compared to former ones, stage scaling is applied along the pipeline for power optimization while satisfying the required SNR for a 9-bit ADC. The sampling capacitances in each stage are shown in Table 2.

The static characteristics are simulated with sine-wave histogram by applying a 200 kHz full-scale sine wave sampled at 10 MHz. As demonstrated in Fig. 7, the maximum differential nonlinearity (DNL) and integral nonlinearity (INL) are within 0.51 and 0.49 LSB, respectively. Figure 8 shows the 512-point FFT spectrum when 1.5 MHz input signal is applied to the ADC with 10 MHz sampling rate. The signal-to-noise-plus-distortion ratio (SNDR) achieves 52.3 dB, which corresponds to 8.4 effective-number-of-bits (ENOB). The SNDR and spurious-free dynamic range (SFDR) with different conversion rates when applying a 1.5 MHz input signal are depicted in Fig. 9(a). The maximum conversion speed is about 12 MS/s with a SNDR of 49.6 dB. Incomplete settling of the opamp at high sampling rates lead to increased harmonic and SFDR degradation. Figure 9(b) also illustrates the SNDR and SFDR with different input frequencies sampled at 10 MS/s. A SNDR drop can be observed at input frequency near $f_S/2$. This is caused by memory effect of opamp-sharing since no reset phase is available for the opamp input [17]. When the input fre-

Table 2 Sampling capacitance in each stage.

STAGE	C_s(pF)
S/H	1.2
STAGE 1	0.8
STAGE 2 & 3	0.6
STAGE 4 & 5	0.6
STAGE 6 & 7	0.4

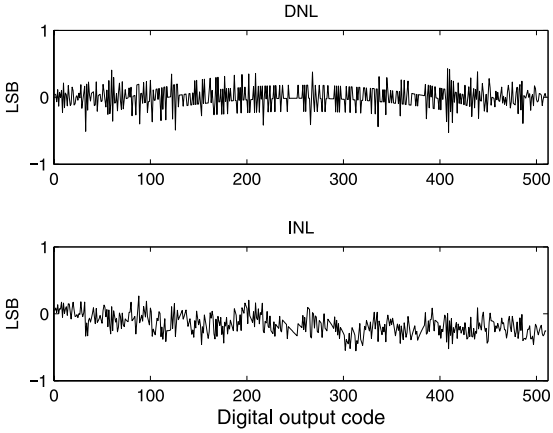

Fig. 7 DNL and INL plot.

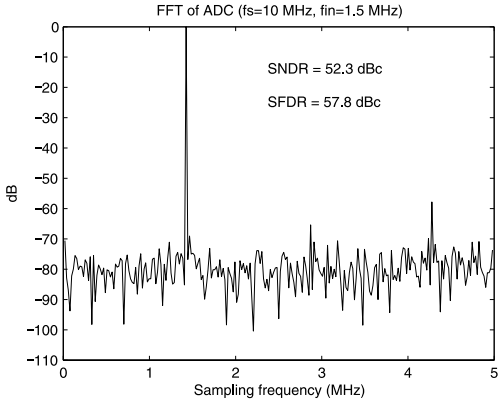

Fig. 8 FFT spectrum of 0.8-V pipelined ADC.

quency approaches $f_S/2$, the ADC samples almost twice within one period of input signal. Therefore the opamps without reset phase tend to "memorize" the previous state and settle in the wrong direction at the beginning. Extra slewing time is then needed before the opamps finally settle to the desired output. Such phenomenon seriously degrades the available settling time and therefore deteriorates the spectrum performances at near-Nyquist input frequencies.

Non-ideal device characteristics such as capacitor mismatch and Vth deviations may degrade ADC performance. Normally in a pipelined ADC, device imperfections will exhibit themselves in terms of offset and gain errors [21]. Offset can be greatly reduced or eliminated by the use of digital error correction. Gain error, which is usually the dominant

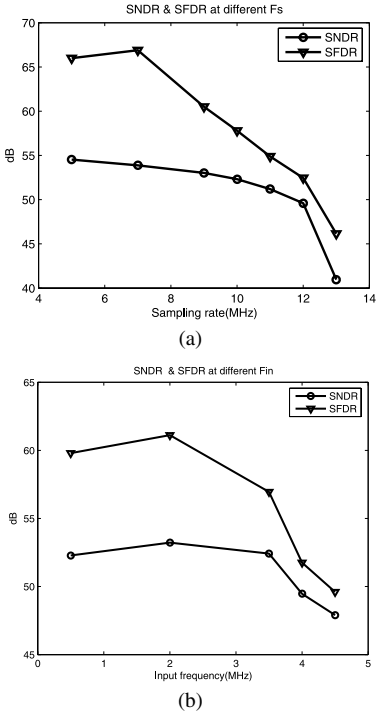

Fig. 9 SNDR and SFDR performance: (a) SNDR & SFDR at different f_S. (b) SNDR & SFDR at different f_{in} sampled at 10 MS/s.

Table 3 Power distribution in each block.

Block	Power(mW)
1st Opamp	0.46
2nd Opamp	0.37
3rd Opamp	0.37
4th Opamp	0.27
Comparators	0.51
Digital Logic & Clock Generator & Output Buffer	0.42
Total Power	2.4

Table 4 Summary of the simulation results (40°C).

Technology	0.18 μm CMOS
Supply Voltage	0.8 V
Resolution	9-bit
Conversion Rate	10 MSample/s
Full Scale Analog Input	0.8 V_{pp}
Maximum DNL	−0.51 /+0.49 LSB
Maximum INL	−0.49 /+0.37 LSB
SNDR/SFDR/ENOB @f_{in} = 1.5 MHz	52.3 dB/57.8 dB/ 8.4 bit
Total Power consumption	2.4 mW

error source, depends upon the accuracy of capacitor matching. In modern CMOS technology, the capacitor matching can achieve 10-bit level with careful layout techniques such as common-centroid and employing dummies. Therefore in our 9-bit ADC design, capacitor mismatch contributes to

Table 5 Comparison of proposed work with other SO-based pipelined ADC.

Design	Watari [8]	Vaz [9]	Wang [11]	Kim [12]	Wu [13]	This work
Technology	0.5-μm	0.18-μm	90-nm	0.18-μm	0.18-μm	0.18-μm
V_{DD}	1 V	1.5 V	1.2 V	1.8 V	1 V	0.8 V
Resolution	9-bit	10-bit	10-bit	8-bit	8-bit	9-bit
F_s (MS/s)	5	50	12	200	100	10
Power (mW)	1.6	29	3.3	30	30	2.4
SNDR (dB)	50	57.2	52.6	48	41.5	52.3
FOM1 (pJ/step)	1.24	0.98	0.8	0.73	3.09	0.71
FOM2 (pJ·V/setp)	1.24	1.48	0.96	1.31	3.09	0.57

minor degradation on ADC performance.

The total power of this pipelined ADC at 0.8 V supply is 2.4 mW including digital logic, clock generator and output buffers. The reference voltages 0.6 V and 0.2 V are designated to be provided from external source, so the power used to generate references voltage are not included in the power calculation. Table 3 shows the power distribution in each block, where opamp 1 to 4 correspond to the opamp allocation map in Fig. 3. The simulated performance of the proposed ADC is listed in Table 4 and a comparison with other switched-opamp based ADCs is given in Table 5. A widely used figure-of-merit (FOM1) for the evaluation of ADC is defined as

$$\text{FOM1} = \frac{Power}{2^{\text{ENOB}} \cdot f_s} \tag{4}$$

In low-voltage ADC, since the power consumption will inversely increase with reduced supply to maintain a specified SNR, another more appropriate FOM2 which reflects the difficulties for designs with reduced dynamic range is given by [22]

$$\text{FOM2} = \frac{Power}{2^{\text{ENOB}} \cdot f_s} \cdot V_{DD}. \tag{5}$$

In this definition, the proposed ADC has a FOM2 of 0.57 pJ/step, which is comparable to the lowest in SO-based ADC up to date.

5. Conclusion

Switched-opamp technique has been extensively employed in many switched-capacitor applications to deal with the poor conduction state of switches operated with low voltage supply. On the other hand, opamp sharing approach is an effective way to reduce the power consumption since it directly saves half the number of the required opamps. This paper proposed the methods and circuit structures required to reuse the opamps in a switched-opamp circuit configuration. In addition, a S/H with unity feedback factor in switched-opamp structure was proposed to further reduce the overall input-referred noise and also the power consumption. Using a 0.18-μm CMOS 1P6M process, a 0.8-V 9-bit 10-MS/s pipelined ADC with 2.4 mW and 0.71 pJ/step FOM has been designed and verified the proposed ideas.

Acknowledgments

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