LETTER

A Versatile Step-Up/Step-Down Switched-Capacitor-Based DC-DC Converter

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SUMMARY For battery-powered electronic products, one way to extend battery life is to use a versatile step-up/step-down DC-DC converter. A new versatile step-up/step-down switched-capacitor-based converter structure is proposed, and its efficiency is analyzed. In the step-down case, the efficiency is the same as, or even better than the efficiency of linear regulators.

key words: *DC-DC converter, switched-capacitor, step up, step down, efficiency*

1. Introduction

In recent years, it is a trend to integrate DC-DC converters with the system in a chip. Switching-capacitor-based DC-DC converters have drawn attention, since no bulky inductors are required and hence can be integrated into a monolithic chip [1]. In addition, an increasing number of battery-powered portable electronic products has been developed and introduced to market. How to increase a battery life has become an important topic. One way to extend battery life is to use a versatile step-up/step-down DC-DC converter to convert the battery voltage to the desired output voltage. When the battery voltage is higher than the desired output voltage, the DC-DC converter is configured to a step-down regulator. When the battery voltage is depleted lower than the desired output, the DC-DC converter is then configured to a step-up converter. Versatile DC-DC converters are attractive to portable electronics, such as laptops. For a given lithium ion battery, its battery life can be effectively prolonged with a versatile DC-DC converter, compared to the system equipped with a step-down only converter. Switching-capacitor (SC) converters have the potential to be versatile step-up/step-down DC-DC converters.

Although SC converters have many advantages, they have two main drawbacks. First, their voltage conversion ratio is usually predetermined by circuit structure; secondly, their line and load regulation capabilities are weak. Recently, different control schemes have been proposed to improve these issues. For example, a pulse-width-modulated (PWM) control scheme was used to control the charging time of the capacitors, and hence an adjustable voltage conversion ratio is achieved [2], [3]. An on-resistance control or current control scheme was used to increase voltage regulation capacities [4], [5].

In [5], a voltage doubler structure was adopted as a versatile step-up/step-down converter (its input voltage is 1.8–3.5 V and output voltage is set to 3.2 V). The circuit is redrawn in Fig. 1(a). For a voltage doubler structure, the upper limit of its power efficiency, η_{dou}, is determined by the ratio of its output and input voltages, V_{OUT} and V_{IN}, i.e.,

$$\eta_{dou} \leq \frac{V_{OUT}}{2V_{IN}}. \tag{1}$$

However, while V_{IN} is higher than V_{OUT}, its efficiency is lower than the efficiency of a linear regulator, η_{lin}, i.e.,

$$\eta_{lin} \approx \frac{V_{OUT}}{V_{IN}}. \tag{2}$$

Although a linear regulator can only be used in the step-down case, rather than in both the step-up and the step-down cases, lower efficiency in the step-down case is still a deficit for SC converters.

In fact, this issue can be solved by a slight modification. A modified versatile step-up/step-down converter circuit is

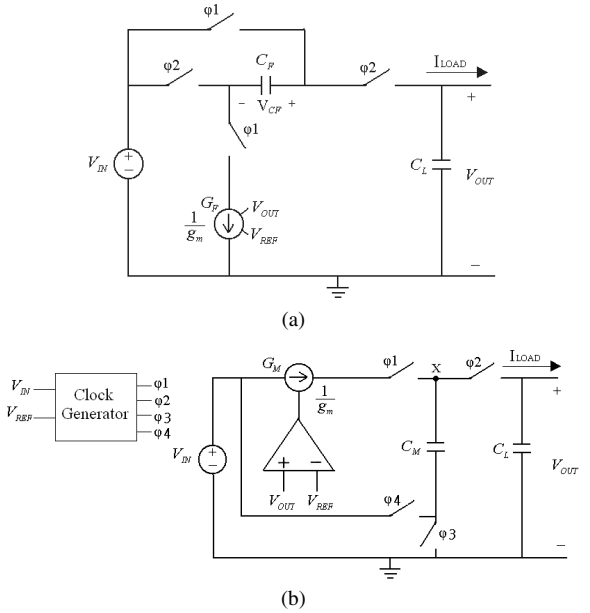

Fig. 1 (a) Regulated voltage doubler. (b) Modified versatile step-up/step-down converter.

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presented, which raises the efficiency in the step-down case to be the same as that of a linear regulator, while keeping the step-up efficiency the same as Eq. (1).

2. Proposed Step-Up/Step-Down SC-Based DC-DC Converter

Figure 1(b) shows the proposed circuit. The voltage-controlled current source (VCCS) is moved to near the input voltage source, rather than ground. There are also four switches, $\varphi1-\varphi4$, in the proposed circuit, and those switches are controlled by a control block, labeled as clock generator. The clock generator has two inputs, V_{IN} and V_{REF}, where V_{REF} is the desired output voltage and V_{OUT} should be the same as V_{REF} in a steady state. When V_{IN} is lower than V_{REF}, the proposed circuit acts as a step-up converter and Fig. 2(a) shows the clock timing diagram to drive the four switches. Both $\varphi1$ and $\varphi3$ are turned on during the charging phase, and the capacitor C_M is charged by the VCCS, G_M. In the discharging phase, both $\varphi2$ and $\varphi4$ are turned on, and C_M is flipped to be connected in series with the input voltage source to serve the load and C_L. When V_{IN} is higher than V_{REF}, the proposed circuit acts as a step-down converter with its switch timing diagram shown in Fig. 2(b). In the step-down case, switch $\varphi3$ is always turned on, while switch $\varphi4$ is always turned off. Switch $\varphi1$ is turned on during the charging phase, and C_M is charged by the VCCS, G_M. During the discharging phase, switch $\varphi1$ is turned off to isolate the load from the input voltage source. During this phase, switch $\varphi2$ is turned on, and the load and C_L are served by C_M. In both configurations, all clock signals are non-overlapping.

The power efficiency of the proposed circuit in the step-up case is also limited by Eq. (1) [5], and the efficiency in the step-down case is described as follows. Figure 3 shows its steady-state average current models with a constant current load, I_{LOAD}, during the charging and discharging phases, respectively, where r_1 and r_2 are equivalent on-resistance of the switches $\varphi1$ and $\varphi2$, respectively. In a steady state, the average current of C_M and C_L must be zero over a complete cycle. Otherwise, the capacitor voltages either increase or decrease until a steady-state solution is reached. Hence,

$$I_{CH(AVG)}D = I_{DIS(AVG)}(1-D) \tag{3}$$

$$I_{CL(AVG)}(1-D) = I_{LOAD}D \tag{4}$$

where $I_{CH(AVG)}$ is average charging current of C_M during the charging phase, $I_{DIS(AVG)}$ is average discharging current of C_M during the discharging phase, $I_{CL(AVG)}$ is average charging current of C_L during the discharging phase, and D is the duty ratio of the clock signal for switch $\varphi1$. During the discharging phase,

$$I_{DIS(AVG)} = I_{CL(AVG)} + I_{LOAD} = \frac{I_{LOAD}}{1-D}. \tag{5}$$

With Eqs. (3) and (5),

$$I_{LOAD} = DI_{CH(AVG)} \tag{6}$$

The input source provides current only during the charging phase. Thus, the power efficiency, η_{sc_d}, of the proposed circuit in the step-down case is

$$\eta_{sc\_d} \approx \frac{V_{OUT}I_{LOAD}}{V_{IN}I_{CH(AVG)}D} = \frac{V_{OUT}}{V_{IN}}, \tag{7}$$

which is the same as Eq. (2), the efficiency of a linear regulator.

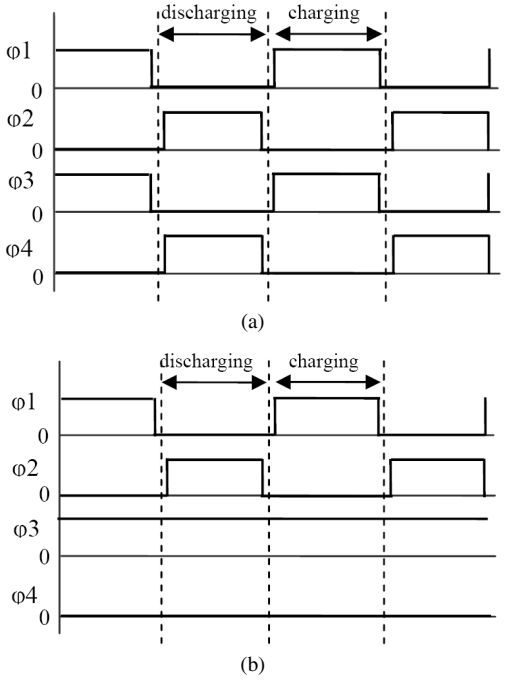

Fig. 2 Timing diagrams of four switches for the (a) step-up and (b) step-down configurations.

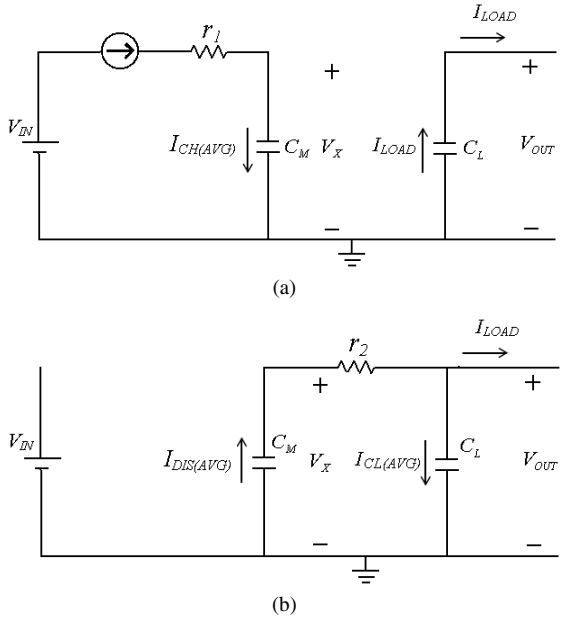

Fig. 3 The steady-state average current models with a constant current load: (a) charging phase (b) discharging phase.

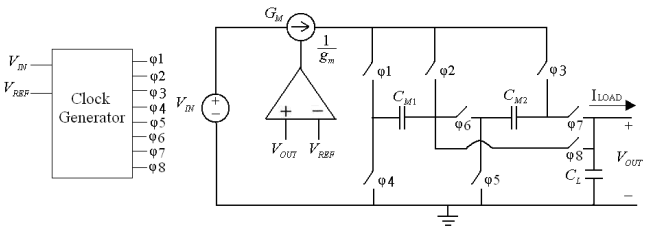

Fig. 4 A versatile step-up/step-down SC converter with a conversion ratio of up to three.

Theoretically, the voltage conversion ratio of the proposed circuit is between two and zero. If higher conversion ratio is needed, more capacitors are required. Figure 4 shows a versatile step-up/step-down SC converter with a conversion ratio of up to three. The circuit was derived from the series-parallel type power converter [6]. In [6], when there are two flying capacitors in the power converter, two transistors are manipulated for regulation, while only one is required for the circuit in Fig. 4. The efficiency of the proposed circuit in the step-up configuration is

$$\eta_{tri\_u} < \frac{V_{OUT}}{3V_{IN}}, \tag{8}$$

and its efficiency in the step-down configuration is

$$\eta_{tri\_d} < \frac{V_{OUT}}{V_{IN}}, \text{ for } 2V_{OUT} \geq V_{IN} > V_{OUT}, \tag{9}$$

$$\eta_{tri\_d} < \frac{2V_{OUT}}{V_{IN}}, \text{ for } V_{IN} > 2V_{OUT}. \tag{10}$$

They can be derived by the same approach described in Sect. 2. From Eq. (10), its efficiency is higher than that of a linear regulator for $V_{IN} > 2V_{OUT}$, with the price of an extra capacitor, more switches, and more complicated control circuits [7].

3. Simulation Results

The proposed circuit in Fig. 1(b) was implemented in TSMC 0.35 μm mixed-signal 2P4M polycide 3.3/5 V process. The output voltage is set to 3.3 V, and the input voltage range of the circuit is 2.2–5 V. The upper bound of the input range is limited by the maximal allowable supply voltage of the used process. The theoretical lower bound of the input range should be 1.65 V. However, the circuit implemented with the 0.35 μm process is supposed to be driven by a 3.3 V voltage. When the input voltage goes too low, some transistors fail to operate in their designated regions and the output voltage starts to drop.

Figure 5(a) shows the input and output waveforms for a step response in the step-up case, where V_{IN} is 2.5 V and V_{OUT} is stabilized at 3.3 V. Figure 5(b) shows the waveforms in the step-down case, where V_{IN} is 5 V and V_{OUT} is also stabilized at 3.3 V. Figure 6 shows the input voltage versus the power efficiency for a 7.5 mA current load. In high input voltage range, i.e., in the step-down case, the power efficiency is improved to be limited by Eq. (7), rather than

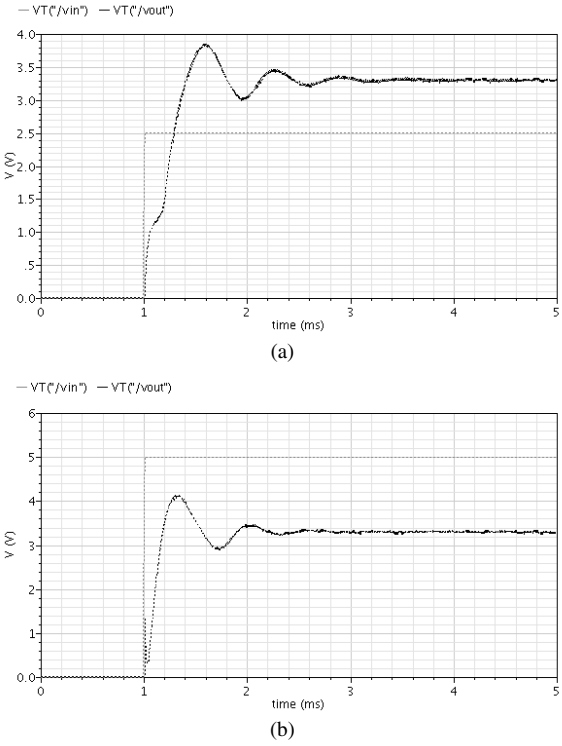

Fig. 5 Input and output waveforms for a step response in the (a) step-up and (b) step-down cases.

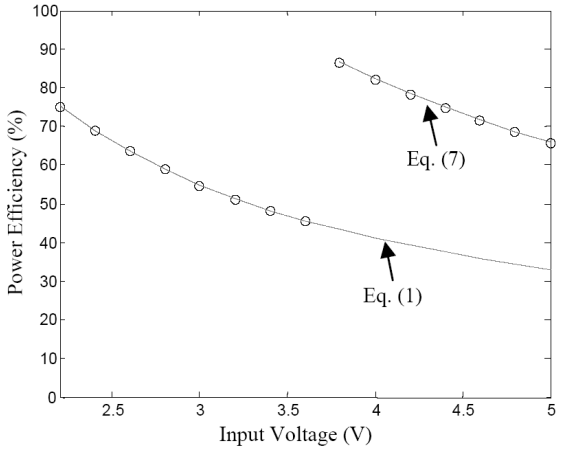

Fig. 6 Power efficiency versus input voltage for a 7.5 mA current load.

Eq. (1). In addition, one factor that affects the power efficiency is the on-resistance of switches. For low-power applications, the influence of this factor can be minimized by implementing the switches with transmission gates.

4. Discussion

In the step-down configuration, the proposed circuit is similar to a quasi-switched-capacitor (QSC) cell, which consists of a capacitor and two MOSFETs [8]. The only difference is that in a QSC cell, an implied switch is placed prior to the gate of the MOSFET that operates either in the saturation

region or cutoff region. In the proposed circuit, the switch, $\varphi 1$, is placed after the drain of the MOSFET, while the gate voltage of the MOSFET remains the same. Since the MOSFET is always turned on, the transition time between the charging and discharging phases is shorter, compared to the QSC cell. Besides, one disadvantage of SC converters is pulsating input current, which may cause electromagnetic interference (EMI) issues. In [8], two QSC cells are used to achieve continuous input current waveform. However, in low-power or battery-powered devices, input current pulsating may not be a serious problem, but one more capacitor, which is in the QSC cell, would definitely increase the size or chip area of the converter. Therefore, although the input current waveform of the proposed circuit is not continuous, it would be fine for low-power devices.

5. Conclusion

Improved versatile step-up/step-down SC converters are proposed, which can extend battery life and be realized by integrated circuit (IC) technology. In the step-up configuration, the efficiency is determined by the ratio of its output and input voltages. In the step-down configuration, the efficiency has been improved to be the same as, or even better than that of linear regulators, depending on the number of used capacitors.

Acknowledgments

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