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PAPER

A 0.8-V 250-MSample/s Double-Sampled Inverse-Flip-Around Sample-and-Hold Circuit Based on Switched-Opamp Architecture

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SUMMARY This paper proposes a low-voltage high-speed sample-and-hold (S/H) structure with excellent power efficiency. Based on the switched-opamp technique, an inverse-flip-around architecture which maximizes the feedback factor is employed in the proposed S/H. A skew-insensitive double-sampling mechanism is presented to increase the throughput by a factor of two while eliminating the timing mismatch associated with double-sampling circuits. Furthermore, a dual-input dual-output opamp is proposed to incorporate double-sampling into the switched-opamp based S/H. This opamp also removes the memory effect in double-sampling circuitry and features fast turn-on time to improve the speed performance in switched-opamp circuits. Simulation results using a 0.13-μm CMOS process model demonstrates the proposed S/H circuit has a total-harmonic-distortion of −67.3 dB up to 250 MSample/s and a $0.8V_{PP}$ input range at 0.8 V supply. The power consumption is 3.5 mW and the figure-of-merit is only 7.4 fJ/step.

key words: *switched-opamp, low-voltage, high-speed, sample-and-hold, double-sampling*

1. Introduction

Sample-and-hold (S/H) is a critical building block in many switched-capacitor (SC) systems, for example, the analog-to-digital converter (ADC). The main function of a S/H is to provide a stable output for the following stages with a specified precision even at high sampling rate. A S/H usually dominates the linearity, noise and power contribution of an overall system because it directly processes the front-end incoming signal [1]. Many S/H architectures have been proposed to achieve high speed while maintaining high linearity [2]–[12]. However not all of them are applicable in the low voltage realm. Driven by the rapid evolution of finer process technology and also the demand for lower power capability, low-voltage circuit design becomes an inevitable trend and choice. While digital power directly benefits from the scaling of supply voltage, analog circuits adversely suffer since the available signal range is shrunk as well [13]. Furthermore, the switch encounters poor conduction, and eventually complete floats, with reduced V_{DD} and hence deteriorates the performance of traditional SC circuits. To solve the floating switch problem, one of the promising methods is the switched-opamp (SO) technique, developed by Crols et al. [12], in which the floating switch is replaced by a switchable opamp which is able to charge and reset the sampling capacitor during its respective on and off phase.

S/Hs based on switched-opamp architecture are therefore suitable for low-voltage applications [6], [9]–[11], [14], [15]. However, the drawbacks of SO technique such as lower circuit feedback factor and additional opamp turn-on time prohibit SO-based S/H from operating at high speed [6], [12]. This paper proposes useful solutions to deal with the problems mentioned above. From the architectural perspective, an inverse-flip-around (IFA) architecture which improves the feedback factor is cooperated with double-sampling to achieve a 4-fold speed improvement in S/H. At the circuit level, a dual-input dual-output opamp structure which minimizes the turn-on time is proposed. More advantages will be clarified in the following sections.

This paper is organized as follows: Sect. 2 points out the disadvantages of conventional S/H structures and then comes up with the proposed IFA S/H architecture and its skew-insensitive double-sampled version. Section 3 details the opamp architecture specifically for the proposed double-sampled IFA S/H. Simulation results of the developed S/H using a 0.13-μm CMOS device models are shown in Sect. 4. Finally, Sect. 5 concludes this paper.

2. Double-Sampled Inverse-Flip-Around Sample-and-Hold

2.1 Low-Voltage S/H Design Issues

Flip-around S/H as depicted in Fig. 1(a) is the most widely used sample-and-hold architecture in SC applications due to its high speed and high linearity [2], [16]. The operation can be described as follows. During ϕ_1, the sampling capacitor C_S acquires the input signal. ϕ_{1A} is a slightly advanced phase of ϕ_1 to determine the sampling instant and avoid nonlinear charge injection. During ϕ_2, C_S is "flipped around" the opamp in a feedback loop and the charge stored in ϕ_1 are held in C_S to produce $V_{OUT} = V_{IN}$. High speed can be achieved in this architecture since the feedback factor β is ideally equal to 1 neglecting the input parasitic capacitance of opamp. However, the flip-around S/H is not applicable at low supply voltage due to the floating switch problem. As shown in Fig. 1(a), switches S_1 to S_3 are connected to either the system input or the opamp output, therefore they must process a rail-to-rail signal range. At a low voltage supply, these floating switches may encounter poor conduction or even turn off since none of the transmission MOS in a switch will turn on. The insufficient conduction of floating switches thereby prohibits the flip-around architecture from direct employment in low voltage S/H. Several excel-

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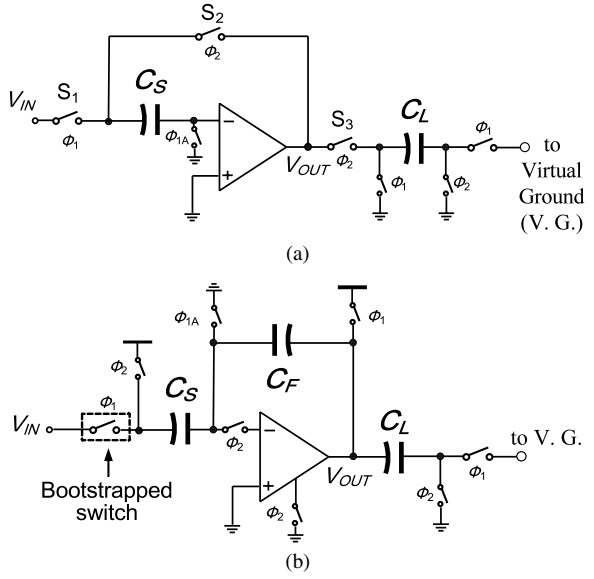

Fig. 1 Conventional S/H architectures. (a) Flip-around architecture [2], [16], (b) low-voltage SO-based S/H [14], [15].

lent works concerning low-voltage sampling circuits have been proposed [6], [9]–[11], [14], [15]. Figure 1(b) shows a charge-redistribution S/H architecture which is commonly employed in low-voltage systems based on switched-opamp architecture [14], [15]. The operation is as follows. During ϕ_1, the opamp turns off and C_S samples the input while C_F is reset. During ϕ_2, the opamp is activated and the input charge stored in ϕ_1 transfers from C_S to C_F to produce the corresponding V_{OUT}. In this architecture, a bootstrapped switch [17] is used to interface the input signal for high linearity. All the other switches are connected to either V_{DD} or ground and hence no floating switches exist. A major drawback of this SO-based S/H is the reduced feedback factor compared to the conventional flip-around architecture. A reduced feedback factor β directly degrades the speed and noise performance [1], [16]. For a sample-and-hold circuit, the maximum sampling rate is determined by the opamp bandwidth, feedback factor, as well as the required linearity. Since the opamp's output must settle within $\pm 1/2^{N+1}$ full scale range to achieve N-bit linearity in half of the sampling period, the maximum sampling rate of an N-bit S/H in terms of opamp bandwidth and feedback factor can be expressed as [1]

$$f_S < \frac{\pi \cdot \beta \cdot f_T}{(N+1) \cdot \ln 2} \tag{1}$$

where β is the feedback factor, f_T is the unity gain frequency of the opamp, and f_S is the sampling rate. On the other hand, the output-referred noise $\overline{v_o^2}$ can be approximated by [1]

$$\overline{v_o^2} = \frac{kT}{\beta C_F} \tag{2}$$

where k is the Boltzmann's constant and T is the absolute temperature. Compared to the flip-around S/H, the sampling

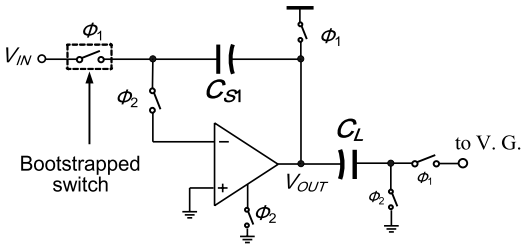

Fig. 2 Inverse-Flip-Around(IFA) S/H with unity feedback factor based on switched-opamp architecture.

speed and noise performance of the S/H in Fig. 1(b) both degrade by a factor of two due to the reduced feedback factor. A lower feedback factor also implies more power consumption if the same speed or signal-to-noise ratio (SNR) are required to be achieved. In the following contexts, we propose a SO-based S/H circuit in combination with double-sampling to solve these deficiencies.

2.2 Inverse Flip-Around S/H Architecture

The concept of the proposed SO-based S/H is by observing the features of the switched-opamp architecture in two aspects: (i) the feedback capacitor must be permanently connected to the output nodes of the opamp in a switched-opamp architecture; (ii) the opamp must be turned-off in one of the two non-overlapped phases, during which the output stage can be pulled to V_{DD} or ground using additional switches. From the observations stated above, the sampling action can be realized by directly attaching the sampling capacitor onto the opamp output node instead of connecting it to ground using a switch as in Fig. 1(b). The proposed S/H architecture is shown in Fig. 2 where a single-ended configuration is used for explanation. C_{S1} samples the input signal respect to V_{DD} at ϕ_1 since the opamp is currently turned-off and the output node is pulled to V_{DD}. During ϕ_2, the input signal path is terminated by turning off the bootstrapped switch, while the top plate of C_{S1} is connected to the opamp inverting input, resulting in an unity feedback and $V_{OUT} = V_{DD} - V_{IN}$. The inversed polarity issue can be easily resolved in fully-differential configuration. The name "inverse-flip-around (IFA)" indicates the S/H structure operates in an inverse fashion compared to traditional "flip-around" S/H structure. In Fig. 1(a), the input signal is sampled respect to the opamp input during ϕ_1 and the bottom plate of C_S is flipped to opamp output during ϕ_2. On the contrary, in the proposed S/H structure depicted in Fig. 2, the input is sampled respect to the opamp output during ϕ_1 and the top plate of C_S is flipped to opamp input during ϕ_2. Such configuration exploits the features of switched-opamp architecture, i.e. the (i) and (ii) stated above, and turns these drawbacks into benefits. It has the following advantages: The settling speed is potentially doubled compared to the S/H in Fig. 1(b) since the feedback factor is now ideally equal to 1 rather than 1/2. The improvement in feedback factor also implies the output-referred noise of the S/H is re-

duced by half according to Eq. (2). S/H usually dominates the system noise performance because it locates at the front-end while the following stages may attenuate their resulting noise through the interstage gain [1]. Reduced noise also indicates smaller loading capacitance and hence higher speed and lower power consumption can be achieved from system perspective. A minor advantage of the IFA S/H compared to Fig. 1(b) is that it only has one capacitor and hence no gain error induced from capacitor mismatch.

Charge injection and clock feedthrough errors in S/H circuits in Fig. 1(a) and Fig. 1(b) can be regarded as a DC offset by using an advanced clock phase ϕ_{1A}. In the proposed scheme, the advanced clock phase is not required because the bootstrapped switch always ensures a constant overdrive voltage. The channel charge stored in the bootstrapped switch can be expressed as

$$Q_{ch} = C_{OX} \cdot W \cdot L \cdot (V_{GS} - V_{TH}) \tag{3}$$

where Q_{ch} is the channel charge and C_{OX} is the gate capacitance per unit area. Since $V_{GS} - V_{TH}$ is fixed by the bootstrapping behavior, the released charge during turn-off is independent of the input signal, and the resulting injection can be regarded as a DC offset which can be largely reduced by fully-differential structure. Besides, all the other switches are connected to V_{DD}, ground or virtual ground. Hence their respective charge injections are also independent of the input signal. Furthermore, the clock feedthrough and threshold voltage variation due to body effect which contributes to high-order distortion can be alleviated by properly minimizing the bootstrapped switch size as long as the settling requirement is satisfied.

2.3 Skew-Insensitive Double-Sampling IFA S/H

The proposed IFA S/H improves the potential sampling rate by a factor of two. Its throughput can be further enhanced by applying the double-sampling concept [2], [14], [18], [19]. Normally, an opamp in SC S/H circuits idles in sampling mode and operates in hold mode. Double-sampled S/H [2] reuses the opamp in idle mode and produces a two-fold throughput. The conceptual diagram of applying double-sampling in the proposed IFA S/H is depicted in Fig. 3(a) with a single-ended configuration. Practically, the manipulation of double-sampling into IFA S/H incurs three significant problems. First, double-sampling is not compatible with switched-opamp architecture. This is because double-sampling is inherent a kind of opamp-sharing in time domain. It demands the opamp to be active in both phases. On the contrary, switched-opamp technique requires the opamp to turn off in one of the two non-overlapped phases. As a result, the adaptation of double-sampling into the SO-based IFA S/H requires not only two sets of hardware but also additional modification of the opamp structure. In the proposed opamp design, dual output stages are used to solve this dilemma. When one of the dual output stages is turned on to hold the sampled input, the other is turned off and provides the required high impedance for the following stage.

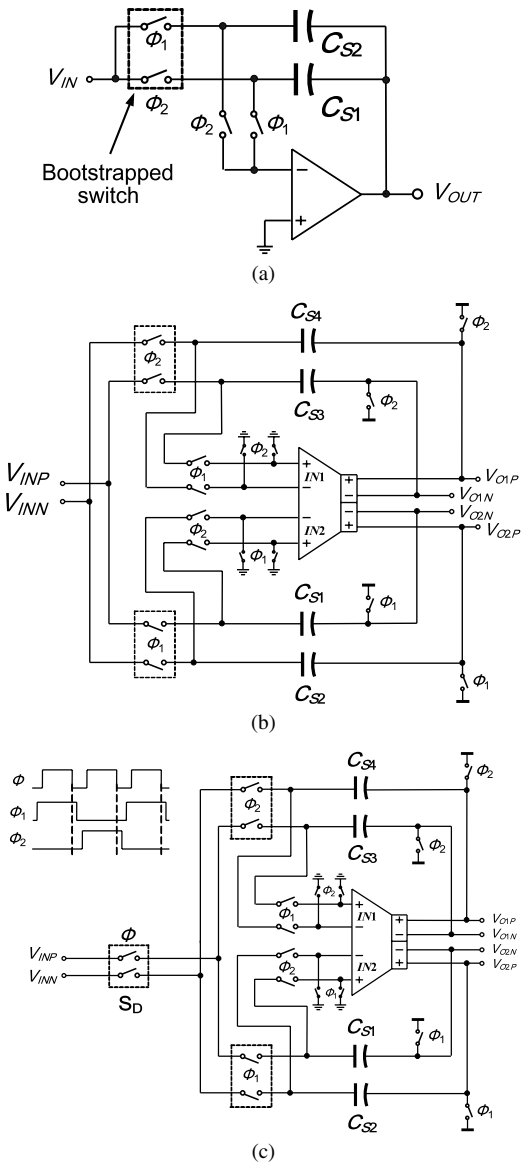

Fig. 3 Proposed double-sampled IFA S/H: (a) Conceptual diagram, (b) fully-differential IFA S/H with double-sampling, and (c) fully-differential IFA S/H with skew-insensitive double-sampling.

The detailed opamp circuit will be described in Sect. 3.

The second problem caused by double-sampling is the memory effect on the opamp input which is never reset in both clock phases [19]. Due to finite opamp gain, the present opamp output is polluted by the charge "memorized" in the input parasitic capacitors. In the proposed opamp design, one more differential input pair is added to eliminate this side-effect. By resetting the input pair which is inactive and keep the other input pair active, the opamp operation is maintained and the memory effect is removed. As a consequence, to solve the two problems mentioned above, a dual-input dual-output switchable opamp is necessary. Based on the opamp requirement described above, a fully differential version of Fig. 3(a) is depicted in Fig. 3(b). Note the opamp symbol has two input pairs ($IN1$ & $IN2$) and two output

stages (V_{O1} & V_{O2}). The switches enclosed in dashed boxes represent the bootstrapped switches. All the other switches are simply realized with NMOS or PMOS transistors.

The third issue of double-sampled S/H is due to timing mismatch between its two channels. Since the two channels are controlled by two non-overlapped clock phases, the turning-off timing skew between ϕ_1 and ϕ_2 leads to non-uniform sampling and hence distortion. A spurious tone located at $f_S/2-f_{in}$ is generated with a magnitude proportional to the timing error and input frequency f_{in} [2], [20]. The spectral components of a double-sampled sinusoidal signal V_{in} with timing skew can be expressed as

$$\frac{1}{2T}\sum_{n=-\infty}^{\infty} V_{in}\left(f_{in}-n\frac{f_S}{2}\right) \times\left[1+e^{-jn\pi}\times e^{j2\pi\Delta T(f_{in}-n(f_S/2))}\right] \quad (4)$$

where T is the clock period and ΔT is the timing skew error. The magnitude of the spur is about $20\log(|\pi\Delta T f_{in}|)$ by using the small angle approximation.

Figure 3(c) demonstrates the proposed skew-insensitive circuit architecture of the double-sampled IFA S/H and its timing diagram. The concept in [8], [21] is adapted here, but the switch selection and allocation are rearranged to adapt the IFA S/H. The circuit operation is explained as follows. The bootstrapped switches denoted S_D are controlled by a special clock phase ϕ which uniquely determines the sampling instant. As depicted in the timing diagram of Fig. 3(c), ϕ has a frequency two times of those of ϕ_1 and ϕ_2. Its falling edge is slightly advanced before the falling edges of ϕ_1 and ϕ_2. During ϕ_1, output stage V_{O1} is turned on but output stage V_{O2} is turned off. When $\phi = 1$, the differential input signals can be sampled on C_{S1} and C_{S2} respect to V_{DD} by connecting V_{O2P} and V_{O2N} to V_{DD}. When ϕ transits from V_{DD} to ground, S_D is open and the input sampling path is terminated. Since the falling edge of ϕ precedes that of ϕ_1, the stored charge is determined by ϕ and independent of ϕ_1. During ϕ_2, the output stage V_{O2} is activated, the top plates of C_{S1} and C_{S2} are connected to input pair $IN2$ to form the feedback loop, and the held output are available on output stage V_{O2}. Similar operation applies for the second sampling loop constructed by C_{S3} and C_{S4}. By the timing control of an extra phase ϕ, the timing skew between ϕ_1 and ϕ_2 no longer affects the sampling instant and thus alleviates the non-uniform sampling effect. In addition, it is worthy to note that since the sampled output are available at two distinct output pairs, the proposed S/H can be directly applied on two-channel pipelined analog-to-digital converters such as in [14].

3. Opamp Design

One critical speed-limiting factor of SO-based circuits is the slow turn-on time of the switchable opamp. This is because the opamp requires additional time period to recover to normal operation from a disabled state [12]. The proposed IFA S/H has optimized its sampling speed from architectural level by improving the feedback factor and adopting double-sampling. In the circuit level, an opamp with fast turn-on time is proposed. Figure 4 shows the opamp structure employed in the double-sampled IFA S/H. Several requirements have to be satisfied in order to implement this S/H. Since the supply voltage is only 0.8 V, the opamp is generally designed to have an input common-mode of either V_{DD} or ground [12]. In the IFA S/H, the input signal is sampled respect to V_{DD} by using the disabled output pairs; therefore in order to balance the common-mode signal, the input common-mode of opamp has to be set to ground. The opamp is essentially a Miller-compensated two-stage opamp. The input stage adopts folded-cascode structure and consists of two PMOS input pairs. These two input pairs commonly share a single bias current switched alternatively with ϕ_1 and ϕ_2. Whenever one of the dual input pairs is disabled by turning off the switch M_{S1} or M_{S2}, the gate terminals of that input pair can be reset to ground. Such mechanism removes the memorized charge residing at the opamp input parasitics while still maintaining the same amount of bias current.

There are also two sets of output stages but the pairing assignment is different from the dual input pairs. V_{O1P} and V_{O2P} share a common bias current in different phases and so do V_{O1N} and V_{O2N}. The operation of the output stages is as follows. During ϕ_1, M_{S3}/M_{S5} and M_{S9}/M_{S10} turn on while M_{S4}/M_{S6} and M_{S7}/M_{S8} turn off. The current of M_9 and M_{10} are directed to V_{O1P} and V_{O1N} respectively. V_{O2P} and V_{O2N} nodes are in high impedance state since no currents flow through them, and they are referred to V_{DD} by M_{S9}/M_{S10}. During ϕ_2, the roles exchange while operating in the same manner. Such arrangement ensures the current paths established by M_9 and M_{10} are never turned off and hence a faster turn-on time can be achieved. Although there are two sets of input pairs and output stages, the power consumption is not doubled due to the bias current reuse. The dynamic SC common-mode feedback (CMFB) circuit as shown in Fig. 4(b) is used to provide proper output common-mode level control. Two sets of SC branches are required for dual output stages in both phases. The error amplifier compares the SC level-shifted output common-mode with ground level and provides the correct polarity for CMFB control signal (V_{CMFB}). The circuit of error amplifier is simply the same as the input stage of the main opamp.

The opamp is designed to meet the specification of the IFA S/H. From Eq. (1), a 250 MS/s, 10-bit S/H with double-sampling requires an opamp with an unity-gain frequency more than 300 MHz, assuming $\beta = 1$ and neglecting slew rate and finite clock transition time for simplicity. In practice, nonlinear settling limited by slew rate shortens the available linear settling time and hence a much higher opamp bandwidth is required. Simulation results show the opamp achieves a 67.5-dB DC gain with a 74° phase margin. The unity-gain frequency is 575 MHz and a static power of 1.9 mW is consumed from a 0.8 V supply.

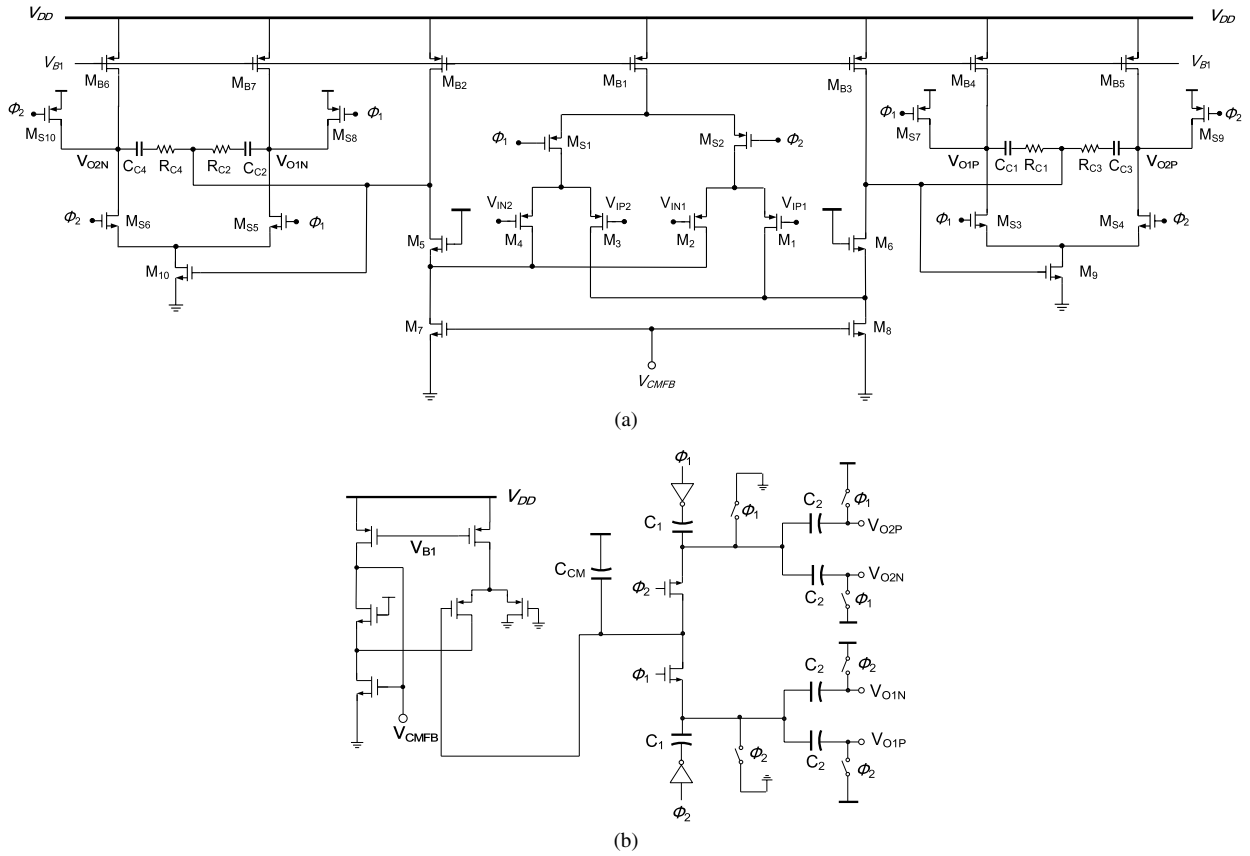

Fig. 4 Opamp with dual-input pairs and dual output stages. (a) Main opamp, (b) common-mode feedback circuits.

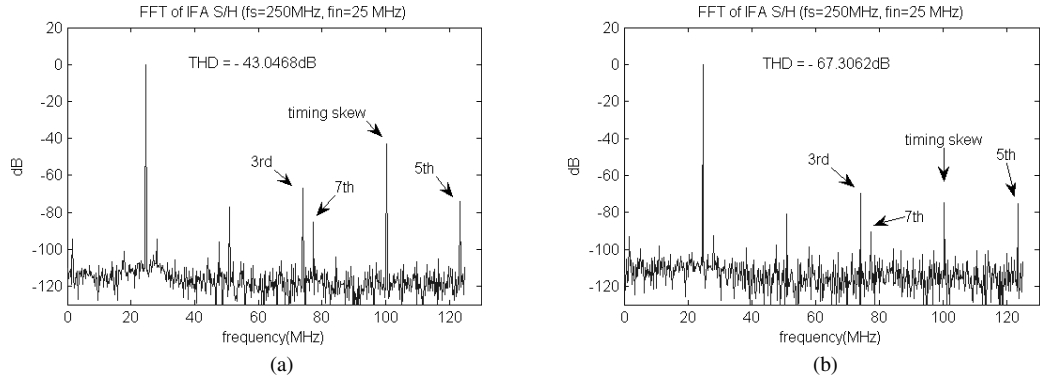

Fig. 5 FFT spectrum of IFA S/H at 250 MHz sampling rate with 25 MHz input frequency. (a) Before using skew-insensitive scheme, (b) after using skew-insensitive scheme.

4. Simulation Results

The proposed sample-and-hold has been designed at 0.8-V using a 0.13-μm CMOS process model. The threshold voltages of NMOS and PMOS are about 0.35 V and −0.3 V, respectively. A sampling capacitor of 1.2 pF and loading capacitor of 1 pF are used in the S/H. The capacitor value settings are aimed at satisfying the thermal noise requirement of a 10-bit ADC application [1]. The S/H is clocked at 125 MHz and the equivalent sampling rate is 250 MSample/s by employing double-sampling. Figure 5 shows the FFT spectra of the double-sampled IFA S/H. Both the FFT spectra of the circuit implementations in Fig. 3(b) and Fig. 3(c) are given to illustrate the effectiveness of the proposed skew-insensitive double-sampling scheme. A 0.8-V_{PP}, 25 MHz differential input signal is applied with a 0.1 ns falling edge mismatch between ϕ_1 and ϕ_2, which corresponds to 2.5% mismatch for a 250 MHz sampling rate. The spectra before and after adopting the skew-insensitive mechanism are shown in Fig. 5(a) and Fig. 5(b), respectively. The total-harmonic-distortion (THD) improves from −43 dB to

−67 dB. The spurious tone located at $f_S/2 - f_{in}$ which corresponds to the timing-skew is obviously cancelled by the skew-insensitive circuitry. The THD vs. different input amplitudes of the skew-insensitive double-sampled IFA S/H is plotted in Fig. 6. A 0.1 ns timing error is also added in the simulation. As can be expected, smaller signals bring in less harmonic distortion and hence better THD. More than 10-bit linearity can be achieved with a 0.9 V_{PP} input signal and 9-bit linearity for a 1 V_{PP} signal. The degradation at larger input amplitudes mainly comes from the nonlinearity due to finite opamp gain since the large input swing forces the output transistors into triode region. The total power consumption at 0.8 V is 3.5 mW, including the ones of clock generator and bias circuitry. A specification summary is given in Table 1. The comparison with previous works is shown in Table 2 which includes high-speed [2], [22] and low-voltage [6], [8], [11] cases. As can be observed in the table, this work has the lowest supply voltage and highest sampling speed while maintaining comparable linearity. In addition, the proposed IFA S/H has the largest ratio of input-range to supply voltage, which is a significant index especially in low-voltage design since the available signal swing is limited. A figure-of-merit (FOM) commonly used to evaluate the performance of S/H or ADC is expressed as FOM1 [8]:

$$FOM1 = \frac{Power}{2^{ENOB} \cdot f_S} \tag{5}$$

Taking the design complexity of low-voltage circuit into consideration, FOM1 can be modified as FOM2 [23] described below:

$$FOM2 = \frac{Power}{2^{ENOB} \cdot f_S} \cdot V_{DD} \tag{6}$$

The proposed S/H compares favorably with other state-of-the-art works.

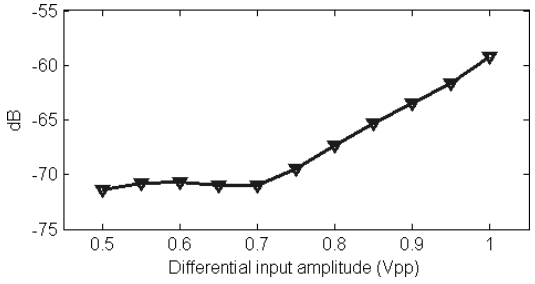

Fig. 6 Total harmonic distortion with different input amplitude.

Table 1 Summary of the simulation results (40°C).

Technology	0.13-μm CMOS
Supply Voltage	0.8 V
Sampling Rate	250 MSample/s
Input Range(differential)	0.8 V_{pp}
THD	−67.3 dB@ f_{in} = 24.658 MHz
Total Power Consumption	3.5 mW

5. Conclusion

Switched-opamp technique renders an effective solution for the floating switch problem in low-voltage SC circuitry. However inferior speed performance becomes the major limitation of SO-based circuits due to its lower circuit feedback factor and longer opamp turn-on delay. In this paper, we proposed a SO-based S/H architecture which operates up to 250 MS/s with a 0.8 V supply. In the architectural level, an inverse-flip-around S/H which maximizes the feedback factor is presented. Together with double-sampling, the potential sampling rate is 4-fold compared to conventional SO-based S/H. Additionally, in the circuit level, a dual-input dual-output opamp with short turn-on delay is adopted to boost the overall performance. The side-effects brought by double-sampling are also compensated by the opamp design. Simulation results show that the FOM of the proposed S/H achieves 7.4 fJ/step which compares favorably with other published results. Its low-voltage, low-power, high-speed characteristics are especially suitable for modern high-speed ADC applications.

Acknowledgment

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Table 2 Comparison of proposed work with other SO-based pipelined ADC.

Design	Waltari [2]	Lee [22]	Baschirotto [6]	Lee [8]	Keskin [11]*	This work*
Technology	0.5-μm	0.5-μm	0.5-μm	0.35-μm	0.35-μm	0.13-μm
V_{DD}	3 V	3 V	1.2 V	1.5 V	1 V	0.8 V
Full-Scale Input(V_{PP})	1.8	0.8	0.825	0.8	0.8	0.8
F_s (MS/s)	220	200	40	50	20	250
THD @ f_{in}	−62 dB @73 MHz	−56.5 dB @75 MHz	−50 dB @2 MHz	−58.2 dB @2.5 MHz	−64 dB @10 MHz	−67.3 dB @25 MHz
Power (mW)	25	4.8	1.2	2.6	N.A.**	3.5
FOM1 (fJ/step)	110.4	43.9	116.1	78.3	N.A.	7.4
FOM2 (fJ·V/step)	331.4	131.8	139.3	117.4	N.A.	5.9

* This work and ref[11] provide simulation results. All the other works are experimental results.
** The opamp power is not given in the sampling circuit in [11], hence the total power is not available.

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