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Oscillator-Based Reconfigurable Sinusoidal Signal Generator for ADC BIST

Hsin-Wen Ting · Cheng-Wu Lin · Bin-Da Liu · Soon-Jyh Chang

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Abstract In order to perform an on-chip test for characterizing both static and transmission parameters of embedded analog-to-digital converters (ADCs), this paper presents an oscillator-based reconfigurable sinusoidal signal generator which can produce both high and low frequency sinusoidal signals by switching the oscillator into different modes. Analog and digital signals can additionally be produced concurrently in both modes to provide not only test stimuli, but also reference responses for the ADC built-in self-test. The generated oscillation signal amplitude and frequency can be easily and precisely controlled by simply setting the oscillator clock frequency and initial condition coefficients. Except for a 1-bit digital-to-analog converter and smoothing filter, this proposed generator is constructed entirely by digital circuits, and hence easily integrates this silicon function and verifies itself before testing the ADCs.

Keywords Reconfigurable oscillator · Sinusoidal signal generator · Sigma–delta modulator

1 Introduction

With advancing integrated circuit manufacturing technology, to realize a complex system on a single chip (SoC) has become today's main IC design trend. Since there are increasingly more analog and mixed-signal circuits integrated in the chip, realizing a complete system on a single chip becomes more difficult. SoC chip testing is challenging, especially because of its growing analog and mixed-signal cores. The most frequently used mixed-signal blocks are analog-to-digital (ADC) and digital-to-analog (DAC) converters. Conventional test methods for analog and mixed-signal circuits mainly focus on functional tests, which are both expensive and time-consuming. One promising strategy for resolving this problem is the built-in self-test (BIST) approach, in which both stimulus generation and response analysis are performed on the same chip [4, 8, 13] as shown in Fig. 1. The test stimulus generator is one of the key building blocks in the ADC BIST scheme. Developing a flexible and easy-to-realize test stimulus generator for ADCs testing is the focus of this paper.

A sigma–delta ($\Sigma\Delta$) modulator based signal generator, as shown in Fig. 2, which can produce low-frequency high-quality sinusoidal signal has been proposed in [9]. In their signal generation scheme, however, only ADC static parameters i.e. offset error, gain error, integral nonlinearity (INL) and differential nonlinearity (DNL), can be extracted. The generated oscillation frequency can only be about 0.2% of the clock frequency sourced from the trade-off between signal quality and over-sampling ratio (OSR) [9]. In addition to static behaviors, transmission performance is also important in characterizing an ADC. In [14–16], a band-pass $\Sigma\Delta$ modulator based sinusoidal signal generator was proposed to generate high frequency test stimulus. It can generate high frequency, up to one-quarter clock frequency, analog test stimuli to test transmission specifications, such as signal-to-noise-and-distortion ratio (SNDR) and an effective number of bit (ENOB), of an ADC. However, the generated analog stimulus quality is sensitive to the analog smoothing filter characteristic. For example, signal-to-noise ratio (SNR) of the generated sinusoidal test

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H.-W. Ting (✉) · C.-W. Lin · B.-D. Liu · S.-J. Chang
Department of Electrical Engineering,
National Cheng-Kung University,
Tainan, Taiwan
e-mail: hwt93@spic.ee.ncku.edu.tw

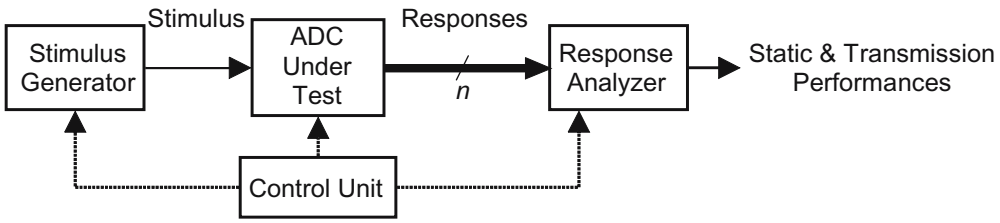

Fig. 1 General ADC BIST scheme

stimulus may degrade significantly if the central frequency of the smoothing band-pass filter is deviated. In general, more design efforts are necessary to better determine central frequency of the analog band-pass filter. Therefore, to alleviate the analog band-pass smoothing filter design difficulty, a new reconfigurable oscillator based sinusoidal signal generator is proposed. It shapes the generated bit-stream noise level to a lower frequency band instead of the conventional lower and higher frequency bands.

Conventionally, distinct signal generators are employed to provide a high- and low-frequency sinusoidal test stimulus to extract ADC static and transmission parameters, respectively. However, it is area expensive to realize different signal generators on chip to provide both high- and low-frequency signals. Furthermore, in order to on-chip analyze the measured responses, a huge reference response volume must be stored in memory and transported to the response analyzer for comparison, requiring a large amount of memory and long test time. An oscillator-based reconfigurable sinusoidal signal generator which can produce not only a low frequency but also a high frequency signal by switching the oscillator into a different mode is proposed in this paper for reducing hardware overhead. In addition, analog test stimuli and digital reference responses can be produced concurrently in both modes. With this on-chip reference response generation, additional memory and time to store and transport reference responses is not required.

The paper is organized as follows: The basic oscillator based signal generator concept is introduced in Section 2. The architecture and operations of the proposed oscillator-based reconfigurable signal generator and the considerations of device resolution and stimuli accuracy are described in Section 3. The concurrent signal generation concept is also explained in this section. The simulation results demonstrate the proposed architecture the effectiveness in Section 4. Finally, the paper is concluded in Section 5.

2 The Oscillator

The basic digital oscillator scheme [9, 16] is shown in Fig. 3. The characteristic equation of this oscillator is given by

$$z^{-2} + \left(K_f - K_c\right)z^{-1} + 1 = 0 \tag{1}$$

Let $K = K_c - K_f$, the roots of Eq. 1 are expressed as Eq. 2 and will lie on the unit circle with K is between −2 and 2.

$$z = \frac{K \pm \sqrt{K^2 - 4}}{2} = e^{j2\pi\frac{f_{OSC}}{f_{CLK}}} \tag{2}$$

Based on the above equation, the oscillation frequency relationship w.r.t. the coefficient $K\left(= K_c - K_f\right)$ can be plotted as shown in Fig. 4. For values of coefficient K between ±2, the oscillation frequency of the oscillator varies continuously between very low frequency and half the clock frequency. When the coefficient K approaches to 2, the oscillation frequency is much lower compared to the clock frequency. The low-frequency oscillating signal can be employed to determine the static parameters of an ADC.

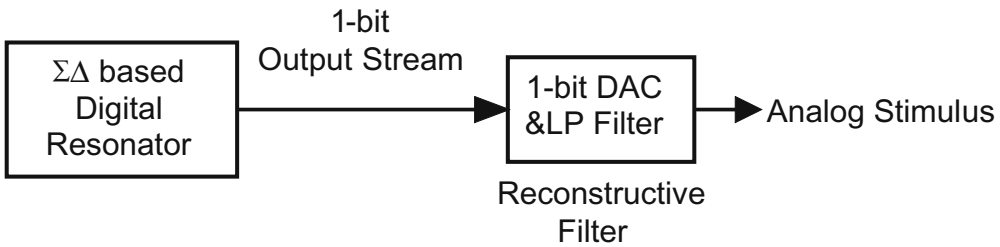

Fig. 2 A sigma–delta (ΣΔ) modulator based signal generator

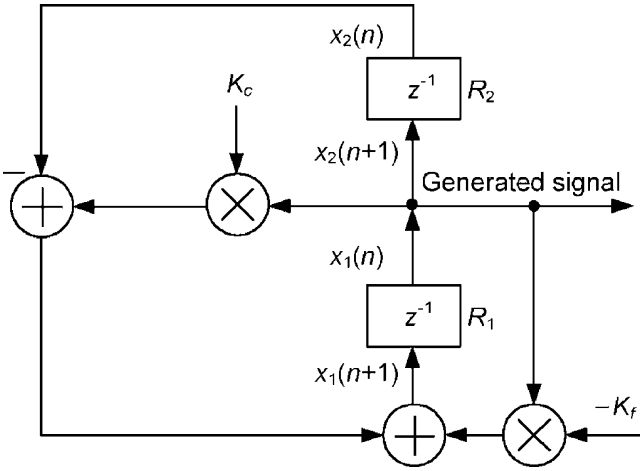

Fig. 3 The basic digital oscillator

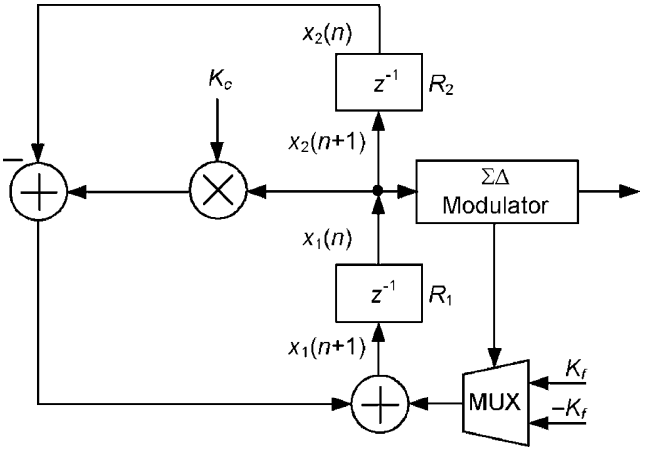

Fig. 5 The sigma–delta modulation based digital oscillator

In addition, the oscillation frequency can be up to half the clock frequency when coefficient K approaches to −2. The high-frequency oscillating signal can be served as the stimuli in determining the transmission parameters.

Precisely, the corresponding oscillation frequency (f_{OSC}), amplitude (A), and phase (ϕ) of the oscillating signal can be expressed as the following equations [15] if the clock frequency is f_{CLK}.

$$f_{OSC} = \left[\pi - \arccos\left(\frac{-K}{2}\right)\right]\frac{f_{CLK}}{2\pi} \tag{3}$$

$$A = \frac{x_1(0)}{\sin\phi} \tag{4}$$

$$\tan\phi = \frac{x_1(0)\sin\left(2\pi f_{OSC}/f_{CLK}\right)}{x_1(0)\cos\left(2\pi f_{OSC}/f_{CLK}\right) - x_2(0)} \tag{5}$$

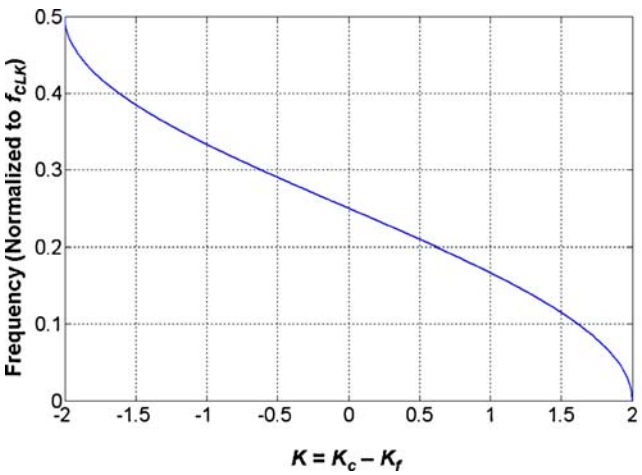

Fig. 4 The relationship between oscillation frequency and coefficient K

3 Oscillator-Based Reconfigurable Signal Generator

An oscillator-based reconfigurable sinusoidal signal generator providing test stimuli and reference signal for embedded ADC is developed in this section. One approach for realizing the sinusoidal signal generator is to combine the digital oscillator with a multi-bit DAC and a smoothing filter. However, the linearity and area overhead of the multi-bit DAC are major challenges. Another promising structure is the sigma–delta (ΣΔ) modulation based signal generator [9, 16] in which a ΣΔ modulator is integrated into the digital oscillator. By using this approach, the analog test stimuli can be easily constructed by using a 1-bit DAC and filter if a 1-bit ΣΔ modulator is incorporated. The inherent linearity and small area overhead of a 1-bit DAC are two of the major advantages of this approach.

3.1 Architecture

A 1-bit ΣΔ modulator at the oscillator output can be inserted, shown in Fig. 5, to suppress the in-band noise and one of the multipliers can also be replaced by a 2-to-1 multiplexer [7, 9] to reduce circuit complexity.

To generate a low frequency sinusoidal signal, the coefficient K approaching to 2 can be set to produce an

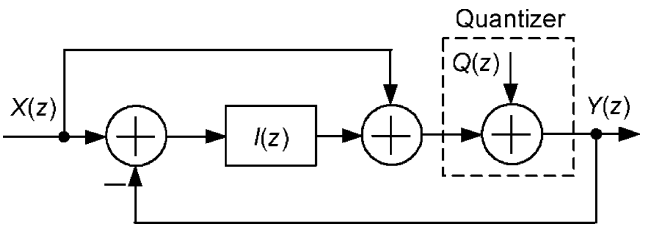

Fig. 6 A modulator with unity STF

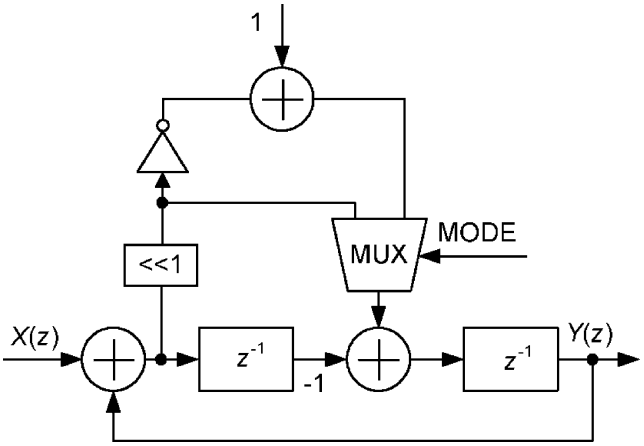

Fig. 7 The proposed reconfigurable integrator

oscillating signal with a frequency much lower than the clock frequency by observing Fig. 4. K_c can be set equal to 2 and K_f equal to a small number to set coefficient K approaching to 2. Letting K_c equal to 2 can replace the multiplier by just a simple shift to further reduce circuit complexity. Furthermore, setting the coefficient K_f equal to a small number, not only fine-tunes the oscillation frequency, but also reduces the injected quantization noise generated from the ΣΔ modulator inserted at the oscillator output.

The coefficient K is conventionally selected to approximate zero to produce an oscillating signal with a frequency approximate to a quarter of the clock frequency ($f_{CLK}/4$) [13–15]. In these works, a high-order ΣΔ modulator is necessary to repress the out-of-band noise if a low-pass type ΣΔ modulator is employed. In order to moderate difficult realization of a high-order low-pass ΣΔ modulator, a band-pass ΣΔ modulator was usually used [13–15]. In addition, a band-limited modulator is commonly used to make the noise transfer function (NTF) zeros in different locations to produce a flat and wider signal band to moderate difficult design of the analog smoothing filter.

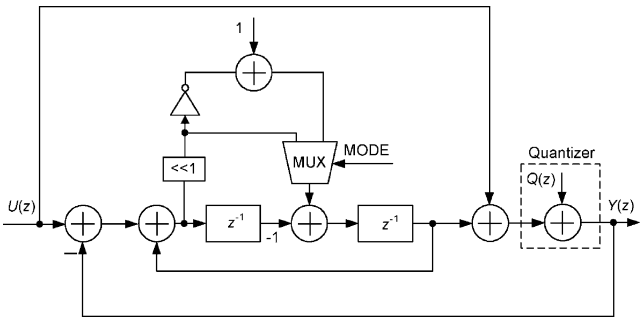

Fig. 8 The reconfigurable ΣΔ modulator with unity STF

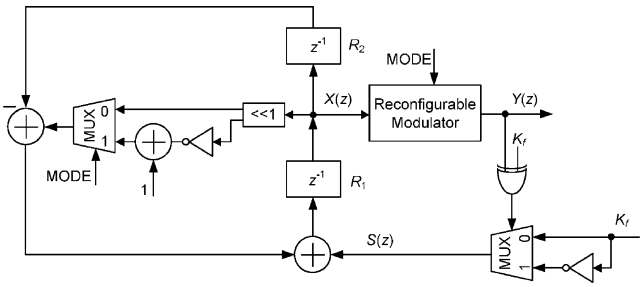

Fig. 9 The oscillator-based reconfigurable sinusoidal signal generator

To achieve better noise immunity, the minimum order of the band-limited modulator is four or higher [14–16]. To generate a higher frequency sinusoidal signal, instead of choosing K_c to zero, the coefficient K_c is set to −2 to produce an oscillating signal with a frequency approximate to half clock frequency, $f_{CLK}/2$ as shown in Fig. 4. By this selection, the coefficient K_c is either 2 in low frequency mode or −2 in high frequency mode. The multiplier of 2 can be simplified by only shift operation, and the multiplier of −2 can be realized by simple logic circuit because the shift operation in low frequency mode is performed. As a result, the oscillator can generate signal frequency up to half clock frequency, $f_{CLK}/2$, with acceptable extra overhead. Also, coefficient K_f is selected to a small number to not only fine-tune oscillation frequency, but also reduce injected quantization noise generated from the ΣΔ modulator inserted at the oscillator output. It is also noteworthy that K_f must be a negative number to prevent the coefficient $K\left(=K_c-K_f\right)$ from becoming smaller than −2. This can be easily achieved by inverting the multiplexer control input, shown in Fig. 5. In summary, the digital oscillator can be reused in two different oscillating modes by switching the coefficient K_c to 2 and −2 and controlling the multiplexer to set the coefficient K_f in either a small positive or negative number.

The modulator signal transfer function (STF) must be unity to design the incorporated ΣΔ modulator, by

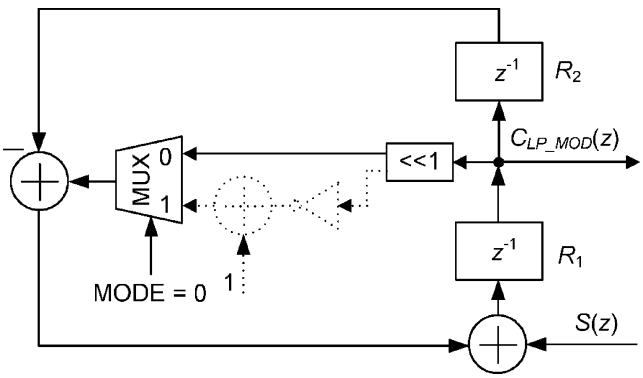

Fig. 10 The modified signal generator for generation of a low-frequency signal

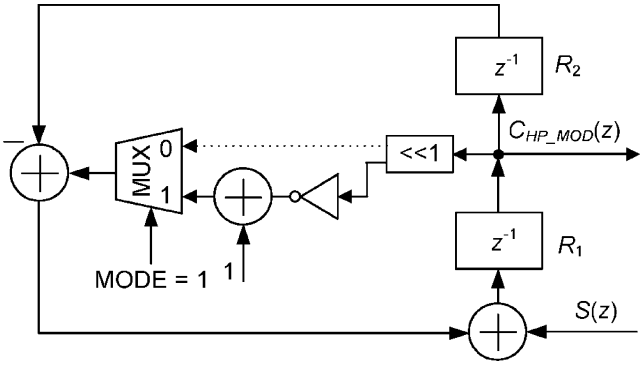

Fig. 11 The modified signal generator for generation of a high-frequency signal

comparing Fig. 5 with Fig. 3. One possible realization for unity STF modulator is shown in Fig. 6 [12].

This structure has the advantage that its STF is independent of the integrated block $I(z)$. The transfer function is expressed in Eq. 6 and $Q(z)$ is the quantization error induced in quantizer.

$$Y(z) = X(z) + Q(z) \cdot [1 + I(z)]^{-1} \tag{6}$$

The NTF depends on the integrated block $I(z)$ and zeros of NTF are equal to the poles of $I(z)$. Therefore, the integrator block function can be changed to realize different NTF.

In this proposed signal generator, the conventional second order low-pass ΣΔ modulator is used for generation of a low frequency stimulus. Consequently, the integrator block used in the second order low-pass ΣΔ modulator is given by Eq. 7 by using the unity STF topology shown in Fig. 6.

$$I(z) = \left(2z^{-1} - z^{-2}\right) \cdot \left(1 - z^{-1}\right)^{-2} \tag{7}$$

For generating a high frequency sinusoidal signal, a second order high-pass ΣΔ modulator [5] is used. A high-pass ΣΔ modulator is based on the same principle as a low-pass one, i.e. the quantization noise is shaped away from the signal band by the loop filter. The only difference is the signal band position, now located at $f_{CLK}/2$ compared with a pass-band at dc for the low-pass ΣΔ modulator. Therefore, NTF zeros are located at half of the sampling frequency, that is $z=-1$, to obtain a higher frequency sinusoidal signal. As a result, the corresponding integrator block used in the second order high-pass ΣΔ modulator is given by

$$I(z) = \left(-2z^{-1} - z^{-2}\right)\left(1 + z^{-1}\right)^{-2} \tag{8}$$

The integrator block for the second order low-pass and high-pass modulators are both composed of two registers, one shift operation, and two adders. And the only difference between the two modulators is the multiplication factor, i.e. 2 or −2. Therefore, the second order low-pass and high-pass modulators can be combined into one and a multiplexer inserted to select the modulator type in different oscillating mode as shown in Fig. 7. A 1-bit control signal (MODE) is used to select the operation model. When MODE=0, the low-pass modulator is selected and a simple shifter is manipulated to perform the "multiplied by 2" computation; while MODE=1, the high-pass modulator is selected and a simple shifter combined with an inverting logic are manipulated to perform the "multiplied by −2" computation.

As a result, a reconfigurable ΣΔ modulator is designed, as shown in Fig. 8, by integrating the reconfigurable integrator (Fig. 7) into the modulator with unity STF (Fig. 6). Furthermore, a reconfigurable ΣΔ modulation based digital oscillator can be realized, as shown in Fig. 9, by integrating the reconfigurable ΣΔ modulator (Fig. 8) into the digital oscillator (Fig. 5). When MODE=0, the low-pass modulator is selected to produce low frequency signal; while MODE=1, the high-pass modulator is selected to produce a high frequency signal. The modulator can, not only be reconfigured itself, but also shares the integrator blocks, and no multiplier is necessary; therefore the total area overhead can be greatly reduced.

Table 1 The coefficients and initial conditions of the oscillator in two modes

Mode	Initial condition	Coefficients
High-frequency signal	$x_1(0) = 2^{-9}$ & $x_2(0) = 0$	$K_f(0) = 2^{-17}$ & $K_f(0) = -2$
Low-frequency signal	$x_1(0) = 2^{-9}$ & $x_2(0) = 0$	$K_f(0) = 2^{-17}$ & $K_f(0) = 2$

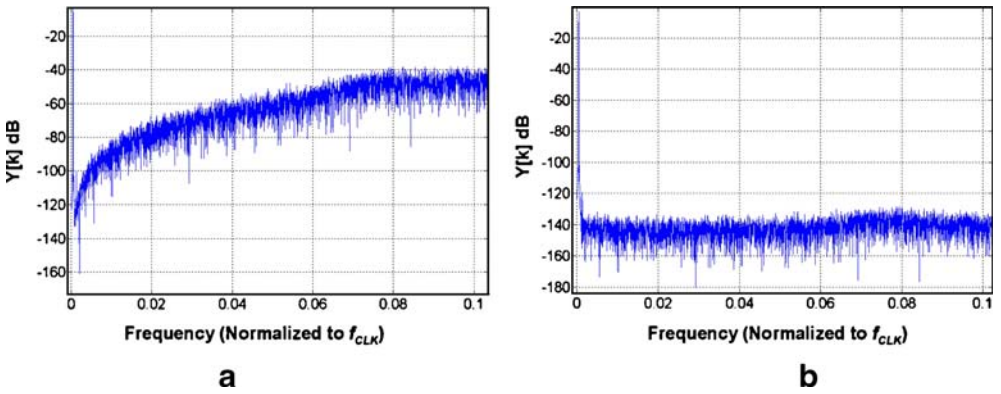

Fig. 12 Spectrums of the **a** output bit stream and **b** reference signal for second order low-pass modulator

3.2 Concurrent Analog and Digital Signal Generation

A reference response is usually necessary as the measured response counterpart for the general ADC BIST methods [1, 8, 13] and a large reference response volume must be previously stored in extra memory and transported to the response analyzer circuit. Hence, more area overhead for the response analyzer circuit, embedded memory, and time for transporting pattern for the BIST process are necessary. Intuitively, an extra digital filter can be inserted to extract the desired signal. However, this will cause more hardware overhead. One of the advantages of this proposed oscillator based sinusoidal signal generator is that not only an on-chip analog test stimuli, but also a digital reference signal without extra overhead can be provided concurrently. The basic idea is to filter out the in-band noise of the ΣΔ modulator's output bit-stream by this oscillator itself. That is the two-register loop in the left-hand side of the oscillator shown in Fig. 9 behaves as a digital filter.

As mentioned previously, MODE=0 is set, and a small value for K_f is selected for generation of a low frequency signal. The multiplexer in the left-hand side of the oscillator will output the shifted value by observing Fig. 10. Therefore, the transfer function of the left-half oscillator is obtained and described as

$$H_{LP}(z) = \frac{C_{LP\_MOD}(z)}{S(z)} = \frac{z^{-1}}{(1-z^{-1})^2} \tag{9}$$

Therefore, the signal inside the bit stream is reconstructed by the left-half oscillator because the transfer function, $H_{LP}(z)$ is a low-pass function and the out-of-band high frequency shaped noise will be filtered out.

Furthermore, MODE=1 is set, and a small negative value for K_f is selected for generation of an oscillating frequency around half of the clock frequency. The left-half oscillator multiplexer will block the shifted value by observing Fig. 11. Therefore, the left-half oscillator transfer function is obtained as

$$H_{HP}(z) = \frac{C_{HP\_MOD}(z)}{S(z)} = \frac{z^{-1}}{(1+z^{-1})^2} \tag{10}$$

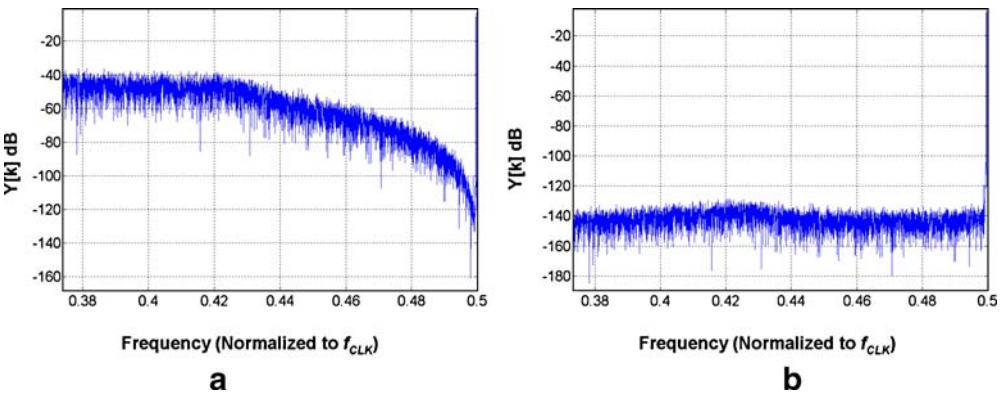

Fig. 13 Spectrums of the **a** output bit stream and **b** reference signal for second order high-pass modulator

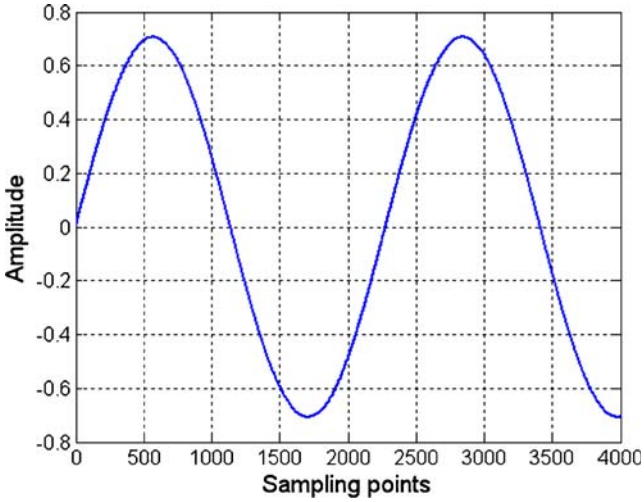

Fig. 14 The time domain wave of the low-pass reference signal

Likewise, the signal inside the bit stream is reconstructed by the left-half oscillator because the transfer function, $H_{HP}(z)$ is a high-pass function and the out-of-band low frequency shaped noise will be filtered out.

As a result, it is concluded that no matter the operating mode and modulator type, both stimuli and reference signal are obtained concurrently without any extra overhead. Therefore, the generated signals can serve as test stimuli applied to ADCs BIST directly and the reference patterns will behave in response analyzer to compare with the ADC digital output codes.

3.3 Resolution of Device and Accuracy of Stimulus

In general, the linearity of signal source must be more accurate than the device under test (DUT) to ensure the test result [6]. Therefore, the accuracy of stimulus, resolution of device, and test accuracy are also related. Generally speaking, the common desired design target is to make linearity errors of DUT are smaller than 0.5 least significant bit (LSB). The value 0.5 LSB is often defined as a reference specification (*RS*). Then the required accuracy of stimulus is therefore expressed in Eq. 11.

$$N_s|_{RS=0.5LSB} = \log_2\left[\frac{1}{(0.5/2^N)}\right] = N+1 \tag{11}$$

When a test procedure for a N-bit ADC would provide test accuracy within x% ($0 < x < 100$) of the device's reference specification, the accuracy of stimulus, N_s, is therefore suggested to be accurate to

$$N_s|_{RS=0.5LSB} = N + 7.64 - \log_2 x \tag{12}$$

Better test accuracy (small x) and larger DUT resolution (larger N) is therefore related to a larger requirement of accuracy for the test stimulus.

In the view of system, the front-end anti-aliasing filter used to filter out the unwanted signal component in conversion process will be helpful to moderate the requirements of analog filter. Furthermore, test accuracy is also related to the requirement of stimulus. If only an approximately characterization of device's functionality is necessary, the requirements of analog filter is also moderated. Therefore, test accuracy is also a consideration in selection of analog filter. In addition, to apply stimuli have difference frequencies can evaluate ADC's performance fully. And the purpose of this work is therefore to propose a sinusoidal signal generator to provide stimuli with different frequency ranges (DC and AC) and make ADC's complete character-

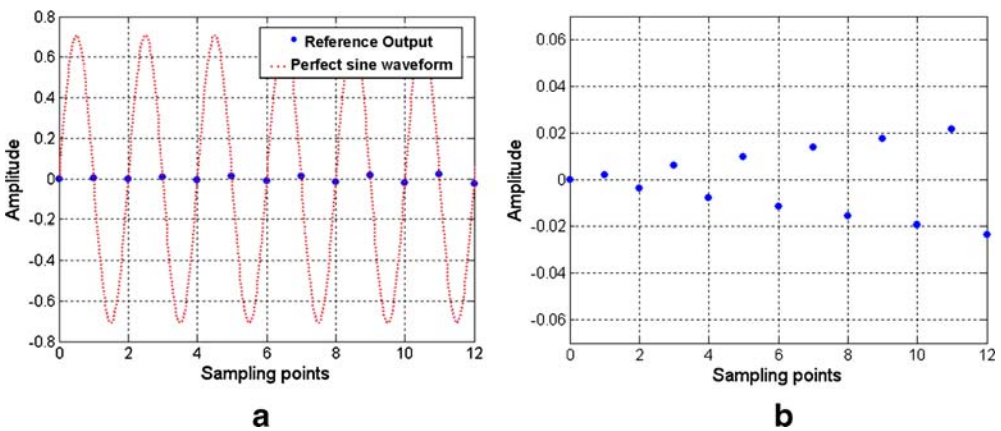

Fig. 15 **a** The time domain wave of the high-frequency reference signal. **b** The close-up view for the wave of the high-frequency reference signal

Table 2 Relationships between the specifications of analog filters and SNDR of stimuli

Filter type	Filter order	SNDR of stimulus (dB)
Low pass	4	62.9
High pass	8	62.6

ization possible. Therefore, two types of analog filter are necessary when ADC's performances to two different stimuli frequencies are concerned by using the proposed method and conventional single modulator based method. And the overhead of analog filter is the same compared to the conventional single modulator based method. But the cost of modulators can be reduced as mentioned in Section 3. A by using the proposed method.

4 Simulation Results

The proposed oscillator-based reconfigurable sinusoidal signal generator is designed and synthesized by 1P6M 0.18-μm CMOS technology. In addition, the design was also put in the ARM development platform to verify the proposed architecture functionality. The coefficients and initial conditions used in two different modes are listed in Table 1. It is readily to calculate that f_{OSC_H} and f_{OSC_L} are about 0.5 f_{CLK} and $4.4\times10^{-4}f_{CLK}$ respectively. In addition, the oscillating signal amplitudes for both modes are selected to approximate 0.7. The outputs of the oscillator based sinusoidal signal generator are performed by 64K FFT in both modes to estimate the signal qualities and shown in Figs. 12 and 13, respectively.

Findings show that the noise is shaped to a higher frequency band in low frequency mode, while the noise is shaped to a low frequency band in high frequency mode. It can also be observed that the oscillator indeed performs the low-pass and high-pass function itself in the two different modes. The SNDR of the extracted low- and high-frequency digital reference signal are 91.3 dB and 91.1 dB respectively. As is known, the coherent frequency f_c is determined in Eq. 13 where M is an integer referred to as the Fourier spectral bins and the number of samples is N under the sampling frequency is f_{CLK} [3].

$$f_c = M\frac{f_{CLK}}{N} \tag{13}$$

In addition, to complete one unit test period, the number of samples is obtained by

$$N\_\text{period} = \frac{f_{CLK}}{f_{OSC}} \tag{14}$$

When the signal generator is operated in low frequency mode, it is expected that the value of M will be much smaller compared to N from Eq. 13. In other words, the value of M is about half of N in the high frequency model. According to Eq. 14 and the set up in Table 1, there will be about 2,272 sample points to complete a unit test period in low frequency mode, and about two sample points to complete a unit test period in high frequency mode. The time domain description of low pass mode is shown in Fig. 14, and it is obvious that there are about 2,272 samples to complete the unit test period. In Fig. 15, observation shows two sample points in one period and a close-up view distinguishes that the sample points are indeed different in high frequency mode. Consequently, the reference signal is obtained without any extra area overhead.

Because the reused modulator will be operated as a low or high pass modulator, analog low and high pass filter are used to extract the oscillating signal information in both modes. The relationships between analog filter and stimuli

Table 3 Performance comparisons of the proposed oscillator-based sinusoidal signal generator and [4, 5, 7]

		This work	[4]	[5]	[7]	
Modulator type		Low + high-pass	Low-pass	Band-pass	Low + band-pass	
Order	High frequency mode	2	2	4	4	8
	Low frequency mode				2	2
Number of gate counts		4,080	n.a.	n.a.	6,517	13,359
Maximum clock frequency (MHz)		78 MHz	3.072	1	72	52
Maximum oscillating frequency		39 MHz	5 kHz	255 kHz	18 MHz	13 MHz

specifications are listed in Table 2. Chebyshev approximation was used to reduce the required filter order [2, 10, 11] .

The comparisons of synthesis results between the proposed structure and previous work are listed in Table 3. The total gate count numbers and maximum clock frequency can be found. The total gate count number is found to be 4,080 and the maximum clock frequency approaches to 78 MHz in the proposed oscillator based signal generator. The maximum clock frequency indicates that the maximum oscillating frequency approached to 39 MHz in high frequency mode. Compared to the fourth order band-pass modulator based signal generator with a pass band of about $0.01f_{CLK}$, the proposed structure saves about 35% of area overhead for the oscillator, and the maximum oscillating frequency improves about two times. Furthermore, compared to the band-pass eighth order modulator based signal generator with a pass band of about $0.02f_{CLK}$, the proposed structure saves about 65% of area overhead for the oscillator and the maximum oscillating frequency improves about triple times [15]. The oscillating frequency of the single low-pass modulator based oscillator [9] is the least among these works because the zero of NTF is near DC. And the oscillating frequency and the zero of NTF of the single band-pass modulator based oscillator are about one quarter of the clock frequency by its nature [16]. Obviously, the maximum oscillating frequency of the proposed oscillator is about half of the clock frequency.

In addition, simulations were done to demonstrate the utilization of this stimulus in ADC testing. An 8-bit ADC has different nonlinearity errors are modeled. The specified nonlinearity errors are identically distributed normal random variables and ±0.5 LSB indicates the nonlinearity errors are within ±0.5 LSB with 99.7% probability. And the desired test accuracy x and the reference specification is 50 and 0.5 LSB, respectively. Therefore, the accuracy of stimulus is therefore approximated to 10 bit from Eq. 12.

Table 4 INL errors

Types of stimulus and reference patterns		Types of stimulus and reference patterns	
Low frequency		High frequency	
INL error	Extracted INL error	INL error	Extracted INL error
0 LSB	−0.046~0.049 LSB	0 LSB	−0.080~0.083 LSB
−0.5~0.5 LSB	−0.556~0.554 LSB	−0.5~0.5 LSB	−0.584~0.588 LSB
−1.0~1.0 LSB	−1.064~1.070 LSB	−1.0~1.0 LSB	−1.093~1.097 LSB

Table 5 DNL errors

Types of stimulus and reference patterns		Types of stimulus and reference patterns	
Low frequency		High frequency	
DNL error	Extracted DNL error	DNL error	Extracted DNL error
0 LSB	−0.039~0.038 LSB	0 LSB	−0.074~0.075 LSB
−0.5~0.5 LSB	−0.545~0.546 LSB	−0.5~0.5 LSB	−0.575~0.577 LSB
−1.0~1.0 LSB	−1.057~1.061 LSB	−1.0~1.0 LSB	−1.080~1.082 LSB

The simulated nonlinearity errors, DNL and INL, are obtained by using sine-wave histogram method [3] and listed in Tables 4 and 5. The extracted nonlinearity errors are close to the modeled ones. The estimated error is sourced from the finite accuracies of the generated stimuli and reference patterns.

5 Conclusion

An oscillator-based reconfigurable sinusoidal signal generator, which can produce high and low frequency signals by switching the oscillator into different modes, was proposed in this paper. Except for a 1-bit DAC and analog filter, the circuits are entirely constructed by digital circuits, and the tuning coefficient used in the circuit is easy to realize in VLSI technology. In addition, the generated signal has precise mathematic definition. The circuit is flexible because the oscillating signal can be controlled precisely to support different stimuli in BIST methodology. The analog stimuli and digital reference signal can also be generated concurrently in both modes without extra overhead. Therefore, the signals can serve in BIST front-end methodology to provide test stimuli and reference codes for ADC testing. The generated stimuli and reference codes can be applied to ADCs to obtain the dynamic and static parameters, respectively.

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Hsin-Wen Ting received the B.S. and M.S. degrees in Electrical Engineering from the National Cheng-Kung University (NCKU), Tainan, Taiwan, in 2002 and 2004, respectively. He is currently working towards his Ph.D. degree at NCKU. His research interests include integrated circuit design and design for testability for analog and mixed-signal circuits.

Cheng-Wu Lin received the M.S. degrees in Electronic Engineering from National Cheng-Kung University (NCKU), Tainan, Taiwan, in 2006. He is currently working towards his Ph.D. degree at NCKU. His research interests include integrated circuit design and design automation for analog and mixed-signal circuits.

Bin-Da Liu received the B. S., M. S., and Ph.D. degrees all in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1973, 1975, and 1983, respectively. From 1975 to 1977, he served as Electrical Officer in the Combined Service Forces. Since 1977 he has been on the faculty of the National Cheng Kung University, where he is currently Distinguished Professor in the Department of Electrical Engineering and Director of the SoC Research Center. He has published more than 240 technical papers. He also contributed chapters in the book *Neural Networks and Systolic Array Design* (D. Zhang Ed. Singapore: World Scientific Publisher, 2002), the book *Accuracy Improvements in Linguistic Fuzzy Modeling* (J. Casillas, O. Cordón, F. Herrera, and L. Magdalena Eds. Heidelberg, Germany: Springer-Verlag, 2003) and the book *VLSI Handbook*, second edition (W. K. Chen Ed. Boca Raton, FL: CRC Press, 2006). His current research interests include low power circuits, neural network circuits, sensory and biomedical circuits, and VLSI implementation of fuzzy/neural circuits and audio/video signal processors.

Dr. Liu is a member on the Board of Governors of Taiwan IC Design Society and a member of Phi Tau Phi, Taiwan SOC Consortium, International Union of Radio Science, Chinese Fuzzy Systems Association, Chinese Institute of Electrical Engineering (CIEE), and the Institute of Electronics, Information and Communication Engineers (IEICE). He was Vice President of Region 10 of the IEEE Circuits and Systems Society during 2005–2006, a CAS Associate Editor for the *IEEE Circuits and Devices Magazine* during 2003–2005, and an Associate Editor for the *IEEE Transactions on Circuits and Systems I: Regular Papers* during 2004–2005. He received many awards, including the Low Power Design Contest Award from the ACM/IEEE in 2003, Outstanding Electrical Engineering Professor Award from the CIEE in 2004, and best paper award from the 2006 IEEE Asia Pacific Conference on Circuits and Systems. He is currently serving as an Associate Editor for *the IEEE Transactions on Biomedical Circuits and System, the IEEE Transactions on Fuzzy Systems*, and *the IEEE Transactions on Very Large Scale Integration (VLSI) Systems.* He is a Fellow of the IEEE.

Soon-Jyh Chang received BS degree in electrical engineering from National Central University, Taiwan, in 1991. He obtained his M.S. and Ph.D. degrees in Electronic Engineering from National Chiao-Tung University, Taiwan, in 1996 and 2002 respectively. Presently, he is an assistant professor of Electrical Engineering at National Cheng-Kung University in Taiwan. His research interests including design and testing for analog and mixed-signal circuits.