# Short Paper

## Structure-Based Specification-Constrained Test Frequency Generation for Linear Analog Circuits

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In this paper, an approach to generating the sinusoidal stimulus of the right frequency of a linear analog circuit for testing circuit parameter faults under the constraints of the specifications of the circuit under test (CUT) is presented. This approach considers tolerance bounds due to fabrication process fluctuations of tested parameters using a statistical model and maps them to an accepted region of the observed signature of the CUT. The generated test stimulus is derived based on a proposed testing confidence level. Test generation procedures for both the monotonic and non-monotonic relationships between the signature and the parameter are proposed and demonstrated. The procedures are applied to a continuous time state-variable filter example circuit to show the effectiveness of the methodology.

***Keywords:*** test pattern generation, analog IC test, structural test, specification test, Monte-Carlo analysis

### 1. INTRODUCTION

Test pattern generation for analog circuits is a difficult task due to the wide variety of circuits, the non-deterministic nature of circuit parameters and the limited controllability and/or observability [1]. There are two basic approaches to test pattern generation for analog circuits, i.e., the functional-driven approach and the structure-based approach. In the functional-driven approach, test patterns are generated to exploit the difference in performance of the normal and faulty circuits [2-4]. However, this approach lacks clear metrics for evaluating the effectiveness of the generated test inputs at the functional level. In the structure-based approach, a fault model, usually at the circuit level, is adopted, and

Received October 3, 2001; revised April 12 & July 15, 2002; accepted September 4, 2002.
Communicated by Cheng-Wen Wu.

test patterns (signals) are generated to exploit the observed signature difference between the normal and faulty circuits. It is natural to generate test stimuli by maximizing the observed signature difference between the good and defective circuits [5-7]. This approach usually is efficient for catastrophic faults. Howevr, it is not necessarily efficient for soft faults because the difference between the faulty response and the normal response may not be a monotonous function of the deviating component value. In addition, testability transfer factors have been introduced to aid the construction of efficient dynamic test sets [8], and the sensitivity of circuit components to test parameters has been adopted to generate efficient tests for single and multiple faults [9, 10]. There are also approaches that correlate specifications to non-specification tests for analog circuits [11-13]. In these approaches, the bounds of the tolerance region for each parameter of the CUT can be evaluated under the single fault assumption. However, uncertain regions exist when these bounds are mapped to the observed signatures, especially when the relationship between the observed signature and parameter variation is non-monotonic. It is hard to identify whether a CUT passes or fails the test if the measured performance falls into an uncertain region.

This paper proposes a test frequency generation method which correlates circuit parameters to circuit specifications and considers fluctuation in the manufacturing process. And then, it generates tests based on a predefined testing confidence level. This method can eliminate the uncertainties encountered in [11-13] and provide test frequencies which can be used to more effectively test the circuit.

The paper is organized as follows: The process of correlating analog faults with specifications is presented first. Then, in section 2, we present Monte Carlo simulation conducted to find the effect of the manufacturing process fluctuation on the above relation and describe a procedure for deriving parameter tolerance ranges under a predefined testing confidence level. Section 3 describes the test generation procedure that maps the parameters to the observed signatures. An illustrative case study on the continuous-time state-variable filter benchmark circuit [14] is presented in section 4 to demonstrate the effectiveness of the approach. Section 5 concludes the paper.

## 2. MAPPING SPECIFICATIONS TO CIRCUIT PARAMETERS

The test pattern generation problem dealt with in this paper is stated as follows: Given the netlist and specifications of a CUT under a specified level of manufacturing process fluctuation, the problem is to generate the efficient test frequency for each circuit parameter (resistance, capacitance, W/L etc.) under a desired testing confidence level and to derive the corresponding tolerance range for the observed signature. When the CUT passes the tests, which are derived for each circuit parameter, all the circuit specifications are implicitly met.

Consider a circuit of $\boldsymbol{m}$ parameters, $\boldsymbol{P} = [p_1, p_2, \ldots, p_m]$, where $p_i$ may be the resistance of a resistor, the capacitance of a capacitor, the $W/L$ ratio of a transistor, the $V_T$ value of a transistor etc. The performance of the circuit is bounded by $\boldsymbol{n}$ specifications, $\boldsymbol{S} = [s_1, s_2, \ldots, s_n]$, for which $\boldsymbol{S^u} = [s_1^u, s_2^u, \ldots, s_n^u]$ and $\boldsymbol{S^l} = [s_1^l, s_2^l, \ldots, s_n^l]$ denote the upper and lower bounds for these specifications, respectively. The circuit is designed with its parameters at the nominal $\boldsymbol{P}$ values: $\boldsymbol{P^0} = [p_1^0, p_2^0, \ldots, p_m^0]$. Correspondingly, it has a target performance, $\boldsymbol{S^0} = [s_1^0, s_2^0, \ldots, s_n^0]$.

A specification, for example the $j$-th specification ($s_j$), can be represented as a function of all parameters, i.e.,

$$s_j = f(p_1, p_2, \ldots\ldots, p_m). \tag{1a}$$

Under the single fault assumption, for example the $i$-th parameter ($p_i$) deviation fault, all the parameters in Eq. (1a) are fixed to their nominal values except $p_i$, which is allowed to vary. Hence, $s_j$ can be represented as a function of $p_i$, denoted as $s_j(p_i)$, that is,

$$s_j(p_i) = f(p_1^0, p_2^0, \ldots, p_{i-1}^0, p_i, p_{i+1}^0, \ldots, p_m^0). \tag{1b}$$

For a fault free circuit, i.e., the $i$-th parameters ($p_i$) equal to its nominal value ($p_i^0$), the value of the $j$-th specification equals $s_j(p_i^0)$, while for a faulty circuit with $p_i$ deviating to a value $K$, $s_j$ shifts to $s_j(K)$. $s_j$ can be obtained, easily if Eq. (1b) is simple and explicit, or with more difficulty via simulation if Eq. (1b) is non-explicit and complicated.

Considering the variations in the parameter space due to fluctuation in the process, there will correspondingly be variation in the specification space of the circuit. The relationships between the specification and the parameter will become a band instead of a single curve [16]. If the variations of all the parameters are assumed to be random with a normal distribution, the corresponding distribution of specifications will also be Gaussian [15]. Generally, specification $s_j$ has a distribution, due to the process fluctuation, with respect to parameter $p_i$, denoted as $s_j(x, p_i)$, such as follows:

$$S_j(x, p_i) = \frac{1}{\sqrt{2\pi}\sigma_j(p_i)} e^{\frac{-(x-\mu_j(p_i))^2}{2\sigma_j^2(p_i)}}, \tag{2}$$

where $x$ is the value of specification $s_j$, $\mu_j$ is the mean value and $\sigma_j^2$ is the variance of specification $s_j$. If there is a fault on $p_i$, i.e., $p_i = K$, then $s_j$ will have a new distribution with a new mean value ($\mu$) and new variance ($\sigma^2$), which can be obtained through Monte Carlo simulation and statistical analysis.

For a fault-free circuit whose specification $s_j$ is bounded by $s_j^u$ and $s_j^l$, the circuit passes a specification test if $s_j^l \le s_j \le s_j^u$ under a specified test input. However, theoretically, there is a very small probability that the circuit may not pass the specification test due to the fact that $s_j$ is a distribution, which is caused by variation in the values of all the other parameters due to the process fluctuation even though $p_i$ is at its normal value. As the parameter $p_i$ deviates from its nominal value to the faulty value, the probability of the CUT passing specification $s_j$ decreases. The probability that the circuit will pass $s_j$ when $p_i$ deviates to the faulty value $K$ is

$$Prob(p_i = K \xrightarrow{pass} s_j) = \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{s_j^l}^{s_j^u} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx. \tag{3}$$

In addition, the probability that the CUT will fail $s_j$ when $p_i$ deviates to the faulty value $K$ is

$$Prob(p_i = K \xrightarrow{fail} s_j) = \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{-\infty}^{s_j^l} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx + \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{s_j^u}^{\infty} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx. \tag{4}$$

Naturally,

$$Prob(p_i = K \xrightarrow{pass} s_j) + Prob(p_i = K \xrightarrow{fail} s_j) = 1. \tag{5}$$

Hence, theoretically, according to the above analysis, for a CUT, even when it passes all specification tests, it still has a certain possibility, although small, of failing to work normally. Here, the term "**testing confidence** (***TC***)" is introduced. It is the probability that a CUT, when passing a test, will work normally.

The bounds of the ranges of "accept" or "reject" for a circuit to pass specification $s_j$ for $p_i$ can be obtained by solving Eq. (3) under a given testing confidence level:

$$TC = \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{s_j^l}^{s_j^u} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx. \tag{6}$$

For example, if *TC* is 90%, four bounds, denoted as $BP1_{ij}$, $BP2_{ij}$, $BF1_{ij}$, and $BF2_{ij}$, respectively, solved for parameter $p_i$ to pass or fail $s_j$ [16]. The circuit will pass $s_j$ with over 90% probability when $p_i$ is between $BP1_{ij}$ and $BP2_{ij}$, and will fail, with over 90% probability, if $p_i$ is below $BF1_{ij}$ or over $BF2_{ij}$. Within the two gray regions, i.e., $BF1_{ij}$ to $BP1_{ij}$ and $BP2_{ij}$ to $BF2_{ij}$, the circuit cannot be determined to be "pass" or "fail" due to random variations caused by process fluctuations of other parameters. If we reduce *TC*, then these two regions will shrink. For example, if we only require a *TC* of 50%, then these two regions will shrink to zero.

When a circuit is fault-free, it satisfies "all" specifications. As a result, the bounds of the "accept" range for $p_i$ are given by

$$BP1_i = maximum(BP1_{i1}, BP1_{i2}, \dots, BP1_{in}), \tag{7a}$$

$$BP2_i = minimum(BP2_{i1}, BP_{i2}, \dots, BP2_{in}). \tag{7b}$$

On the other hand, a circuit is considered to be faulty if it violates one of the specifications. Hence, the bounds of the "reject" range for $p_i$ are

$$BF1_i = maximum(BF1_{i1}, BF1_{i2}, \dots, BF1_{in}), \tag{8a}$$

$$BF2_i = minimum(BF2_{i1}, BF2_{i2}, \dots, BF2_{in}). \tag{8b}$$

In summary, in the above, we have demonstrated how the tolerance bound of a parameter can be derived, starting from the constraints of specifications under a desired level of testing confidence. We have shown that tolerance bounds depend on a given level of testing confidence.

## 3. TEST GENERATION PROCESS

In this section, we will illustrate how to generate the test stimulus and the corresponding tolerance ranges of an observed signature while considering the "accept" tolerance ranges, which are obtained as described in the previous section.

The relationships between signatures and parameters fall into two categories: monotonic and non-monotonic. Different test strategies are proposed to generate test stimuli for these two categories:

### 3.1 Test Generation under the Monotonic Signature – Parameter Relationship

When a monotonic relationship exists between a signature and a parameter, the signature is an either monotonic increasing (as shown in Fig. 1) or decreasing function of the parameter. In this case, it is easy to determine the pass/fail range of the observed signature by mapping the pass/fail tolerance bounds of the parameter axis onto the parameter axis via the relationship curve. There are two uncertain regions on the signature axis, resulting from the uncertain regions on the parameter axis. As discussed in the previous section, if we require for a 50% *TC*, these two uncertain ranges will shrink to zero.

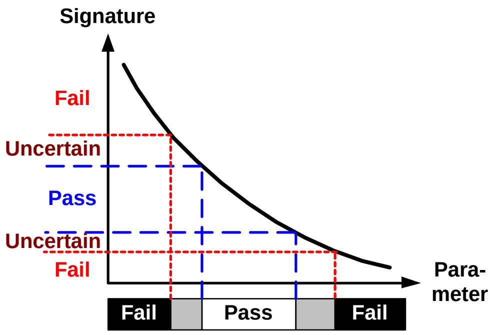



Fig. 1. Tolerance range for a monotonic relationship between a signature and a parameter.

Now, the problem of test generation is to generate the test stimulus that can best distinguish the fault effect. The sensitivity-based method [9, 10] generates test stimuli based on the maximum sensitivity of the signature with respect to the parameter, for which there is a fault to be tested. However, as the following example shows, consideration of only sensitivity is not adequate for selecting the optimum input test stimulus.

Fig. 2 shows a simple low pass filter, where (a) is the circuit diagram. The transfer function of this low pass filter is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-R_2/R_1}{1+sCR_2}. \tag{9}$$

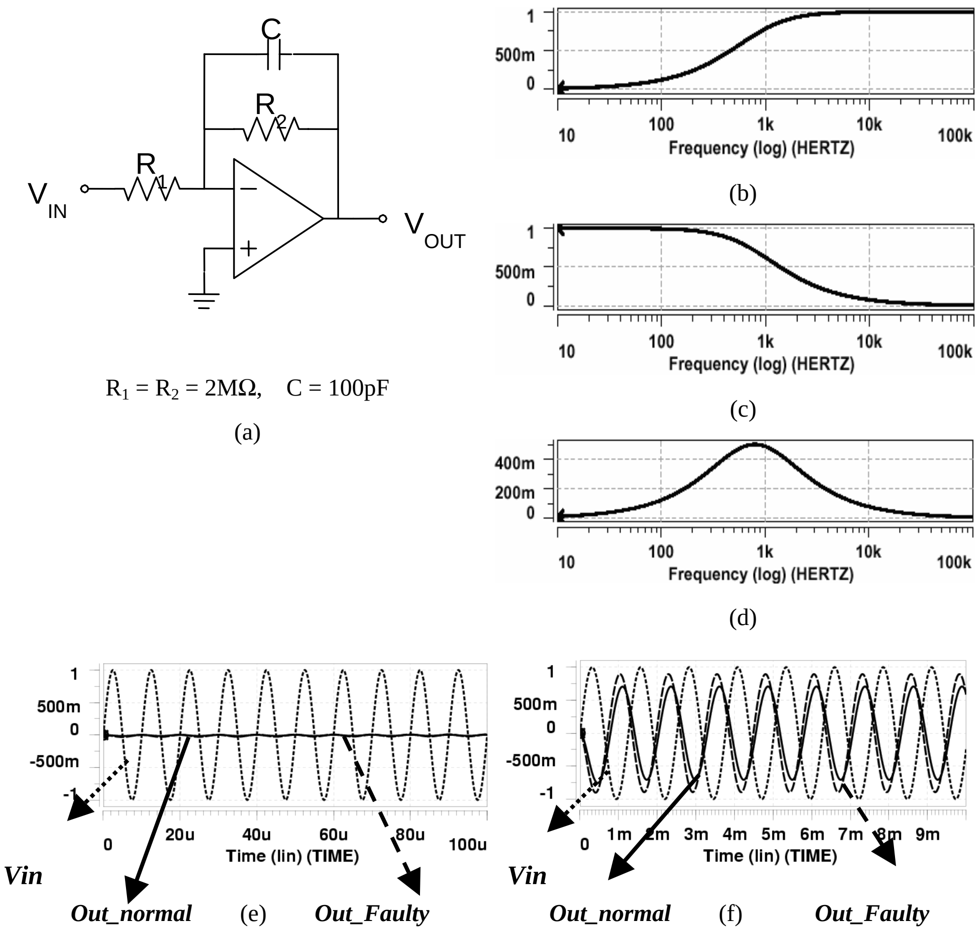



Fig. 2. (a) A low pass filter circuit example; (b) the sensitivity of voltage gain w.r.t. frequency; (c) its a.c. input-output transfer function; and (d) its signature observability curve; (e) the output response for a 100KHz, 1-volt sinusoidal input, which is chosen by only considering the maximum sensitivity; (f) the output response for a 796, 1-volt sinusoidal input, which is chosen by considering the maximum signature observability.

It is assumed that the observed signature is the amplitude of the output signal with a 1-volt sinusoidal signal applied at the input with a variable frequency, and that the parameter to be tested is capacitor *C*. By definition, the sensitivity of the observed signature, i.e., the amplitude of the output, *y*, w.r.t. the parameter *C*, is

$$\left|S_C^y\right| = \left|\frac{\partial y / y}{\partial C / C}\right| = \left|\frac{-j(2\times 10^{-4})\times 2\pi f}{1 + j(2\times 10^{-4})\times 2\pi f}\right|. \tag{10}$$

Fig. 2(b) shows the curve of Eq. (10). According to this figure, a signal with a high frequency is better for testing the fault. However, when we consider the input-output transfer factor, which is shown in Fig. 2(c), we find that the output amplitude is nearly zero for this circuit if a high frequency signal is chosen as the test signal. That is, it is not sufficient for selecting the test signal if only sensitivity is considered! Hence, to generate the optimum input stimulus, we define "***signature observability"*** in the following.

**Definitions:**

(a) The ***signature sensitivity*** of a parameter $p_i$ for the observed signature $y_j(x)$ is denoted as

$$S_{p_i}^{y_j}(x) = \frac{\partial y_j(x) / y_j(x)}{\partial p_i / p_i}. \tag{11a}$$

(b) The ***input-output transfer factor***, ***IOTF***, is defined as the ratio of the observed signature $y_j(x)$ with respect to input stimulus $In(x)$ and is represented as

$$IOTF_j(x) = \frac{y_j(x)}{In(x)}. \tag{11b}$$

(c) The ***signature observability*** of the observed signature $y_j(x)$ with respect to parameter $p_i$ is defined as the product of the fault sensitivity and the input-output transfer factor, and is denoted as

$$FO_i^j(x) = S_{p_i}^{y_j}(x) \times IOTF_j(x) = \frac{\partial y_j(x)}{\partial p_i} \times \frac{p_i}{In(x)}, \tag{11c}$$

where $x$ is the variable to be decided for the input, e.g., the test frequency of an input with constant amplitude. The optimal $x$ should be the one which maximizes the absolute value of the signature observability. As shown in Fig. 2(d), the test frequency for the capacitor $C$ deviation fault should be the medium frequency: 796 (Hz). For a fault where $C$ = 100 ($p$F) deviates to $C$ = 50 ($p$F), Fig. 2(e) shows the output response for a 1-V, 100K (Hz) sinusoidal input, which is chosen by only considering the maximum sensitivity in Fig. 2(b). The output amplitude is almost zero and hard to observe for both normal and faulty circuits; i.e., the faulty effect can not be observed. On the other hand, the output response for a 1-V, 796 (Hz) sinusoidal input signal, which is chosen by considering the maximum signature observability in Fig. 2(d), is shown in Fig. 2(f). An approximately 187 (mV) difference in the amplitude between the normal and faulty circuit is observed.

### 3.2 Test Generation under the Non-Monotonic Signature-Parameter Relationship

As mentioned previously, the relationships between signatures and parameters are not always monotonic, owning to the diverse nature of analog circuits. Fig. 3 shows a case where an observed signature has a non-monotonic relationship with respect to a parameter. In this case, it is difficult to determine the pass/fail ranges of the observed signature by projecting the "pass/fail" tolerance bounds of the parameter via the relationship curve. For example, as shown in Fig. 3(a), if a value $y_1$ of the signature is observed during testing, it is difficult to determine whether the corresponding target test parameter $p$ is good or not since there are two values, $p_1$ and $p_2$, where $p_1$ is located in the acceptable (pass) region, but $p_2$ is in the region unacceptable (fail) region, corresponding to the observed signature value. In this case, there is an uncertain region on observed signature y. This uncertain region is not caused by the process fluctuation, as described in the last subsection, but results simply from the non-monotonic relationship between the observed signature and the target test parameter.

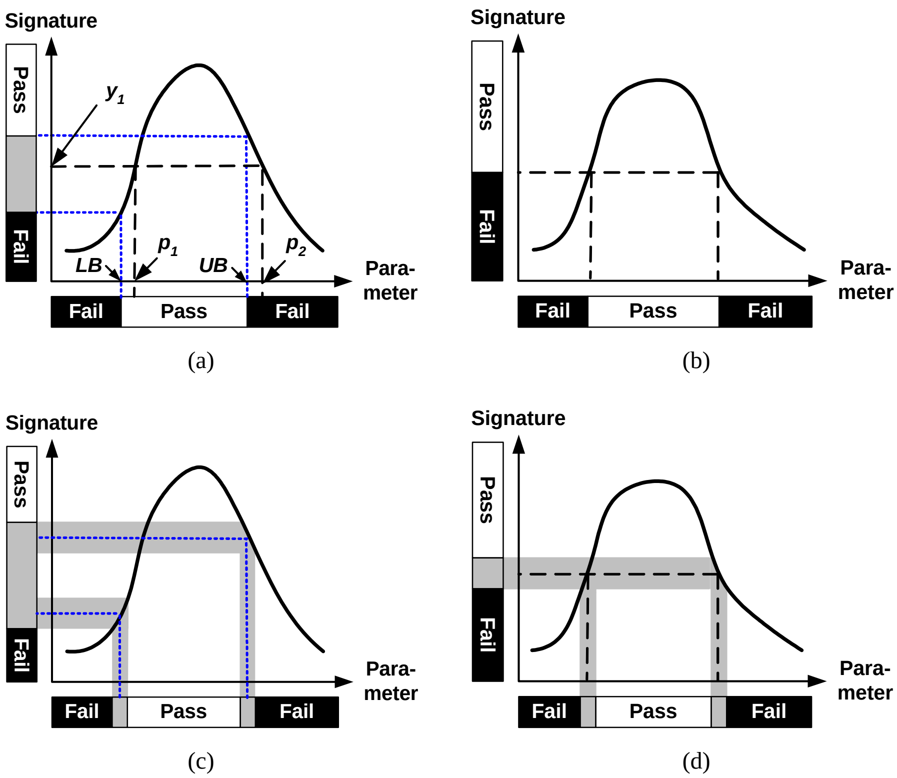



Fig. 3. (a) The non-monotonic relationship between the signature $y$ and the parameter $p$, where $y$ has an uncertain region since the corresponding $p$ has two values: one is in the "pass" region, and, one is in the "fail" region; (b) the uncertain region in $y$ is eliminated if a test stimulus of the generated frequency is applied; (c) the uncertain region of (a) is expanded when the process fluctuation is considered; and (d) the uncertain region due to the process fluctuation that occurs when the generated test stimulus is applied.

Hence, in the non-monotonic specification-parameter case, instead of maximizing the signature observability while finding the test frequency as in the previous monotonic case, it is a good ides to find the test frequency that can eliminate this uncertainty region as shown in Fig. 3(b). This will be explained in the following.

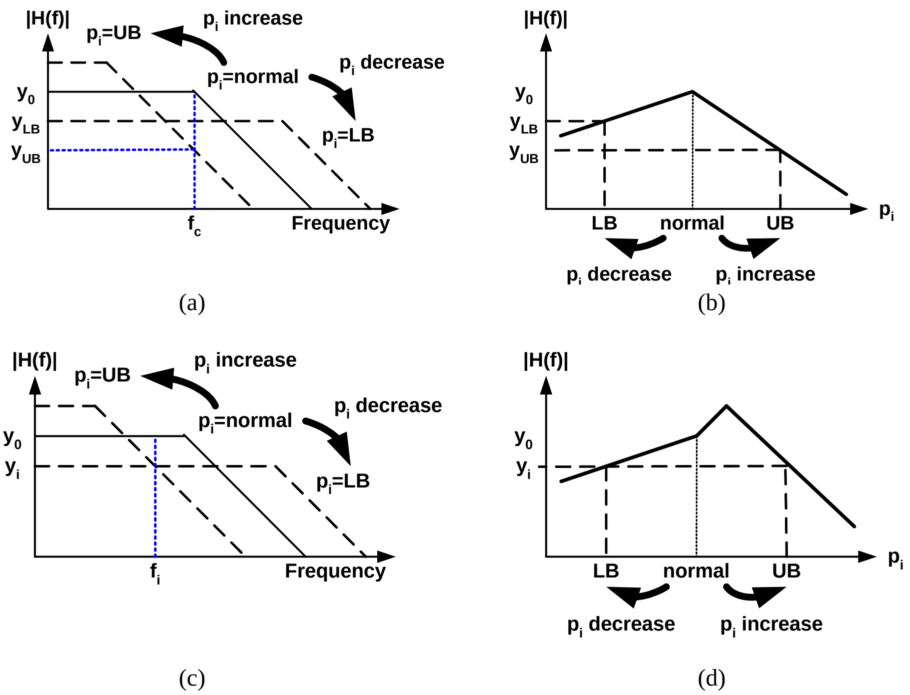



Fig. 4. (a) The a.c. transfer curves of a low pass circuit when the parameter $p_i$ is equal to normal, UB and LB values, respectively, and the cutoff frequency, $f_c$, of the normal transfer curve is chosen as the test frequency; $y_0$, $y_{LB}$, $y_{UB}$ are the low pass transfer gains of the corresponding curves, respectively; (b) the plot of the output voltage (the signature) w.r.t. the parameter $p_i$ when the test frequency $f_c$ is applied as the test stimulus; (c)the same a.c. transfer curves as in (a) but the frequency $f_i$ is chosen as the test frequency; and (d) the plot of the output voltage w.r.t. the parameter $p_i$ when the test frequency $f_i$ is applied.

As shown in Fig. 3(a), the existence of an uncertain region is caused by inequality in the observed signature when the parameter is equal to the upper bound (UB) and lower bound (LB) of the pass region under a given test stimulus. In order to eliminate the uncertain region, we must select a test stimulus which generates a “single value” signature when the parameter is equal to its LB and UB respectively. A low pass circuit will be used to illustrate the approach taken to select the test stimulus of a good test frequency. Fig. 4(a) shows the frequency responses of a circuit when its parameter $p_i$ is equal to the normal, UB, and LB values respectively. For this circuit, if, for example, the cutoff frequency ($f_c$) of the normal circuit is selected as the test frequency shown in Fig. 4(a), then it will have two different output voltages ($y_{LB}$ and $y_{UB}$) when parameter $p_i$ is equal to LB and UB, respectively. Hence, there will be an uncertain voltage range between $y_{LB}$ and $y_{UB}$ as shown in Fig. 4(b), which plots the relationship between the signature $y$ and parameter $p_i$. However, the uncertain region can be eliminated by choosing a test frequency of $f_i$, which will generate a single value voltage output ($y_i$) for both $p_i$ = UB and $p_i$ = LB as shown in Fig. 4(c) along with its corresponding $y$ – $p_i$ relationship as shown in Fig. 4(d).

Mathematically, the test frequency $f$ for parameter $p_i$, denoted as $f_i$, can be obtained by solving

$$y(f)\big|_{p_i=UB} = y(f)\big|_{p_i=LB}. \tag{12a}$$

The pass/fail bounds of the observed signature, $y_i$, will be

$$y_i = y(f_i)\big|_{p_i=UB} = y(f_i)\big|_{p_i=LB}. \tag{12b}$$

The non-monotonic case occurs most often since a circuit designer usually wishes to optimize his design so that the circuit output will degrade on both sides if the parameter value deviates from its designed one.

## 4. EXAMPLE AND SIMULATION RESULTS

In this section, a continuous-time state-variable filter benchmark circuit [14], as shown in Fig. 5, is used to demonstrate the test generation procedure.

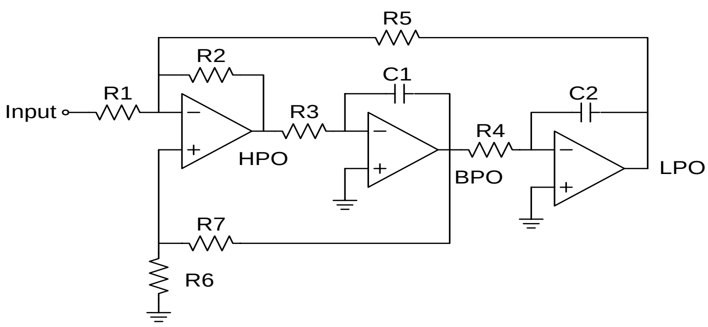



Fig. 5. The circuit of the benchmark continuous-time state-variable filter.

The transfer function of the band-pass output (BPO) of the circuit is given as

$$\frac{V_{BPO}(s)}{V_{in}(s)} = K\frac{\dfrac{s}{R3\cdot C1}}{s^2 + \dfrac{1}{Q\cdot R3\cdot C1}s + \dfrac{K}{R3\cdot C1\cdot R4\cdot C2}}, \tag{13}$$

where $K$ stands for the filter gain and $Q$ represents its quality factor. The following values are taken: R1 = R2 = R3 = R4 = R6 = 1 $M\Omega$, C1 = C2 = 200 $pF$, R6 = 300 $K\Omega$, and R7 = 700 $K\Omega$, and the central frequency for the BPO is 794 (Hz) with a voltage gain equal to 1.11. The operational amplifiers in this circuit are the benchmark operational amplifier of [14]. It is adopted for the purpose of making the study more practical. The specifications of the filter are shown in Table 1.

**Table 1. Specifications of the filter circuit and their nominal values (NV), lower bounds (LB), and upper bounds (UB).**

| Specifications | NV | UB | LB |
|---|---|---|---|
| S1: Gain @ $f_c$ | 1.11 | 1.3 | 1 |
| S2: Central Frequency ($f_c$) | 794 | 900 | 700 |
| S3: Low Cutoff Frequency | 515 | 600 | 400 |
| S4: High Cutoff Frequency | 1231 | 1400 | 1000 |
| S5: 3dB Bandwidth | 716 | 1000 | 500 |
| S6: Quality Factor | 1.11 | 1.3 | 0.9 |
| S7: Gain @ 100Hz | 0.13 | 0.2 | 0 |
| S8: Gain @ 700Hz | 1.07 | ∞ | 0.9 |
| S9: Gain @ 900Hz | 1.07 | ∞ | 0.9 |
| S10: Gain @ 10KHz | 0.08 | 0.2 | 0 |

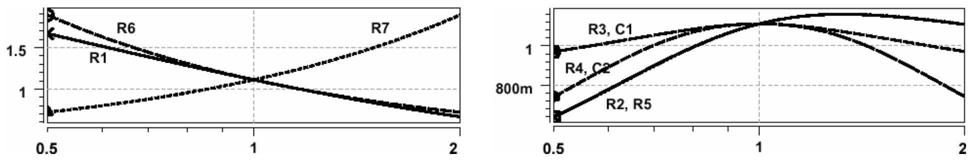
For circuit level faults, the number of parameters (R, C, and W/L and $V_T$ of each transistor) is 66. It can be shown that the variance of each specification caused by the parameters inside the operational amplifiers is much smaller than that caused by the passive components outside the operational amplifiers since the characteristics of the operational amplifier are insensitive to the device parameters inside the operational amplifier due to the negative feedback configuration [16]. Hence, in this study, only the passive components (R1~R7, C1, C2) outside the operational amplifiers were considered.

Through simulation, the bounds of the specifications were mapped to the bounds of the circuit parameters, that is, BF1, BP1, BP2, and BF2, which are shown in Table 2 for 95%, 90% and 50% testing confidence level cases.

**Table 2. Bounds of the "pass" and "fail" ranges of all parameters under 95%, 90% and 50% *TC* (units: *K*Ω for resistors and *pF* for capacitors).**

| Para. | 95% TC | | | | 90% TC | | | | 50% TC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BF1 | BP1 | BP2 | BF2 | BF1 | BP1 | BP2 | BF2 | BF1 | BP1 | BP2 | BF2 |
| R1 | 713 | 858 | 1075 | 1267 | 729 | 841 | 1096 | 1246 | 785 | 785 | 1171 | 1171 |
| R2 | 733 | 903 | 1100 | 1419 | 747 | 868 | 1130 | 1378 | 801 | 801 | 1245 | 1245 |
| R3 | 777 | 905 | 1151 | 1455 | 791 | 891 | 1183 | 1421 | 840 | 840 | 1301 | 1301 |
| R4 | 731 | 880 | 1151 | 1455 | 747 | 862 | 1183 | 1421 | 804 | 804 | 1301 | 1301 |
| R5 | 735 | 900 | 1151 | 1455 | 750 | 868 | 1183 | 1421 | 805 | 805 | 1301 | 1301 |
| R6 | 224 | 269 | 322 | 382 | 227 | 263 | 329 | 375 | 242 | 242 | 351 | 351 |
| R7 | 551 | 662 | 801 | 954 | 561 | 648 | 817 | 935 | 602 | 602 | 873 | 873 |
| C1 | 153 | 182 | 229 | 288 | 157 | 178 | 236 | 280 | 167 | 167 | 257 | 257 |
| C2 | 146 | 174 | 229 | 288 | 149 | 170 | 236 | 280 | 160 | 160 | 257 | 257 |

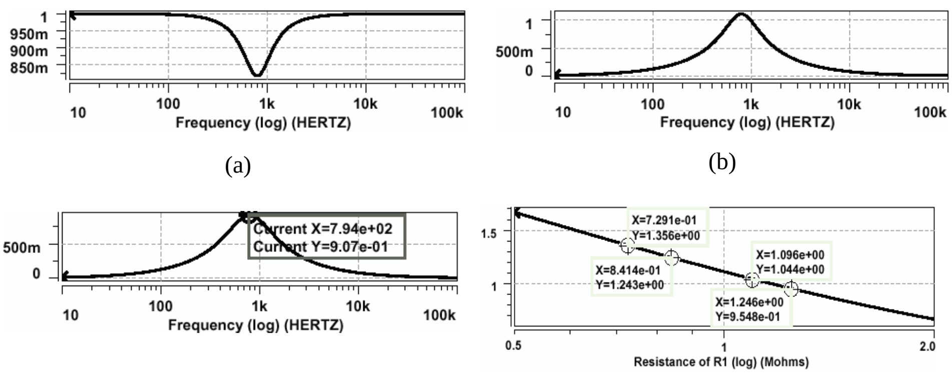
The simulated signatures, i.e., the output of the circuit when a 1-V sinusoidal signal at 794Hz (the central frequency) was applied at the input, are plotted in Fig. 6 for all circuit parameters. The curves are plotted in terms of the values of the parameters in scaling factors from 0.5 to 2.0. It is seen that the signatures w.r.t. R1, R6 and R7 are monotonic, and, those with other parameters are non-monotonic.




(a) (b)

Fig. 6. (a) The simulated signatures-to-be-observed (monotonic) for circuit parameters R1, R6, and R7; and (b) the simulated signatures-to-be-observed (non-monotonic) for all the remaining circuit parameters.

For monotonic relationship parameters R1, R6 and R7, we generated the test frequency for testing them based on the signature observability of Eq. (11). Figs. 7(a), (b) and (c) show the sensitivity, the frequency response and the corresponding signature observability curve of the CUT for R1, respectively, where the test frequency was found to be 794Hz, which is obviously different from the frequencies that have the highest sensitivity. Fig. 7(d) shows the output voltage w.r.t. R1 with the generated 794 (Hz) 1-volt sinusoidal signal applied at the input. The pass/fail ranges of the output voltage were obtained by mapping the computed tolerance bounds of R1, listed in Table 2, onto this curve. For example, given a testing confidence level *TC* = 90%, the tolerance bounds for R1 are BF1 = 0.729(*M*Ω), BP1 = 0.841(*M*Ω), BP2 = 1.096(*M*Ω), and BF2 = 1.246(*M*Ω), and their corresponding signatures are 1.356(V), 1.243(V), 1.044(V), and 0.955(V), respectively. That is, if the observed signature is between 1.044(V) and 1.243(V), R1 is fault-free; if it is larger than 1.356(V) or smaller than 0.955(V), R1 is faulty; otherwise, it is uncertain whether R1 passes or fails the test.




(c) (d)

Fig. 7. (a) The sensitivity curve w.r.t. R1; (b) the frequency response; (c) the signature observability w.r.t. R1; and (d) the signature obtained w.r.t. R1 at the output under the 1 volt, 794 Hz sinusoidal input. "Pass/fail" bounds and tolerance ranges under *TC* =90% are marked.

For the non-monotonic relationship parameters R2~R5, C1 and C2, we generated test frequencies for testing them with the aim of reducing the uncertainty. For example,

Fig. 8(a) shows a.c. transfer curves when R2 is equal to the bounds of the pass/fail range, i.e., 0.801($M\Omega$) and 1.245($M\Omega$), as listed in Table 2 for a given 50% testing confidence level. The intersection point of these two curves implies that BPO has the same voltage gain (1.016) for R2 = 0.801($M\Omega$) and 1.245($M\Omega$) at an input test frequency of 670 (Hz). The relationship curve of the BPO output w.r.t. R2 when a 1-volt, 670 (Hz) sinusoidal signal was applied at the input is shown in Fig. 8(b). The pass/fail range of the observed signature can be obtained by projecting the pass/fail tolerance bounds of R2 through the relationship curve. If the observed signature is larger than 1.016(V), then parameter R2 is in its pass range, and the circuit satisfies all the constraints of the specifications. On the other hand, R2 fails the test if the observed signature is smaller than 1.016(V). Furthermore, if we require a 90% testing confidence level, then the tolerance range of the output amplitude is obtained by projecting the tolerance bounds, 0.747($M\Omega$), 0.868($M\Omega$), 1.13($M\Omega$), and 1.378($M\Omega$), as listed in Table 2, through the relationship curve as shown in Fig. 8(c). If the observed signature is larger than 1.03(V), then parameter R2 is in its pass range and the circuit satisfies all the constraints of the specifications with a *TC* larger than 90%. Similarly, R1 fails the test with a *TC* larger than 90% if the observed signature is smaller than 0.992(V). It is noted again that, the uncertain regions of the signatures between the pass and fail ranges result from the 90% testing confidence level requirement.

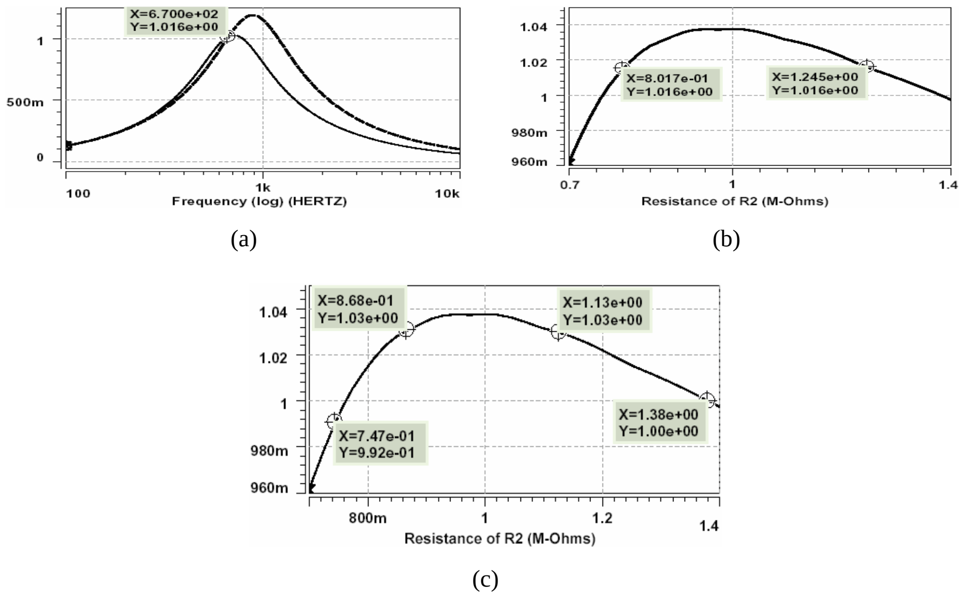



Fig. 8. Test generation for a non- monotonic relationship between the signature (the output voltage under a 1*V* sinusoidal input) and R2; (a) the a.c. transfer curves for R2 equal to 0.801($M\Omega$) and 1.245($M\Omega$); (b) the output voltage w.r.t. R2; and (c) Pass/Fail range determination performed by mapping the tolerance bounds of R2 through the relationship curve for a *TC* = 90%.

## 5. CONCLUSIONS

In this paper, we have presented a structure-based specification-constrained test generation method for analog circuits. The approach starts with derivation of the relationship between the specifications and the device and/or component parameters, and it then considers variations of component parameters due to fabrication process fluctuation by using a statistical model. A testing confidence probability is employed to define upper and lower bounds for the component parameters. The relationship between the observed signature and the parameter may be monotonic or non-monotonic. Signature observability that combines signature sensitivity and input-output transfer factor is used to generate test patterns for monotonic type parameters. For non-monotonic type parameters, test generation with the aim of reducing the degree of misclassification has also been illustrated. Simultaneously, a tolerance range that corresponds to the limitations imposed by the specifications is obtained. A continuous time state-variable filter example circuit has been used to demonstrate the test generation procedure and to show the effectiveness of the generated test frequency in increasing the signature observability and reducing the degree of misclassification of the observed signature.

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