A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13μm CMOS Process

Chun-Cheng Liu+, Soon-Jyh Chang++, Guan-Ying Huang, Yin-Zu Lin

Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan
Email+: jasonkingleo@sscas.ee.ncku.edu.tw and Email++: soon@mail.ncku.edu.tw

Abstract

This paper reports a 10-bit 50MS/s SAR ADC with a set-and-down capacitor switching method. Compared to the conventional method, the average switching energy is reduced about 81%. At 50MS/s and 1.2V supply, the ADC consumes 0.92mW and achieves an SNDR of 52.78dB, resulting in an FOM of 52fJ/Conversion-step. Fabricated in a 0.13μm 1P8M CMOS technology, the ADC only occupies 0.075mm^2 active area.

Introduction

In conventional successive approximation register (SAR) ADCs, the primary sources of power dissipation are the digital control circuit, comparator and the DAC capacitor array. The digital power reduces with advancement of technology. However, the power of comparator and capacitor network is limited by mismatch and noise issues. Recently, several energy-efficient switching methods [1][2] have been presented to reduce the switching energy of the DAC capacitor network. These works reduce the unnecessary energy wasted in switching sequence. However, the SAR control logic becomes more complicated due to the increased capacitors and switches. This work proposes a set-and-down switching method to save the power consumption in switching procedure without splitting or adding any capacitors and switches. In addition, the method also improves the settling speed of the DAC.

Circuit Description

Fig. 1 shows the schematic of the proposed SAR ADC. At sampling phase, the top plates of the capacitors sample the input signal via the bootstrapped switches. At the same time, the bottom plates of capacitors are reset to V_{ref}. Next, the comparator determines which terminal has higher voltage potential. Then, only one relevant capacitor is turned down to ground. After the DAC voltage is settled. The comparator determines which terminal is higher again. The procedures repeat until the LSB is decided.

The switching sequence of this approach does not require up-transition. With the same transistor size, the on-resistance of a NMOS switch is only about 1/3 of a PMOS one. Using only down-transition without up-transition in capacitor switching sequence enhances the DAC settling. In addition, for an n-bit proposed ADC, the number of unit capacitors in a capacitor array is 2^{n-1} which is only half of a conventional one.

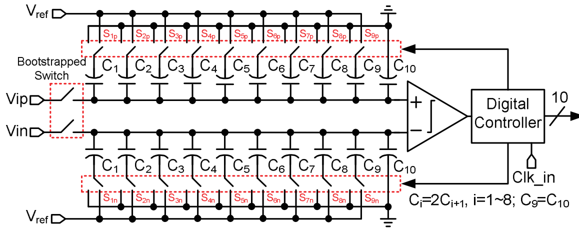

Fig. 1. The proposed SAR ADC.

Fig. 2 shows a 3-bit example of the proposed switching procedure. For an n-bit conventional SAR ADC, the average switching energy can be derived as [2]

$$E_{total,n-bit} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{ref}^{\ 2} \tag{1}$$

The average switching energy for an n-bit ADC using the set-and-down switching sequence can be derived as

$$E_{total,n-bit} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{ref}^{\ 2} \tag{2}$$

For a 10-bit SAR ADC, the conventional switching procedure consumes 1365.3CV_{ref}^2 while the proposed set-and-down switching procedure only consumes 255.5CV_{ref}^2. The proposed technique contributes about 81% switching energy reduction than the conventional switching scheme. On the contrary, split capacitor [1] and energy-saving [2] switching methods only provide 37% and 56% reduction, respectively. Fig. 3 shows the energy comparison of those methods for varying output code. For device matching, a unit capacitor of 10fF is used and the total input capacitance is 5.12pF in each terminal.

Fig. 4 shows the schematic of the comparator without static power consumption. In order to work in a common-voltage range from $V_{ref}/2$ to ground, the comparator utilizes a p-type input pair.

Experimental Result

This ADC is fabricated in a 1P8M 0.13μm CMOS process. The micrograph is shown in Fig. 5. The active core area is 0.075mm^2 (250μm x 300μm). At 50MS/s and 1.2V supply, the SNDR and SFDR are 52.8dB and 67.7dB at 2MHz input frequency, respectively. When the input frequency is up to 50MHz, the SNDR and SFDR are 50.94dB and 60.09dB, respectively. Fig. 6 summarizes the measured dynamic performance versus input frequency. The measured peak DNL and INL are +0.88/-1.00 LSB and +2.20/-2.09 LSB, respectively. The ADC performance is limited by the underestimated comparator offset.

The power dissipation consumed by analog circuits including the comparator, T/H circuit and capacitor network is 0.39mW. The digital power consumption is 0.53mW. The total power consumption of the ADC is 0.92mW. The resultant FOM is 52fJ/conversion-step.

Table I summarizes the comparison with state-of-the-art ADCs [3-5]. The result shows our work is comparable to those excellent designs with similar speed and resolution.

Acknowledgement

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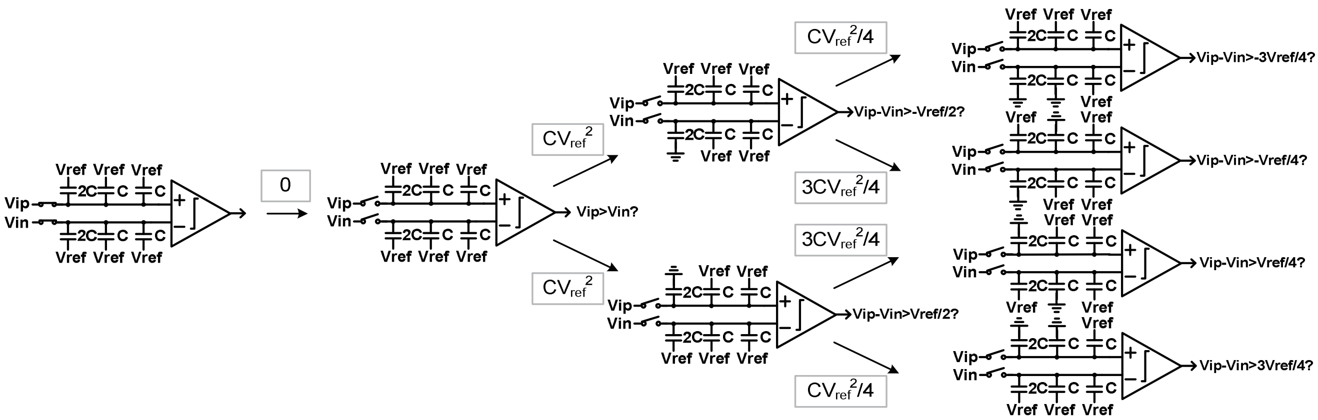

Fig. 2. A 3-bit example of proposed set-and-down switching procedure.

References

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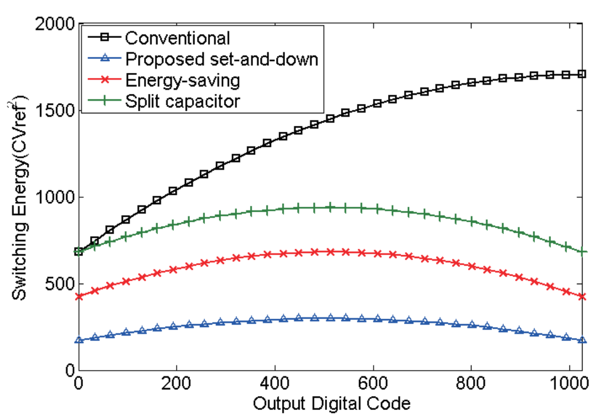

Fig. 3. Switching energy vs. output digital code.

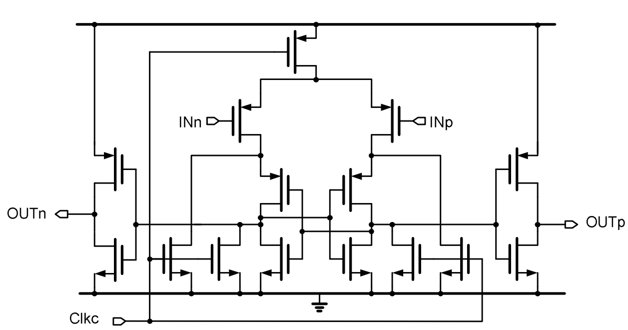

Fig. 4. The schematic of the comparator.

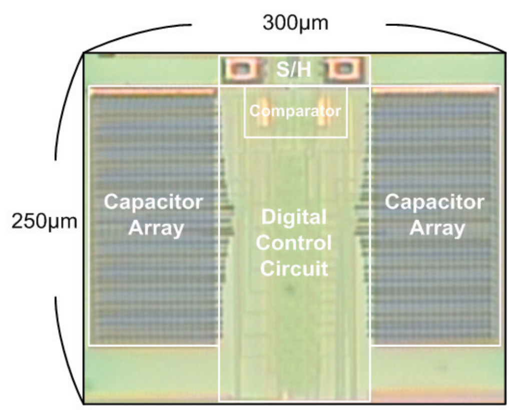

Fig. 5. Die photo of the proposed SAR ADC.

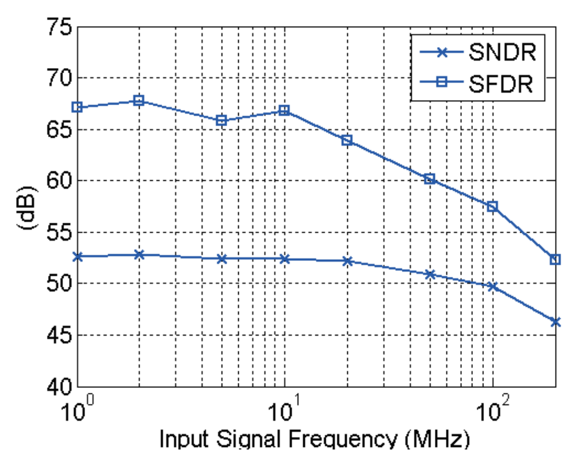

Fig. 6. SFDR and SNDR vs. input frequency at 50 MS/s.

Table I: Comparison to state-of-the-art works

	[3]	[4]	[5]	This work
Architecture	SAR	SAR	Pipelined	SAR
Process	90nm	90nm	90nm	0.13μm
Supply	1V	1V	1.2V	1.2V
Resolution	9bit	9bit	9.4bit	10bit
Sampling rate	50MS/s	40MS/s	50MS/s	50MS/s
SNDR	49dB	53.3dB	49.4dB	52.8dB
ENOB	7.84 bit	8.56 bit	7.91 bit	8.48bit
Power	0.73mW	0.82mW	1.44mW	0.92mW
FOM	65fJ/Step	54fJ/Step	119fJ/Step	52fJ/Step
Core area	0.08 mm^2	0.09 mm^2	0.123 mm^2	0.075 mm^2