4.4 A 5b 800MS/s 2mW Asynchronous Binary-Search ADC in 65nm CMOS

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Digital wireless communication applications such as UWB and WPAN necessitate low-power high-speed ADCs to convert RF/IF signals into digital form for subsequent baseband processing. Considering latency and conversion speed, flash ADCs are often the most preferred option. Generally, flash ADCs suffer from high power consumption and large area overhead. On the contrary, SAR ADCs have low power dissipation and occupy a small area. However, a SAR ADC needs several comparison cycles to complete one conversion, which limits its conversion speed. The highest single-channel operation speed of previously reported SAR ADCs is 625MS/s [1]. The ADC in [1] utilizes a 2b/step structure. For non-multi-bit/step SAR ADCs, the highest reported conversion rate is 300MS/s [2]. The structure of a comparator-based binary-search ADC is between that of flash and SAR ADCs [3]. Compared to a flash ADC (high speed, high power) and a SAR ADC (low speed, low power), a binary-search ADC achieves balance between operation speed and power consumption. This paper reports a 5b asynchronous binary-search ADC with reference-range prediction. The maximum conversion speed of this ADC is 800MS/s at a cost of 2mW power consumption.

Figure 4.4.1 depicts a conventional 3b asynchronous binary-search ADC. The number in the comparator represents the position of the reference voltage in the full-scale range. The first comparator compares the input signal with the middle reference level, 4/8. Depending on the decision of the first comparator, either Comp (6/8) or Comp (2/8) is activated. If Comp (6/8) is activated, it subsequently activates either Comp (7/8) or Comp (5/8). The procedure repeats until the final bit is obtained. Figure 4.4.2 shows the asynchronous binary-search ADC. Similarly, the clock signal is only applied to the first comparator. The output signals of the first comparator are the trigger signals of the 2nd-stage comparators. Once the first comparator makes its decision, one of the 2nd-stage comparators starts the comparison between the input signal and reference level. The decision of the first comparator also serves as the control signal to the reference-switching multiplexer in the 3rd-stage. There are four possible reference levels in the 3rd stage. If the output code of the first comparator shows V_{in} > 4/8, then only 5/8 and 7/8 are the possible references since 1/8 and 3/8 are smaller than 4/8. The selected reference voltages, e.g. 5/8 and 7/8, connect to the 3rd-stage comparators via the reference multiplexer. The comparison of the 2nd-stage comparator and switching of the reference voltages of the 3rd-stage comparators occur simultaneously. The settling time of the switched reference voltages must be shorter than the comparison. When the comparison of the 2nd-stage completes, the triggered 3rd-stage comparator begins its comparison. At this time, the reference voltages of the 3rd-stage comparators have already settled. The accuracy of comparison is guaranteed and no conversion time is wasted. The asynchronous circuit also avoids the requirement of a high-frequency clock. The structure reduces the number of comparators at the expense of increased complexity in the switching network, which tends to grow exponentially with resolution. Nonetheless, in this design it is advantageous to exploit this tradeoff toward minimizing the comparator count.

Binary-search ADCs require sampling circuits such as THAs or SHAs to hold sampled input signals for repeating comparisons. A conventional n-bit binary-search ADC requires 2^n–1 comparators, where only n comparators are activated during one conversion cycle. Theoretically, only one comparator is activated at any moment of the comparison phase. The THA of a conventional binary-search ADC has to drive 2^n–1 comparators. Although most of the comparators are inactive, the cutoff transistors still induce parasitic capacitances to the THA. The proposed circuit only needs 2n–1 comparators, which simplifies THA design. Although a 1b/step SAR ADC only has one comparator, the recovery of the comparator and settling of the DAC limit the conversion speed of a SAR ADC.

Figure 4.4.3 shows the simplified block diagram of the ADC, which consists of a passive THA [3], a reference ladder, 9 comparators, 56 p-type switches and static logic circuits. Low supply voltage limits the linearity of the source follower. The passive THA provides high-quality sampled signals for the comparators. The first comparator, Comp 5, determines the selection of the reference voltages of the 3rd-stage. The 1st-stage and 2nd-stage comparators together select the reference voltages of the 4th-stage comparators. Since both the input signals and reference voltages are differential, one pair of reference voltages is selected among four pairs to a comparator. Likewise, the reference voltages of the 5th-stage comparators are decided by the first three stage comparators. One pair of reference voltages is selected among eight pairs. The logic circuits in this work employ static types to minimize static power consumption. Because comparators are activated in turn during a conversion cycle, a latch-based comparator without static power consumption is selected. In the reset phase, both outputs are forced to ground (logic 0). If the comparator is triggered, one output is at V_{DD} (logic 1) and the other one is at ground due to latch regeneration. TSPC flip-flops running at full clock rate synchronize the output signals of the comparators. For measurement, the synchronous data are sampled by TSPC flip-flops clocked by an external trigger signal.

The ADC is fabricated in a 1P6M 65nm CMOS process with Metal-Oxide-Metal (MOM) capacitors. Figure 4.4.7 shows the die micrograph and zoomed layout view of the ADC core, which occupies 150×120μm^2 active area. The nominal resistance of the reference ladder is 240Ω. Excluding output buffers, the active circuits (comparators, logic circuits and flip-flops) and ladder consume 1.39mW at 500MS/s and 1.97mW at 800MS/s. Figure 4.4.4 illustrates the measured DNL and INL at 800MS/s. The peak DNL is 0.56 LSB and the peak INL is 0.62 LSB. Figure 4.4.5 displays the measured dynamic performance at 800MS/s. For measurement, the output data are decimated by a factor of 4 at 800MS/s. When the input frequency is 400MHz, the ADC achieves 26.92dB SNDR and 35.90dB SFDR. Figure 4.4.5 also shows that the ENOB is 4.40b and ERBW is 700MHz at 800MS/s. The resultant FOM is 116fJ/conversion-step. When the sampling rate increases to 1GS/s, the ENOB decreases to 4.2b. Figure 4.4.6 shows the specification summary at 500 and 800MS/s, where the nominal input range is 600mV. When the input range extends to 800mV, the ENOB becomes 4.60b at 800MS/s. This work demonstrates the power efficiency and high-speed potential (up to 800MS/s) of an asynchronous binary-search ADC with reference-range predication.

Acknowledgment:
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References:
[1] Z. Cao, S. Yan, and Y. Li, "A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 542-543, Feb. 2008.
[2] S.-W. M. Chen and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 574-575, Feb. 2006.
[3] G. Van der Plas and B. Verbruggen, "A 150MS/s 133μW 7b ADC in 90nm Digital CMOS Using a Comparator-Based Asynchronous Binary-Search sub-ADC," *ISSCC Dig. Tech. Papers*, pp. 242-243, Feb. 2008.

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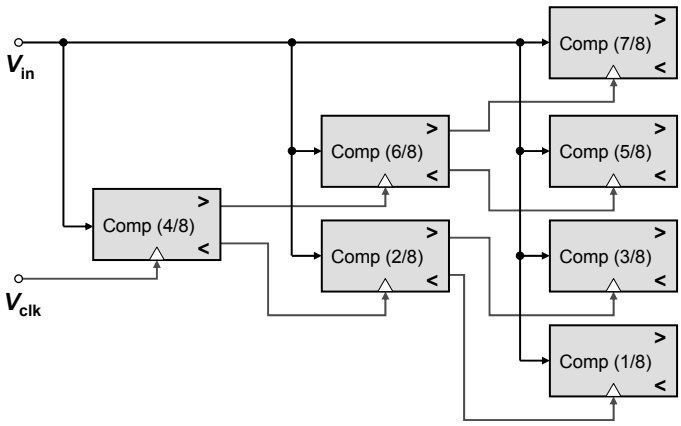

Figure 4.4.1: A conventional 3b asynchronous binary-search ADC.

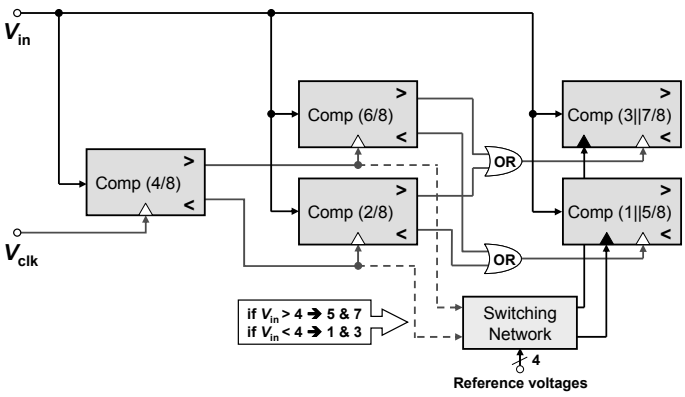

Figure 4.4.2: Asynchronous binary-search ADC with reference-range prediction.

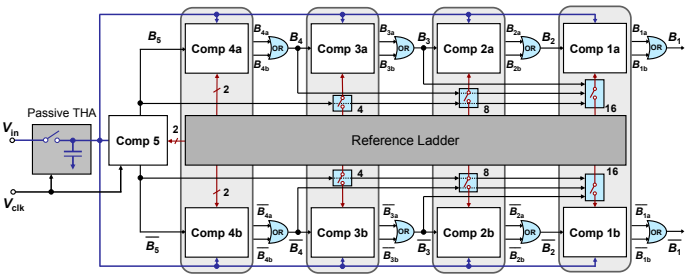

Figure 4.4.3: Simplified block diagram of the binary-search ADC.

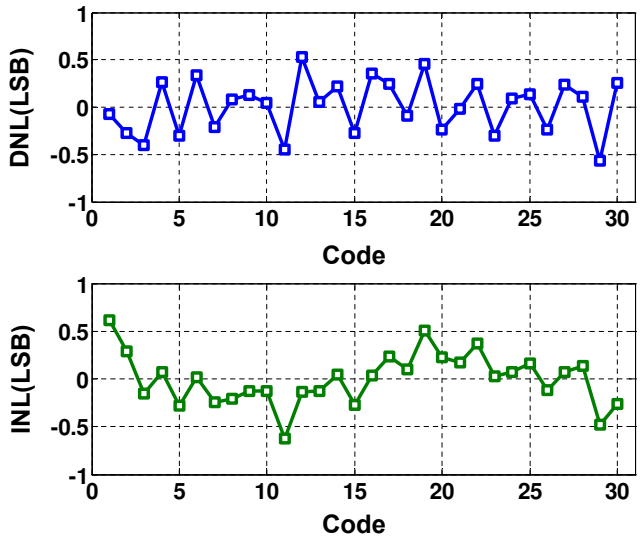

Figure 4.4.4: DNL and INL at 800MS/s.

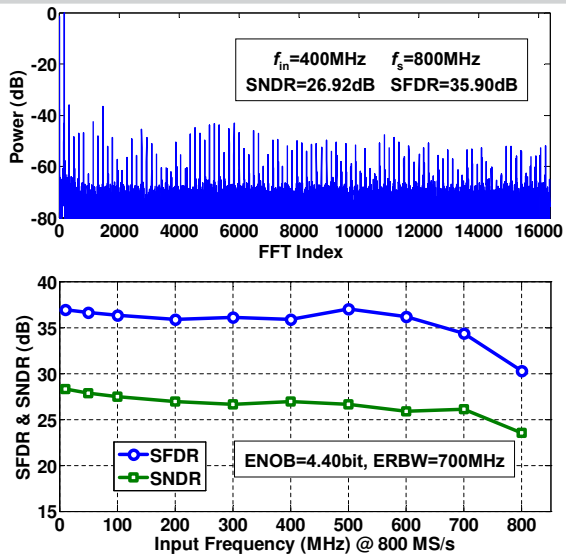

Figure 4.4.5: FFT spectrum, and SFDR and SNDR versus input frequency at 800MS/s.

Specification (Unit)	Experimental Result	
Supply Voltage (V)	1	
Input CM Voltage (V)	0.8	
Input Range (V_{pp})	0.6	
Sampling Capacitance (pF)	1	
Active Area (mm^2)	0.018	
Peak DNL / INL (LSB)	-0.56 +0.53 / -0.62 +0.61	
Sampling Rate (MS/s)	500	800
Power (mW)	1.39	1.97
ENOB (bit)	4.52	4.40
ERBW (MHz)	500	700
FOM (fJ/conv.-step)	121	116

Figure 4.4.6: Specification summary.

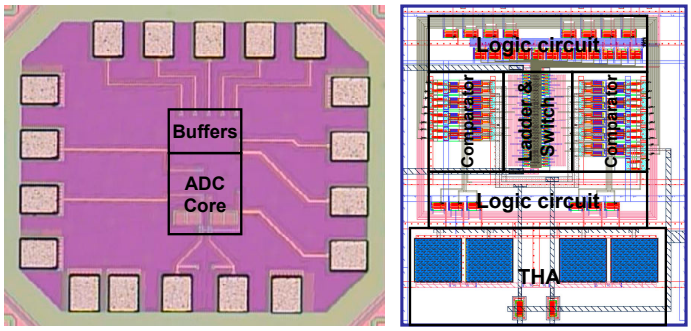

Figure 4.4.7: Die micrograph and core layout view.

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